The Test Stand System for the PHENIX iFVTX Silicon Detector

Ryan A. Rivera, Marcos A. Turqueti

Abstract — **PHENIX is the largest of the four experiments currently taking data at the Relativistic Heavy Ion Collider (RHIC), and the iFVTX is a new pixel tracker which will be installed in the forward tracker region of PHENIX. Fermilab has developed a complete test stand system for the examination of FPix2.1 modules, hybrids, and pixel chips that will be installed in the iFVTX. The system is currently in use for chip, module, and wafer testing at Fermilab. The test stand architecture is flexible and can be adapted to new requirements. In this paper, the software and hardware integration will be discussed followed by an analysis of the advantages of choosing a modular approach for the system. Finally, a selection of tests supported by the system, along with sample results, will be presented and explained.**

Index Terms — **Data Acquisition, FPix2.1, iFVTX, PHENIX, Test Stand.**

I. Introduction

THE test stand system for the iFVTX silicon detector of the Pioneering High Energy Nuclear Interaction eXperiment (PHENIX) is designed to analyze and characterize the pixel chips that will become part of the future detector [1]. The information gathered and generated by the test stand will be used to determine the quality of every potential detector chip. Since the system will be operated during the research, development, and production phases of the PHENIX project, it is crucial that the system provide pertinent grading mechanisms, user-friendly interfaces, and timely results.

It is also important for the test stand to facilitate the accurate interpretation of the data to avoid inefficiency. Too many false positives and the detector will not function; too many false negatives and money is wasted. Great care had to go into the design of the test stand such that neither condition ensued.

At various stages in the detector's production pipeline, individual chips and multi-chip modules must be diagnosed by the test stand. The defective chips will then be filtered out in an effort to minimize the number of faulty components that ultimately reach the detector. Furthermore, the chips that meet the quality standards of the detector must be calibrated – another task of the test stand – in order to associate meaning to their output.

The flexibility and utility to attain all of the aforementioned results are provided by the software and hardware components of the test stand presented in this paper.

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II. Integration of Software and Hardware

The flexibility afforded by software allows for a more natural interface to hardware. The PHENIX test stand takes advantage of this fact – with firmware to bridge the gap. This section will offer an overview of the system as the data path is traversed from its origin, the pixel chip, to its final destination, the application-level software.

A. Hardware

The focal point of the test stand is the FPix2.1 pixel readout chip shown in Fig. 1 [2], [3]. The readout chip is the entity that generates the data, receives commands, and requires diagnosis. It is capable of generating hit data in two ways: by either detecting electrical charge that is deposited on the surface of a bump-bonded sensor, or by detecting artificial charge imparted through its test-inject line.

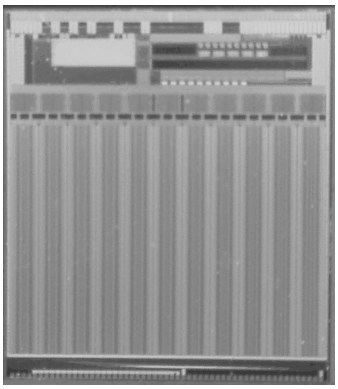

Fig. 1. An FPix2.1 bare readout chip is shown above. The 22 vertical columns claim most of the chip with the end-of-column logic and digital components in the upper third of the image.

The first method requires a hybrid chip; the readout chip together with a sensor is referred to as a hybrid. A hybrid is capable of detecting charge on its sensor with extraordinary sensitivity and precision by amplifying the signal generated by

a passing particle. With proper calibration, charged particles differing by only 200 electrons can be discriminated and their positions known to a precision of better than 6 μm using the 22 by 128 pixel grid of the FPix2.1.

The alternative hit generation method, exploiting the test-inject line, does not require the chip to have a sensor. This method is useful for the purposes of debugging, calibrating, and diagnosing readout chips. It provides a mechanism to mimic a hit by injecting an artificial pulse to a specified pixel.

Although the sources may be different, the hit response to either method is the same. When a hit is detected, the row and column information associated with the affected cells is reported, along with a 3-bit ADC value and time stamp.

The next piece in the data path is the High Density Interconnect (HDI). Due to the small size and numerous signals of the FPix2.1, feature size constraints are demanding. These constraints, together with the added requirement of low mass, make the HDI a necessity. The HDI is a flex circuit with 50 μm copper traces, 50 μm center-to-center pitch, and 150 μm via pads [4]. Up to eight readout chips can be installed on a single HDI flex circuit. These eight-chip modules are the building blocks of the iFVTX detector [5]. The HDI has the responsibility of carrying the signals between the pixel chip and the port card.

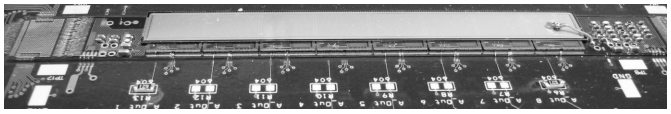

Fig. 2. In the figure, the four hardware layers are visible. The large rectangular sensor, biased with high voltage on the right, can be seen situated atop eight FPix2.1 readout chips. The hybrids are wire bonded to the HDI, which is wire bonded to the port card.

The port card is a printed circuit board that provides a packaged testing interface for the HDI and any number of chips present on the HDI. The port card includes access to the power and signal lines of the HDI. Also, the board is designed to fit into a plastic dark-box to prevent ambient light from affecting the device under test.

B. *Firmware*

The firmware is the means by which communication can occur between the software and the hardware. The firmware carrier for this test stand is the Xilinx Virtex-4 FPGA. It is situated on a PCI compatible board known as the PTA2 [6].

The firmware allows for the transfer of control signals, from PC to chip, and of data, from chip to PC. In short, it does this by converting the LVDS signals, which make up the chip interface, to PCI bus data lines that make up the PC interface.

The clocks for the readout chip are also generated by the firmware; additionally, the firmware serializes and deserializes data to provide the compatibility across platforms. It is an essential link between the FPix2.1 and the application-level software.

C. *Software*

The end of the data road lies within the application-level software. The main software application for the PHENIX test stand is known as *Pinga*. It was designed using Microsoft Visual C++ as an MFC application because of the readily available modular features included with such an application, and the modular approach to which test stands lend themselves.

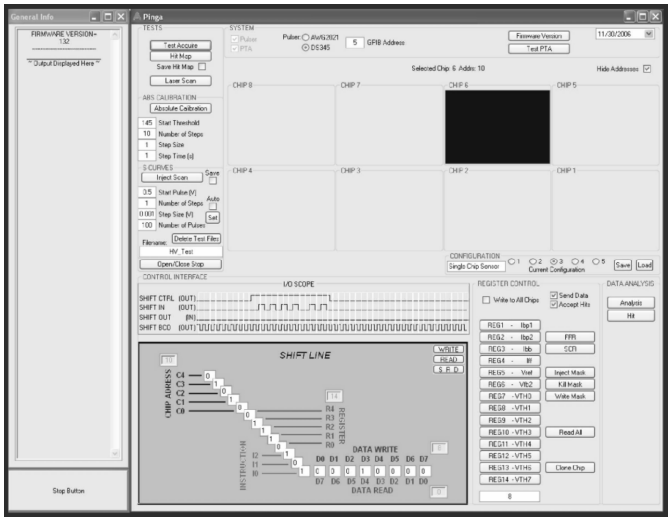

Fig. 3. Shown above is *Pinga*, the graphical user interface to the PHENIX test stand, where real-time display occurs and commands to the FPix2.1 are generated.

There are also several add-on software applications for offline data analysis. *Pinga* does most of the real-time data acquisition and real-time graphical display, but for extensive calculations and more insightful illustrations the computation has to be done offline.

III. The Modular Approach

Prior to assembling the test bench, careful planning went towards incorporating a modular approach into every aspect of the design.

Currently, with respect to the firmware and software, chips can be transparently added to and subtracted from the system. The infrastructure is also present to allow multiple modules per PTA card, and multiple PTA's per PCI bus.

Regarding the actual software source code, the entire design is modular. Microsoft Visual C++ facilitates the use of message-to-module interfaces – where actions taken by the user set off messages, which in turn trigger the execution of blocks of code. This type of interface is useful for quickly adding and removing functionality.

The concept of software modularity focuses on a building block approach. Simple blocks, such as writing or reading a byte of data, are built upon to create incrementally more complicated blocks.

The modular approach extends to applying C++ coding concepts such as virtual classes, dynamic allocation, and polymorphism wherever suitable. Also, an important software design notion was incorporated by including global parameters and functions. Using global entities allowed constants and repetitive tasks that were particularly useful to be accessible to every module in the design.

Finally, the modular approach promotes incremental development, which is critical when just beginning to understand a chip. At such time, it is not well understood which tests are indeed pertinent, which features need to be scrutinized, or what it means to fully characterize a chip.

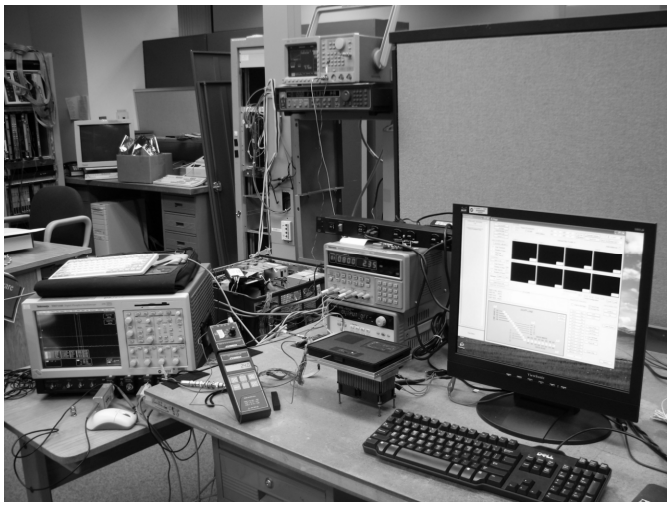

Fig. 4. An example PHENIX test stand implementation is shown above. On the left there is an oscilloscope. In the middle, from top to bottom, there is a pulse generator, a high voltage supply, two low voltage supplies, a thermocouple temperature readout device, and an 8-chip test module (in a dark-box and on a cooling plate). On the right, *Pinga* is running.

IV. Supported Tests and Results

This section will discuss and give example results of the various diagnostics that the PHENIX test bench can administer to the FPix2.1 readout chip. All of the following tests can be applied to individual chips or modules of up to and including eight chips.

A. Bare Chip Diagnostics

These tests can be run without an accompanying sensor bump-bonded to the chip in question, and are usually done on the wafer before the individual chips are diced.

1) Register Write/Read: This is the lowest level functionality diagnostic that the *Pinga* application platform offers. This test consists of a register write followed by a subsequent read. A chip can immediately be cast off as *bad* if a value can not be written and then read back from every register on the chip.

2) Test Acquire: This test allows for the manual selection of pixels to inject through their test-inject lines. When Test Acquire is run, a test charge created by a pulse generator is applied to the cells that are selected by the user.

It is then possible to view which pixels fired, as expected, via the graphical user interface.

3) Inject Scan: This procedure is similar to Test Acquire except that it tests every pixel on the chip systematically. This is needed to properly calibrate the FPix2.1 readout chip.

The calibration process injects charge on the calibration capacitor to determine the mean and dispersion, of the threshold and noise, of the chip [7]. Characterizing the chips, and their individual pixels, is vital to associating meaning to the output and recognizing fault tendencies. Since the test stand is used as a research and development tool, these results can ultimately lead to suggested improvements for future chip designs.

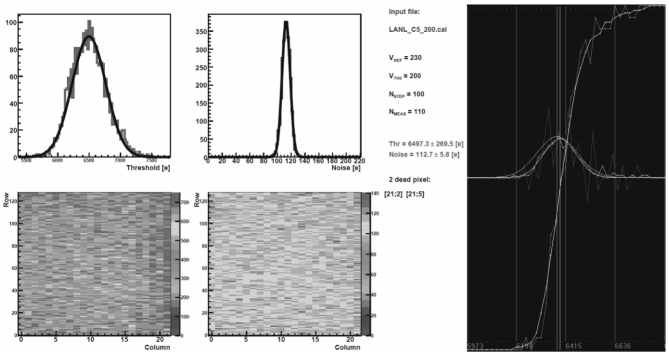

Fig. 5. Above are the results of an Inject Scan test. On the left, the threshold and dispersion parameters are displayed for an example FPix2.1. On the right, the calibration data pertaining to a single pixel is shown.

4) Trigger Capabilities: The FPix2.1 is not a triggered device, so it is always receiving and sending data. However, it can be used as a trigger source. It generates a signal known as *GotHit* that is brought high within a couple hundred nanoseconds of an incoming particle. This signal could be employed as a trigger in future systems.

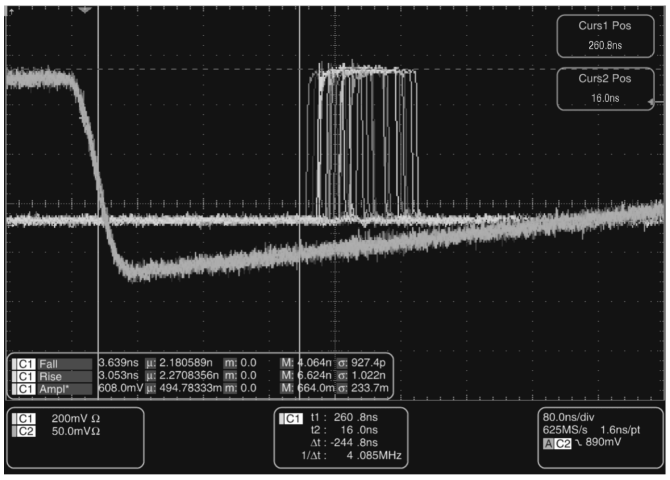

Fig. 6. Above, the square-wave signal dispersion of *GotHit* can be seen indicating the presence of a hit just 250 ns after the injected charge arrives.

The PHENIX test bench was used to determine the feasibility of using the FPix2.1 as a triggering device for a future data acquisition system. It was determined that a

suitable trigger pulse could be achieved [8], [9].

5) Stability Tests: The PHENIX test stand has the ability to map out the stability region of an FPix2.1 over the span of multiple registers. *Pinga* will incrementally mark which points in the register span are stable or unstable. The stability test is utilized to know the range of register configurations in which the chips can stably run, and whether or not the number of chips comprising a module affects the overall stability.

Similar to other tests presented here, *Pinga* records the data whereas analysis and visualization are done offline.

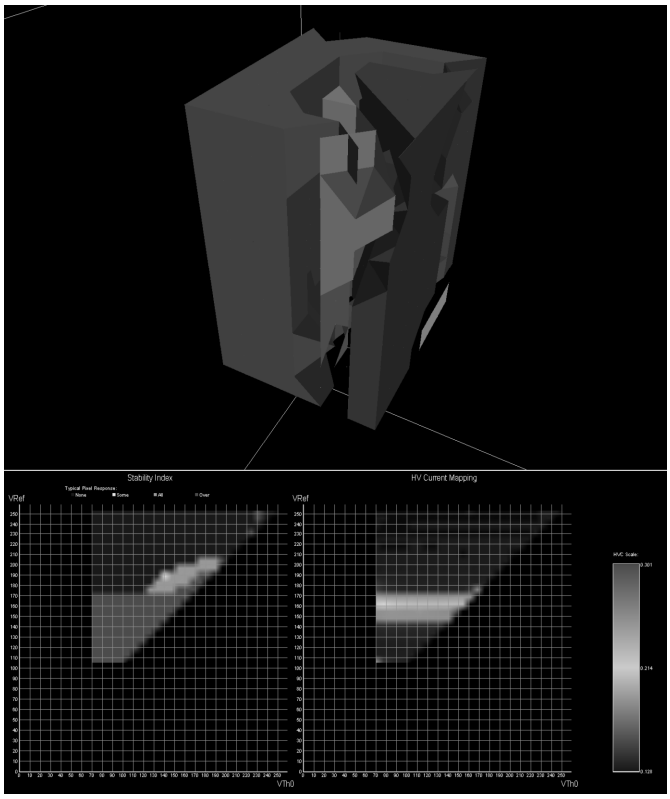

Fig. 7. At the top, a 3-D perspective of a stability mapping is shown. For this example, the registers *Vref*, *Vfb2*, and *Vth0* were spanned. At the bottom, a 2-D stability map is given along with the corresponding high voltage current map for the relationship between *Vref* and *Vth0*.

1) Automatic Wafer Testing: A wafer probe station has been fully automated using a version of the *Pinga* test bench software that was adapted to communicate with a programmable probe station. As a result, an entire wafer can be diagnosed in less than four hours, unmanned – and there are still ample opportunities for enhanced throughput.

The goal of the wafer testing is to obtain a wafer map of the *good* and *bad* bare die chips prior to dicing the wafer as part of the diagnosis chain. Removing poor performers before they even reach a test module will ultimately save time, effort, and money.

After the necessary data is recorded a wafer report can be generated like the one in Fig. 8.

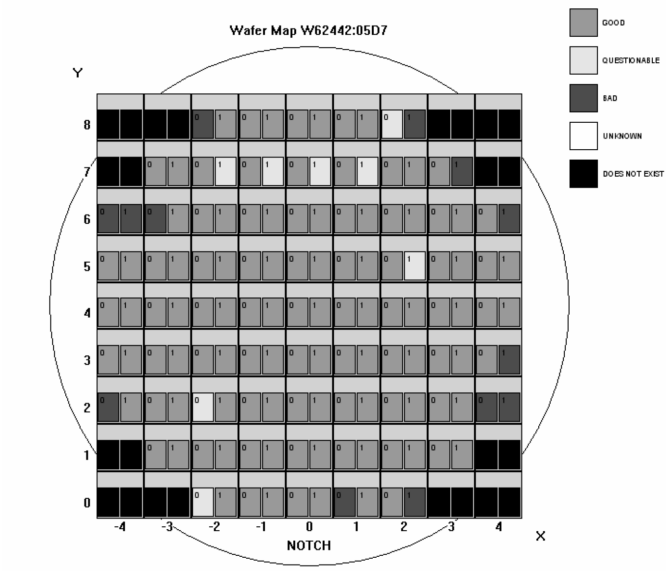

Fig. 8. A mapping of an FPix2.1 wafer is shown above. The tested cells are marked to indicate whether the chip at that position is *good*, *bad*, or *questionable*. Usable chip yield has been around 80 %.

B. Hybrid Chip Diagnostics

These diagnostics must be run with an accompanying sensor bump-bonded to the chip under test.

1) IV Curve: This test varies the bias voltage of the sensor and records the current as a function of voltage. The test is used to determine the sensor's depletion and breakdown voltage for sensors of various types and at various temperatures.

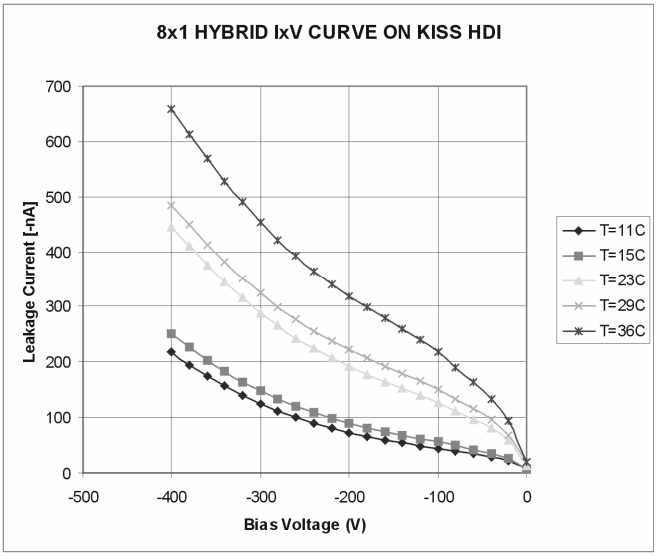

Fig. 9. Above, the temperature variant IV-Curves of a sensor are shown from an analysis done on an eight-chip module.

2) Hit Map: This test provides real-time feedback as to which pixels are firing and how frequently – usually while a chip is exposed to a controlled radioactive source.

Pinga is able to generate a real-time color coded image that provides useful threshold information along with a visual of

the radiation dispersion. Offline applications are available to further visualize the Hit Map data as shown in Fig. 10.

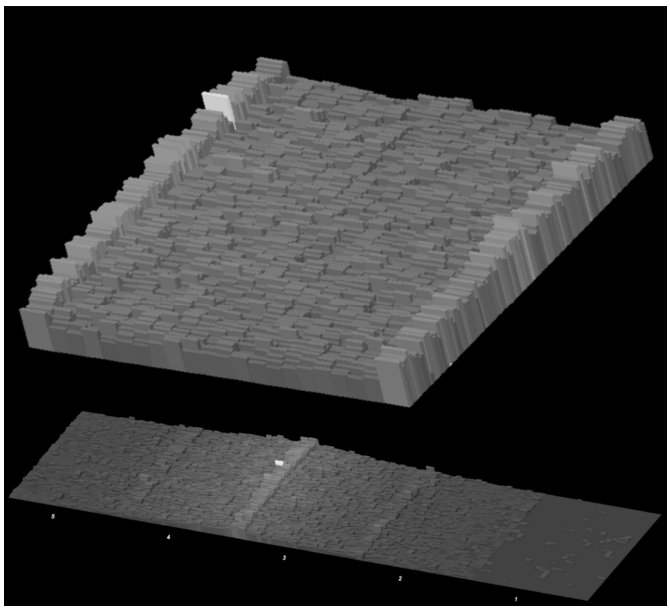

Fig. 10. The figure above shows a 3-D view of hit maps generated by an offline application. At the top, the hits were caused by a uniform radiation source centered on the chip. At the bottom, the radiation was centered between chips three and four of a five-chip module.

3) Absolute Calibration: This diagnostic is required in order to associate a concrete energy value – usually in terms of electron charge – to the ADC readout. First, the chip is subjected to radiation from an x-ray source. Then, by calibrating the ADC threshold registers of the chip, it is possible to correlate the known energy level to the binary values of the threshold registers by recording the register values when pixels begin to respond to the radiation. In this way, ADC values can be converted back to meaningful energies in post-analysis.

V. Future Work

The completion of the PHENIX test stand for iFVTX has opened the doors to many exciting projects. Plans are in place to implement this test stand as the PHENIX iFVTX production-phase testing platform. When the actual detector construction begins, every FPix2.1 eight-chip module will have to pass a series of tests conducted by this test stand in order to be included in the detector.

This test stand has also verified capabilities of the FPix2.1 that could be exploited in future applications. For one, it now seems feasible to use the FPix2.1 not only as a readout chip, but as a triggering device for future data acquisition systems.

Finally, this work will hopefully be positioned well to contribute to the ILC research and development effort – most immediately, the ILC Test Beam. The experience gained by constructing a readout chip diagnosis and data acquisition system could easily be extrapolated to a system such as the telescope for the ILC test beam to be held at Fermilab.

Acknowledgment

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