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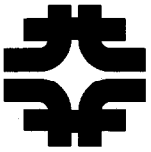

MAIN RING BEAM POSITION DIGITIZER/DISPLAY SYSTEM DESCRIPTION AND OPERATING INSTRUCTIONS

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I. GENERAL

The Digitizer/Display System is a tool used to monitor beam position for a fixed number of main ring turns and store that information for display and analysis. The system is capable of digitizing, with 12-bit resolution, analog information corresponding to beam position once every 20μs. It is expandable to four channels, each capable of storing 1024 words of information.

There are several modules in the system. The Digitizer/Transmitter module performs the actual digitizing function when requested, converts the information to a serial Di-Phase-coded form, and transmits each word along a single coaxial cable from its location (usually at a service building near a beam position detector module) to its corresponding Receiver/Memory module in the Main Control Room. The Receiver/Memory receives this information, decodes it, and stores it into a 1024-word memory. The Computer Interface module sends an interrupt to the computer after a new batch of information has arrived. If the interrupt is acknowledged, this module transfers the information, one word at a time, to the computer (without destroying the contents of the Receiver/Memory modules), generating the necessary handshake signals to achieve the transfer. Finally, each Dual Display Driver in the system converts the information in two Receiver/Memory modules back to analog and presents these signals, along with the

necessary trigger and intensity control signals, to an oscilloscope or other visual monitor for viewing.

II. OPERATING INSTRUCTIONS

A. Digitizer/Transmitter

The ARM pulse is a positive-true TTL-compatible signal which prepares the module for digitizatior After the ARM pulse, the module will digitize the first 1024 signals, beginning each digitization when a TTL DIGITIZE pulse is received. The ARM pulse should be at least 50 ns wide, and the source should be capable of driving a 50-ohm load.

The TTL DIGITIZE pulses initialize a digitizing process with each pulse. The pulse period should be at least 20µs, with pulse width of at least 50 ns. Loading is the same as the ARM input.

The ANALOG IN signal should be synchronized with the TTL DIGITIZE pulse, with constant-level width of at least 1µs. Full scale range should be ±10V max.

The Arm Mode Select switch, located on the front panel, should be set to NORMAL for most operations. In the PROMPT mode, the first TTL DIGITIZE pulse must follow less than 25µs after the ARM pulse, or the 1024 words normally transmitted will be all zeroes, corresponding to -10V at the display. In the NORMAL mode, no time limit is set.

*NOTE: Do not attach ANY input or output cables to the module while power is not applied. Also, if power is removed from the module momentarily, allow at least 5 seconds before re-applying power. Allow at least another 5 seconds before connecting any input or output signals.

B. Receiver/Memory

These modules are located in a standard NIM bin, along with the Computer Interface and Dual Display Driver modules. Interconnections between the modules are achieved via a custom wiring harness assembly. It is important that the appropriate connectors of the harness assembly be connected to the corresponding module (each module and each wiring harness connector are labeled).

For proper operation, each Recei.../Memory's sensitivity must be adjusted to the proper threshold level (see Calibration Procedures). It is important to avoid switching any SERIAL DATA IN cables of any two modules, since different threshold levels on the modules may cause improper operation.

*NOTE: Do not attach the SERIAL DATA IN cable without power being applied to the module. If power is removed from the module, allow at least 5 seconds before re-applying power. Under no circumstances should voltage level into the SERIAL DATA IN connector exceed ±5V.

The UPDATE/HOLD switch should be set to UPDATE for normal operation. When set to HOLD, all incoming data on that channel is inhibited, and the previous data is retained in memory for viewing.

C. Computer Interface

No special operating instructions are required for the Computer Interface module. This module transfers data from the Receiver/Memories to the computer after its interrupt is acknowledged.

The REFRESH LED flashes whenever new data is received by any Receiver/Memory. The OVERRUN LED flashes whenever new data is written into any Receiver/Memory while the Computer Interface is transferring

data. This is an abnormal condition and should be investigated if it occurs.

D. Display Driver

To observe data stored in two Receiver/Memory modules, a dual-trace oscilloscope is required. Connect ANALOG OUT 1 and ANALOG OUT 2 to the two vertical inputs. Connect TRIGGER to the external trigger input on the scope. If the scope has positive blanking Z-axis modulation (positive signal decreases intensity), connect NEG. INTENSIFY to the Z-axis input. If the scope has negative blanking, connect POS. INTENSIFY to the Z-axis input.

Set the oscilloscope controls as follows:

VERTICAL MODE:	Chopped
VERTICAL SENSITIVITY:	5V/div
HORIZONTAL SWEEP:	1ms/div
TRIGGER SOURCE:	External
TRIGGER MODE:	Normal
TRIGGER COUPLING:	AC
TRIGGER SLOPE:	Positive
TRIGGER LEVEL:	Approx. 2.0V

These settings should cause all 1024 words of data to appear on the scope. The vertical sensitivity can be selected as desired, and the horizontal sweep speed can be increased and/or the X10 magnifier can be used to more accurately view the data. At faster sweep speeds, it may be necessary to change the vertical mode to alternate mode.

III. CIRCUIT DESCRIPTIONS

A. Digitizer/Transmitter (Refer to 0453.00-ED-48907)

The Digitizer/Transmitter module, after receiving an ARM pulse,

digitizes 1024 analog signals, each keyed by a TTL DIGITIZE pulse. Each word of information has 15 bits:

1. First, a leading "1" bit to key the receiver.
2. A First Event bit, which is a "1" if the word is the first word in the group of 1024, "0" otherwise.
3. Twelve data bits representing ANALOG IN voltage.
4. A parity bit, generating even parity for all bits.

The information is transmitted serially in Di-Phase Code; each bit of data is transmitted as the ADC converts the data.

The ARM pulse causes a monostable to set the FIRST EVENT, VALID DATA, and DIGITIZE FF's and reset the EVENT COUNTER. When a TTL DIGITIZE pulse occurs, this pulse is delayed by a variable amount (in order to synchronize the TTL DIGITIZE pulse with ANALOG IN), then transmitted via U6 to set the CONVERT and LOAD FF's. The CONVERT FF enables U11 to turn on the LINE DRIVER beginning data transmission.

Timing is controlled by the crystal clock and DIVIDE-BY-3 COUNTER, which produces a 2-phase output (see timing diagram, $\overline{Q1}$ and Q2 outputs). The first pulse (Q2) allows U12 to generate a clock pulse via U11 to the XMT FF whenever the CONVERT FF is set. This causes the XMT FF to toggle on every Q2, generating the leading edge of each data bit in the Di-Phase code.

Gate U13-pin 6 generates the pulse for the second edge of the data bits. This pulse is enabled only if U12 pin 6 is high, so this gate contains the data information. When U12 pin 6 is high during $\overline{Q1}$ of the clock, a "1" is transmitted (a second edge in the Di-Phase code following the first edge); when U12 pin 6 is low during $\overline{Q1}$, a "0" is transmitted (absence of the second edge).

After the CONVERT FF is set and the digitize pulse at U6 pin 8 returns high, U13 pin 12 enables the next Q2 pulse to load a "1" into QA of the STATE COUNTER. This causes U12 pin 6 to go high, causing the leading "1" bit of the word to be transmitted. The setting of the CONVERT FF also causes the Sample/Hold Amp to hold the analog information at its input during the digitizing process.

The next Q2 pulse causes the "1" at QA of the STATE COUNTER to shift to QB (QA had reset the LOAD FF). U10 pin 3 then gates the output of the FIRST EVENT FF thru U12 pin 6, sending this bit as the second data bit. The next Q2 pulse causes QC of the STATE COUNTER to go high. No information is transmitted here, but a CONVERT pulse is applied to the ADC via U10 pins 11 and 8, in order to start the digitizing process. At this point, STATUS goes high, but U9 pin 2 enables the next STATE COUNTER clock pulse. This pulse shifts the "1" in the STATE COUNTER to QD. This enables U13 to gate the SERIAL OUT of the ADC to U12 pin 6. STATUS disables any further clock pulses to advance the STATE COUNTER. U10 pin 8 continues to send CONVERT pulses to the ADC, causing conversion to continue.

When 12 data bits have been transmitted, STATUS goes high, enabling the next Q2 pulse to advance the STATE COUNTER to QE (U9 pin 5). This enables the parity bit to be gated to U12 pin 6 via U10 pin 6. The PARITY FF was toggled on every "1" transmitted by U11 pin 11 and U13 pin 6. Since the PARITY FF is reset by every digitize pulse, even parity is generated.

The next Q2 pulse causes QE to go low, causing a monostable to generate EVENT COUNT. This resets the FIRST EVENT FF, advances the EVENT COUNTER and resets the CONVERT FF. It also triggers the MISSING TRIGGER DETECTOR. If another TTL DIGITIZE PULSE does not

follow within 25μs, the SUBSTITUTE TRIGGER GENERATOR provides another digitize pulse via U6 pin 12 and resets the VALID DATA FF, causing all following words to be "0".

If another TTL DIGITIZE pulse occurs within 25μs, the above process is repeated, except that the FIRST EVENT bit is "0". After 1024 words are transmitted in a similar fashion, the EVENT COUNTER causes a monostable to reset the DIGITIZE FF, ending transmission.

B. Receiver/Memory (Refer to 0453.00-ED-48908)

The Receiver/Memory module receives serial information from the transmitter, decodes it, checks for parity, and loads the valid data into a 1024 word memory.

Data is received on the SERIAL DATA IN line. The LINE RECEIVER provides a 50-ohm termination to the line and senses level changes. The 75107A detects level changes greater than the THRESHOLD level, and, combined with the DATA FF, provides a hysteresis loop with hysteresis equal to twice the threshold level, giving the LINE RECEIVER additional noise immunity.

Each level transition of DATA IN causes the EDGE DETECTORS to generate a pulse. The first edge transmitted causes U5 pin 3 to set the EDGE DETECT FF, enabling U7 pin 4 to gate 10 MHz clock pulses via U7 pin 4 to the PULSE COUNTER. U5 pin 3 also clears the PULSE COUNTER via U7 pin 1. The PULSE COUNTER counts clock pulses until QC goes high (count of 4 pulses). QC clears the EDGE DETECT FF, generating a positive clock transition at the DATA REGISTER. Since QC of the PULSE COUNTER is high, a "0" is entered into the DATA REGISTER. This implies that, if four 10MHz pulses are counted before a second edge is detected by the EDGE DETECTORS, the data bit transmitted must have been a "0". If a second edge is detected before

four 10MHz pulses are counted, the second edge resets the EDGE DETECT FF via U5 pin 3 and clears the PULSE COUNTER. A positive transition again occurs at the DATA REGISTER clock, but this time QC of the PULSE COUNTER is low, so a "1" is entered into the DATA REGISTER. With each positive edge of the clock, U35 toggles the PARITY CHECK FF via U6 pin 6 whenever the data entered is a "1".

Data is shifted into the DATA REGISTER until QG of U19 goes high. Since the first bit of each word is "1", this occurs when all data bits of a word are received. QG triggers the ADDRESS CLEAR and WRITE BUSY monostables. ADDRESS CLEAR is gated to the ADDRESS COUNTER via U9 if QF of U19 is high (the FIRST EVENT bit). Otherwise, ADDRESS CLEAR merely provides a data set-up time for the memories. WRITE BUSY disables RD CLK and RD CLR, which are used by the Computer Interface and Display Driver for readout of information.

At the end of ADDRESS CLEAR, a $\overline{WE}$ pulse is generated, causing data in the DATA REGISTER to be written into the memory location pointed to by the ADDRESS COUNTER if the PARITY CHECK FF detected even parity. Otherwise, a string of "0's" is entered. At the end of $\overline{WE}$, the SHIFT REGISTER CLEAR monostable clears the DATA REGISTER and generates $\overline{CLK}$ via U8, which advances the ADDRESS COUNTER.

C. Computer Interface (Refer to 0453.00-ED-48910)

The Computer Interface module's function is to transfer newly received data from each Receiver/Memory to a Digitizer Interface module, which in turn transfers the data to a computer input port. When new data is received, the Computer Interface sends an interrupt to the computer. If the interrput is acknowledged, the Computer Interface stops the display and begins transfer of the data, one word at a time, to the Digitizer Interface using handshake signals.

Up to four channels of information can be transmitted--the Computer Interface has capability of multiplexing up to four Receiver/Memory data contents onto its data output lines.

When a $\overline{WR}$ pulse is received from any Receiver/Memory, U8 sends a $\overline{STOP}$ pulse to the Display Driver to stop the display. When all $\overline{WR}$'s return high, U9 sets the INTERRUPT FF, sending INT to the computer. It also triggers a 3-second monostable (U9 pin 10), generates a $\overline{DISPLAY}$ pulse via U4 pin 13, and flashes a REFRESH LED. If an ACK pulse is not received within 3 seconds, U9 triggers U10 pin 2, resetting the INTERRUPT FF, aborting the transfer process. (Refer to the timing diagram.)

If ACK is received, U5 pin 1 triggers monostable U30. It also causes U2 pin 8 to set the XFR FF, turning on the tri-state outputs of the data line drivers U21-U27, clearing the 3-second monostable, resetting the INTERRUPT FF, and triggering U8 to send $\overline{STOP}$ to the Display Driver. (Note that the FIRST ACK FF was reset by U1 pin 6 during $\overline{WR}$, enabling U2 pin 8). U8 pin 12 generates RD CLR, clearing the memory address counters. At the end of the ACK pulse, a monostable sets the FIRST ACK FF. Also, U11 pin 5 generates a 1μs pulse, which causes U11 pin 13 to send a STROBE pulse via U3 pin 11, strobing the first data word into the Digitizer Interface.

If 200 ms elapses before the STROBE pulse is acknowledged, U30 pin 12 resets the XFR FF and generates a $\overline{DISPLAY}$ pulse via U29 pin 3, ending the transfer process. If ACK is received, U3 pin 8 triggers U10, causing XFR CLK to advance the memory address counters, accessing the next data word. The trailing edge of ACK again generates STROBE via U11, strobing the next data word. Data is multiplexed onto the data lines via U15-U20. U13 selects the channel to be transferred.

When all words of a channel are transferred, A9, the MSB of the memory address counter, advances U13, causing the multiplexers to select the next channel for transfer. When the final channel is transferred (selected by the solder straps at the outputs of U13), U3 pin 3 resets the XFR FF, ending the transfer process.

If a $\overline{WR}$ is received during the transfer process, U3 pin 6 flashes an OVERRUN LED. When this occurs, a new INT is generated at the end of $\overline{WR}$.

D. Display Driver (Refer to 0453.00-ED-48909)

The Dual Display Driver accepts digital information from two Receiver/Memory modules, converts it to analog, and provides the necessary control signals for display on an oscilloscope.

A $\overline{DISPLAY}$ pulse causes U1 to set the DISPLAY FF. A $\overline{STOP}$ pulse resets the FF. When set, the DISPLAY FF causes U6 pin 10 to gate the READ CLOCK to U21 pin 12, generating RD CLK, which advances the memory address counters. When reset, the DISPLAY FF allows U6 pin 11 to pass XFR CLK pulses to U21 pin 13. This allows the Computer Interface to advance the address counters during data transfer.

Refer to the Display Driver timing diagram for the following description. Each positive transition of the READ CLOCK triggers the TRANSFER DELAY monostable and generates RD CLK. RD CLK advances the address counters on the Receiver/Memory modules, and TRANSFER DELAY allows access and settling time for the data. After TRANSFER DELAY, the DISPLAY PULSE monostable gates data thru U7-U12 to the DAC's, and the PEDESTAL DELAY monostable allows the DAC's to settle to a final level. Then the PEDESTAL INTENSIFY monostable causes U17 and U18 to generate POS and NEG INTENSITY, allowing the DAC output to be visible on the scope. After PEDESTAL INTENSIFY, the DISPLAY PUSLE ends,

causing U7-U12 to remove data from the DAC inputs and apply inputs corresponding to 0V output. The BASELINE DELAY monostable provides settling time for the DAC's, and BASELINE INTENSIFY generates POS and NEG INTENSIFY, allowing the baseline dot to be visible on the scope.

As each data word is accessed and displayed, the memory address counters are advances. When the final memory location is accessed, U13 and U14 trigger the GAP WIDTH monostable, allowing the scope to retrace and disabling the READ CLOCK for this duration. At the end of the GAP WIDTH, the TRIGGER WIDTH monostable provides a TRIGGER pulse to the scope.

IV. CALIBRATION PROCEDURES

*NOTE: All the modules in the Digitizer/Display System are calibrated for proper operation. No further adjustments should be required. However, should the system operating parameters be changed, or if it becomes necessary to periodically check the system for operating accuracy, the following calibration procedures are suggested.

A. Digitizer/Transmitter

The DELAY pot provides some synchronization between TTL DIGITIZE and ANALOG IN. Monitor U1 pin 13 and ANALOG IN on a scope. The trailing edge of U1 pin 13 should fall at least 750 ns before the trailing edge of ANALOG IN. Adjust the DELAY pot accordingly.

To adjust the Sample/Hold Amp,

1. Apply 0VDC to ANALOG IN.
2. With no ARM pulses applied, adjust the VOLTAGE OFFSET until the output of U22 reads 0V exactly.

3. Apply continuous pulses of 21μs period to TTL DIGITIZE and ARM. Monitor the output of U22 with a scope. Set sweep speed at approximately 10μs/div. Vertical sensitivity should be set at ap_ ximately 50 mV/div. Adjust the CHARGE OFFSET pot until the output has as little amplitude change from 0V as possible.

To adjust the ADC,

1. Set the Digitizer/Transmitter module for normal operation, except apply a stable, adjustable DC reference voltage to ANALOG IN. Monitor SERIAL DATA OUT with a storage scope.
2. Adjust ANALOG IN to -9.998 ± 0.001V. Monitor the output of the first data word at SERIAL DATA OUT (occurs when ARM is applied). If necessary, adjust the OFFSET pot until the data string is the Di-Phase code corresponding to 110000000000011.
3. Adjust ANALOG IN to +9.993 ± 0.001V. Again monitor SERIAL DATA out. Adjust the GAIN pot until the data word out is 111111111111110.

B. Receiver/Memory

Only one adjustment is necessary on the Receiver/Memory module--the threshold voltage for the line receiver. To set this level, the corresponding Digitizer/Transmitter module should be set to transmit a known word. Monitor U5 pin 11. The THRESHOLD pot should be set at a level such that voltage at U1 pin 12 is slightly lower than

required to receive data at U5 pin 11 properly. This level should be approximately one-half the peak voltage at SERIAL DATA IN.

C. Display Driver

Timing and display intensity of the Display Driver can be adjusted if required. To set the proper timing:

1. Adjust R1 until the output frequency of the READ CLOCK is 100 KHz.
2. Adjust R2 until the trailing edge of the DISPLAY PULSE is coincident with the trailing edge of READ CLOCK.
3. Monitor outputs of both DAC's on the display scope. Increase the sweep speed until separate pedestal and baseline dots are clearly visible. Increase intensity until the transition levels are visible.
4. Adjust R4 until the intensified zone of the pedestal dot starts after the transition settling time.
5. Adjust R5 until the pedestal intensified zone ends at the beginning of the transition to baseline.
6. Adjust R8 until the baseline intensified zone begins after the transition settling time.
7. Adjust R9 until the baseline intensified zone ends at the beginning of the transition to the next pedestal dot.

The relative baseline and pedestal intensities can be adjusted by R3 and R16 (if NEG INTENSIFY is used) or R7 and R10

(if POS INTEISIFY is used). These adjustments are best made by visual inspection of the display scope traces.

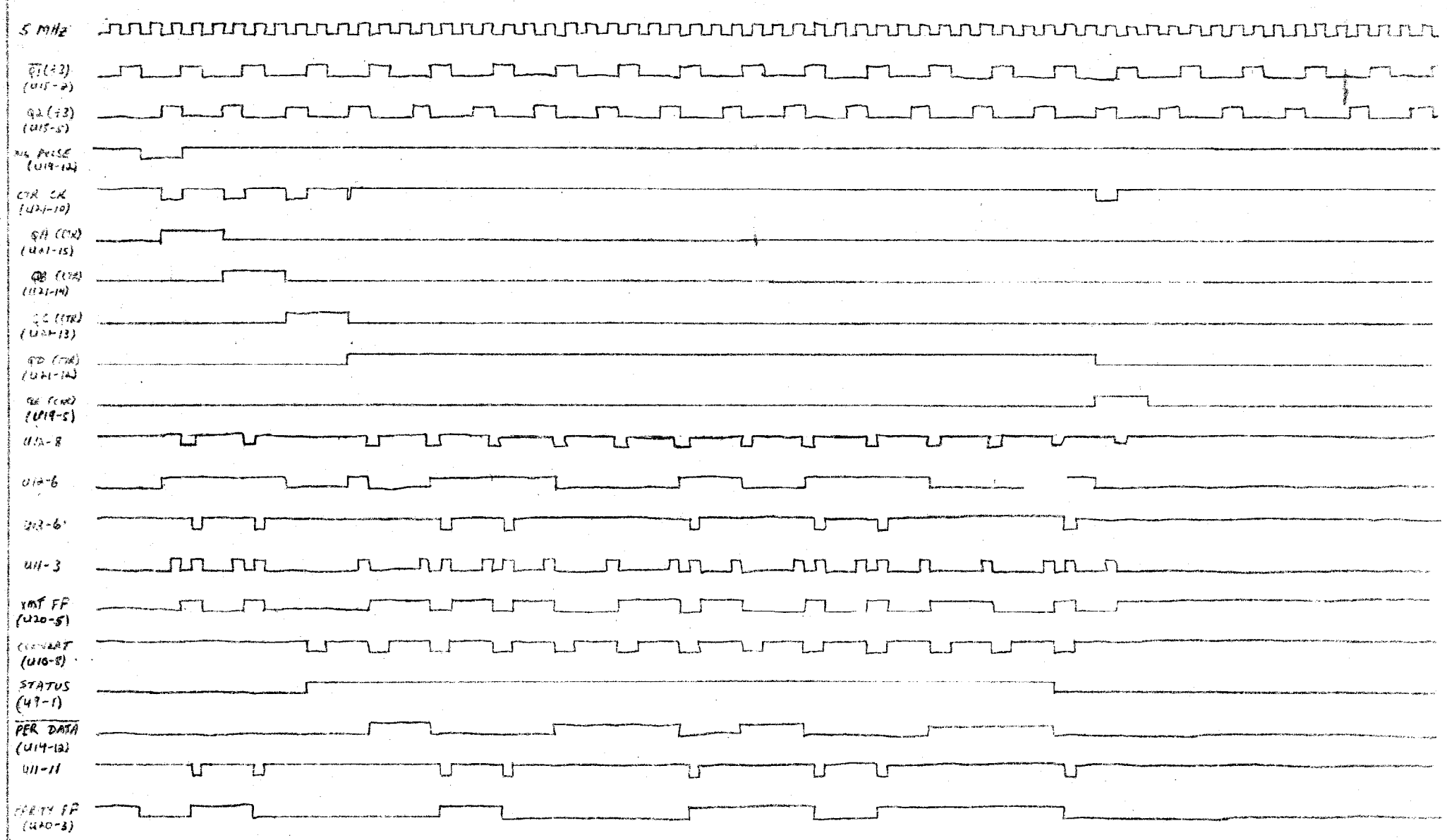
D. Computer Interface

No calibration is required on the Computer Interface module.

Attachments

GP/nep

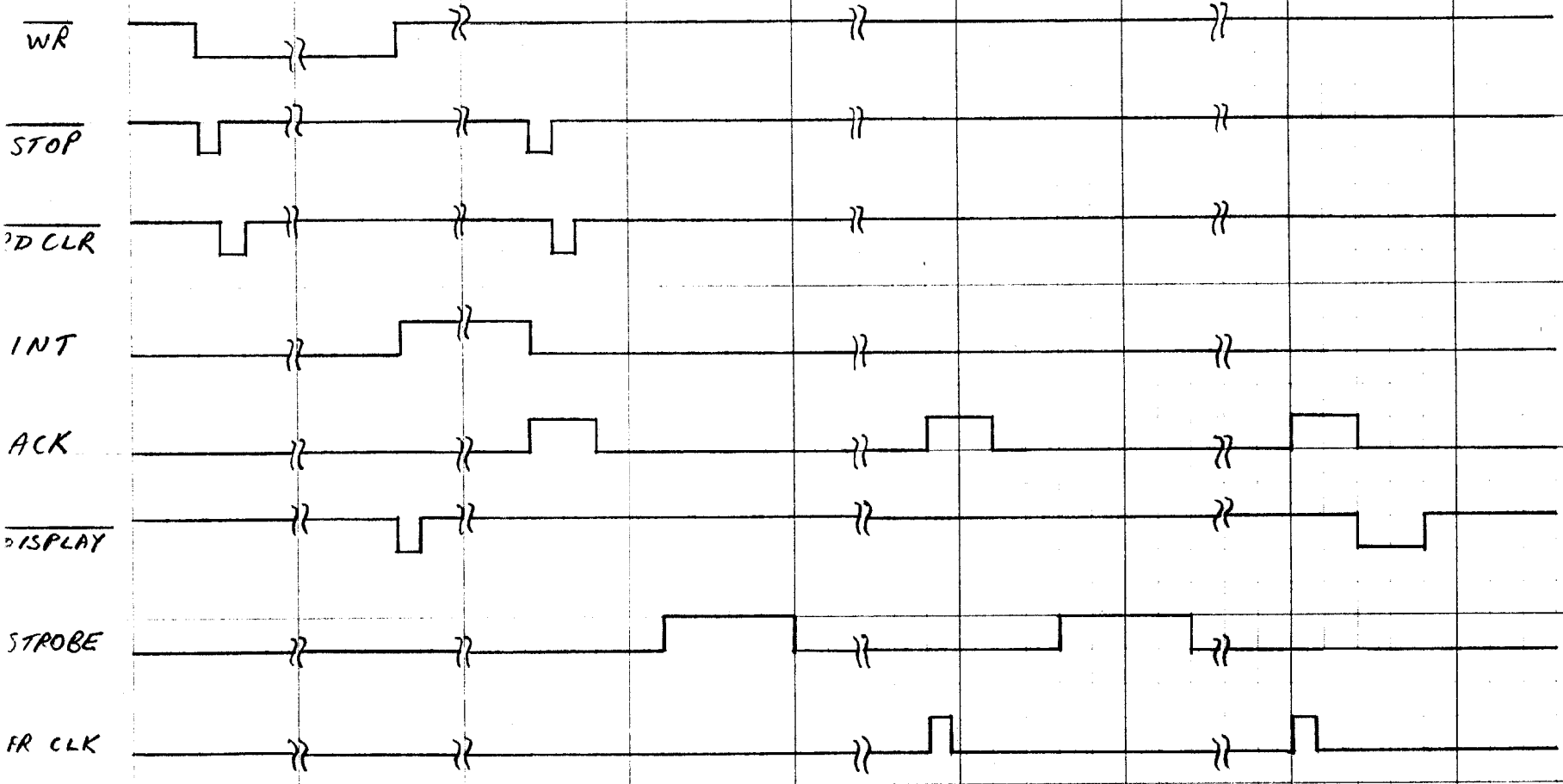
(100nS/div)



DIGITIZER / TRANSMITTER TIMING DIAGRAM

COMPUTER INTERFACE TIMING DIAGRAM

(500nS/div)



DUAL DISPLAY DRIVER TIMING DIAGRAM (ONE CYCLE)