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Electronics Engineering Tools for Modern Data Acquisition Systems

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The very large number of channels and high data rates in modern particle physics experiments put very stringent requirements on the acquisition of data. To reduce the cost as well as the number of cables required to transport the data from detector to counting room, it is necessary to use very large scale integrated circuits for pre-processing the data right on the front-end circuit boards. Also, very high speed optoelectronic circuits are needed to transport the data on to the counting room from the front-end circuits. Two techniques relevant to data acquisition are discussed. The first is Field Programmable Gate Arrays (FPGAs), including using the Very High Speed Integrated Circuit Hardware Description Language (VHDL) to program them. The second is the design of a very high speed optoelectronic circuit for data transport.

PACS numbers: Valid PACS appear here

I. INTRODUCTION TO FPGA'S

In the first part of this course, we will work with a type of programmable logic device called a Field Programmable Gate Array, or FPGA. These chips are used extensively in data acquisition systems for experiments, not only in particle physics, but also in astronomy and astrophysics. Thus, they are likely to be found underground, on the tops of mountains, or even in space. They are useful in everything from simple test stands to full data acquisition systems. Since they are so ubiquitous in scientific work, you, as physicists, are likely to work with FPGA's at some time in your careers, either designing boards containing FPGA's, programming them to do specified tasks, or providing firmware. Even if you do not have direct responsibility for such a system, your familiarity with these, as with any part of the apparatus in the experiments on which you work, makes you a more knowledgeable and valuable collaborator.

A. Flavors and Architecture

There are a number of companies which manufacture FPGA's. The chips can differ in the methods used to program them and thus the number of times they can be reconfigured. Some can be programmed only once[1], since the chips are configured by burning a set of fuses to break connections that are not wanted in the device (called antifusing). Once they are configured, they cannot be reconfigured. The disadvantage of this approach is that once a large number of boards is manufactured containing these devices, it is extremely impractical to remove and replace the chips if they turn out to have a logic error. The advantage to this type of FPGA is that they are relatively radiation hard and thus are especially appropriate for use in so-called embedded systems, where the programmable logic is placed on or near the front end electronics cards, or for use in space-based applications. Others [2] are flash programmed and can be reprogrammed as many as several thousand times. They are non-volatile, i.e., keep their configuration after power is turned off. With some effort, these chips can be reconfigured in the field. This takes several seconds per chip and these devices are relatively expensive.

By far the most common type, or flavor, is the static ram, or SRAM, based FPGA[2–7], which is programmed dynamically by downloading appropriate code and can be reprogrammed an unlimited number of times. Additional circuitry, either on or off chip, is required to load the configuration into the FPGA after power on. Reconfiguration is fast, and some devices even allow partial reconfiguration during operation. The down side is that since these chips are transistor based, they are not radiation hard. As is also the case for memory chips and microprocessors, a bit-flip can occur when an energetic charged particle traverses the active region of a transistor creating electron-hole pairs as shown in Fig. 1. This phenomenon is known as Single Event Upset, or SEU,

Although the devices from different vendors differ somewhat in their architecture and feature sets, they tend to have similar design properties. The most com-

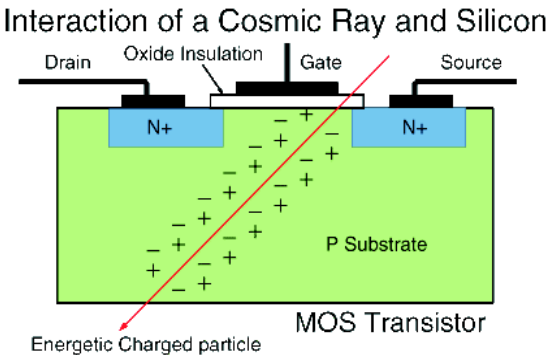


FIG. 1: Charged particle traversing active region of a transistor producing electron-hole pairs.

mon structure is an array of configurable logic blocks, called CLB's, at the center of the chip surrounded by a perimeter of input/output blocks, called IOB's. Both are programmable. The CLB's provide the functional elements for determining the logic. The IOB's provide the interface between the package pins and this internal logic. Typical chips also contain dedicated BlockRAM memories of 4096 bits each and clock DLL's for clock distribution, delay compensation and clock domain control. The overall design allows for a versatile, multi-level interconnect structure. The Spartan II FPGA from XILINX shown in Fig. 2 is an example of this typical architecture.

B. Configuration Methods and Tools

In order to use these very versatile and flexible devices, you will need a design entry method and design entry tools. Possible methods are to use a hardware description language (HDL) editor, a state machine editor, or a block diagram editor. Design tools specific to a particular chip set can be purchased directly from the chip vendor, or one can purchase design entry software that is more general and thus can be used for devices from many different vendors.

Advantages of using an HDL are that it reads like any other software language. It allows the inclusion of comments and is easy to document. Also, text files are easy to share across tools, platforms, and sites. However, HDL code is not as easy to read as a graphical language, i.e., state machine or block diagrams. We will use the Very High Speed Integrated Circuit (VHSIC) Hardware Description Language, or VHDL, for design entry in the laboratory exercises.

After the code is written, it is translated into a netlist, which is built from a set of macros (e.g., adders, multiplexors, and registers). This is called *synthesis*. This is followed by *translation*, a process similar to the linking of software object files, in which all instances of the device are resolved. The next step is to *map* all macro instances onto the target architecture, which consists of LUT's, IOB's, and registers. The design then undergoes a *place and route* process whereby all instances are assigned to physical locations on the silicon. This process is usually iterative, guided by the timing constraints imposed by the designer.

C. VHDL

This language, which was designed under the VHSIC program by the Department of Defense (DOD), is a language that can be used to design and simulate circuits. It was adopted by the IEEE as a standard as IEEE 1076-1987 in 1987 and is updated every five years, e.g., IEEE 1076-1993, etc. The libraries are covered by IEEE 1164. There are many reasons for using VHDL in circuit design. It is capable of describing more complex designs than can be described using schematics. It is not bound to any one vendor. It supports design abstraction and also allows for design reuse. It is a standard and the DOD requires it.

The VHDL design flow is shown in Fig. 3.

The Entity/Architecture pair is the basic building block of all VHDL designs. An entity may be associated with more than one architecture, but an architecture can be associated with only one entity.

The format for an entity file is given in Fig. 4. As an example, the entity file for a DFLOP is shown in Fig. 5. As you can see from the example, the **PORT** definitions are of the form (Port name : **MODE** type), where **MODE** type can be **in**, **out**, **inout**, or **buffer**.

The format for the architecture file is shown in Fig. 6. The file contains a declaration section where signals, constants, and components local to the architecture are declared followed by a set of concurrent statements by which the circuit is defined.

Concurrent statements are order independent. An example of concurrent statements is shown in Fig. 7 along with the circuit they define.

Concurrent statements are order independent. An example of this shown in Fig. 7. The circuit shown can be described equally well by the code to the left or the code to the right.

VHDL predefines the logic operators. The operator **NOT** takes precedence over the others, which are **AND**, **NAND**, **OR**, **NOR**, **XOR**, and **XNOR**. There is no implied precedence for these operators. If there are two or more of them in an equation, the order of precedence is from left to right. Note that **XNOR** was added to the standard in 1076-1993.

There is also a set of predefined relational operators: = Equals; /= Not equal; and, for establishing order, < Less than; <= Less than or equal to; > Greater than; and >= Greater than or equal to.

Comments may be included in the code and start with a double minus sign **--**. The text that follows on the same line is interpreted as a comment. Only single line comments are allowed, i.e., block comments are not permitted in VHDL.

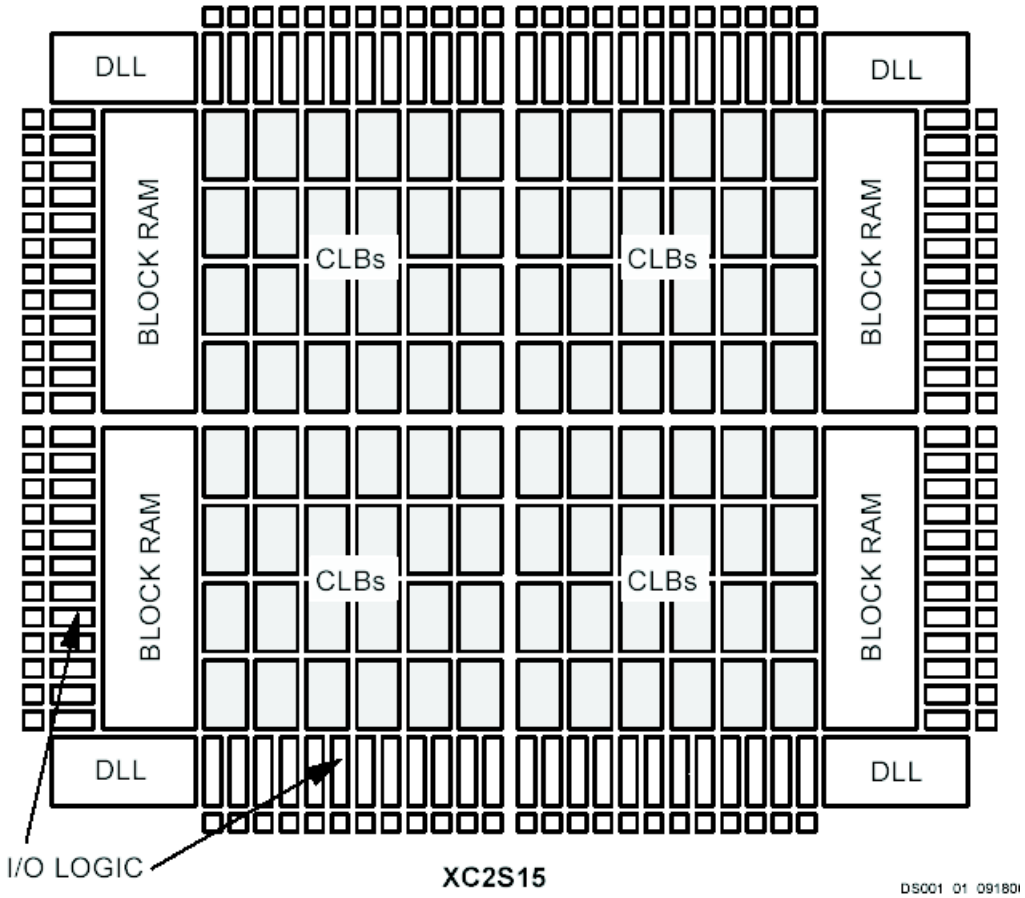


FIG. 2: The Xilinx SPARTAN II is an example of a typical FPGA layout .

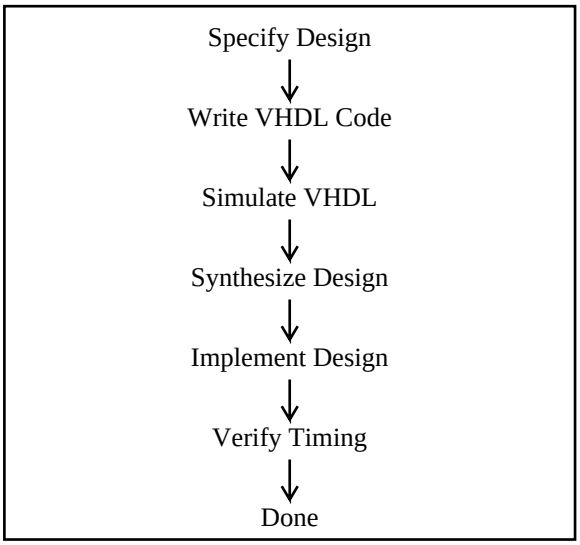


FIG. 3: VHDL Design Flow.

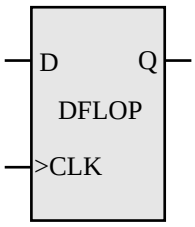
Processes also are defined within the architecture file. These have local variables and contain sequential statements. Processes have either a sensitivity list or a wait statement associated with them. For processes with a sensitivity list, execution begins **only** when a signal in the sensitivity list changes. Processes can be used to make **clocked** circuits. The format for process code is shown in Fig. 8. Keep in mind that a process must have a sensitivity list **or** a **wait** statement but can never have both. That is why they are listed as **optional** in the description.

```
entity entity_name is
   generic  (generic_list);
   port (port_list);
end entity_name;
```

FIG. 4: The entity file.

To pull this information together, the code for an Entity/Architecture pair to define a two input **AND** gate is shown as Fig. 9.

This completes this brief introduction to FPGA's. There are a number of references that you can consult for more in-depth information[8–12].



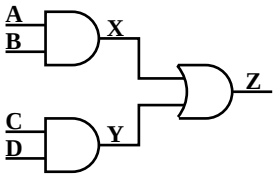
- - becomes - -

```
entity DFLOP is
Port  (D, clk     : in std_logic;
       Q          : out std_logic
       );
end DFLOP;
```

FIG. 5: Example of entity code for a DFLOP.

```
architecture

   architecture_name  of
   entity_name  is
   declarations

begin

   concurrent statements

end  architecture_name;
```

FIG. 6: The architecture file.




```
Z<=X or Y;                    X<=A and B;
Y<=C and D;   same as         Y<=C and D;
X<=A and B;                   Z<=X or Y;
```

FIG. 7: Example of concurrent statements within an architecture file. The circuit shown can be defined by either the code to the left or the code to the right of the figure.

```
Label: -- optional label
process  (optional sensitivity list)
-- local process declarations
begin
-- sequential statements
-- optional  wait  statements
end process;
```

FIG. 8: Format for process code.

```
library  IEEE;
use  IEEE.std_logic_1164.all;

entity  and2vhdl  is
  port(
     In_a      : in  std_logic;
     In_b      : in  std_logic;
     Out_c     : out std_logic
       );
end  and2vhdl;

architecture  and2vhdl_arch  of  and2vhdl  is
begin
   Out_c $<=$ In_a  and  In_b;
end  and2vhdl_arch;
```

FIG. 9: Example of an Entity/Architecture pair for a two input **AND** gate.

II. DESIGN OF A SIMPLE OPTICAL LINK FOR THE TRANSMISSION OF DATA

The second part of our course is an introduction to the design and construction of a simple optical link. Optical links will be used for sending data back and forth from the counting room to the detector in the data acquisition systems for future high energy physics experiments, including ATLAS and CMS in the LHC at CERN (Switzerland) and BTeV at Fermilab (USA). There are good reasons for using this method of data transmission. The ultra-high speed of optical links meets the very high bandwidth requirements of these experiments. Since the data can go out on fewer high speed lines, there is also a large reduction in the number and weight of cables needed. Another benefit is that optical links are relatively immune to electro-magnetic interference (EMI).

A basic optical link has three main components as shown in Fig. 10, each with a specific function. The

transmitter contains a light source, e. g., a light-emitting diode (LED), an edge-emitting laser diode (LD), or a vertical cavity surface-emitting laser diode (VCSEL), that converts an electrical current into an optical signal. The receiver contains a photodiode or a PIN photodiode that converts the light back into an electrical signal, an amplifier that makes the signal easier to detect, and a discriminator that is able to recognize if the bit received is a low or a high. The fiber-optic cable carries the optical signal between them. Fig. 11 shows how the signals flow through the link as they are converted from electrical to optical and then back to electrical by the devices in the link.

Both the transmitter and the receiver are devices for converting energy from one form to another. The transmitter is an electro-optic transducer, which converts an electrical signal to an optical signal. The receiver is an electro-optic device that converts the optical signals back into electrical signals. The semiconductor p-n junction is the basic structure used in electro-optic devices. When a positive voltage is applied across the p- and n-contacts (forward bias), electrons and holes are injected from the n and p doped materials into the active region of the device. In many III-V semiconductors, such as gallium arsenide, the electrons and holes recombine directly, emitting photons with energies roughly equal to the bandgap of the material.

There are several different kinds of electro-optic transducers that can be used as transmitters. One is the light-emitting diode (LED) shown in Fig. 12 from which light is randomly emitted when the carriers recombine. These spontaneous emissions are not strongly correlated; in fact, photon frequencies and propagation directions are randomly distributed. The average time to recombination is a few nanoseconds. This relatively long carrier lifetime limits the speed at which the light output by an LED can be modulated to a few hundred megabits per second and also the efficiency of the electro-optical conversion. Thus an LED is not a good choice for the transmitter in an ultra-high speed optical link.

The laser diode is another type of electro-optic transducer. The basic physics behind the operation of lasers can be understood in terms of three fundamental processes: absorption, spontaneous emission, and stimulated emission. Absorption occurs when an electromagnetic wave of energy $h\nu$ is incident on the active region of a semiconductor and creates an electron-hole pair by raising an electron from the valence to the conduction band. The energy of the incident photon must exceed the bandgap energy in order for this to occur. $h\nu \geq E_c - E_v$. (See Fig. 13.) An electron in the conduction band can recombine with a hole, i.e., return to the valence band releasing energy by emitting a photon of energy $h\nu = E_c - E_v$. This is the process of spontaneous emission, which occurs with lifetime, τ. This process is illustrated in Fig. 14. Recombination can also occur by stimulated emission when an electromagnetic wave of energy $h\nu = E_c - E_v$ is incident on the p-n junction as shown in Fig. 15. As for spontaneous emission, the energy of the photon emitted will be $h\nu = E_c - E_v$. But in this case the produced photon will be emitted in the same direction and with the same phase as the incident wave.

We can see from Fig. 16 that a plane electromagnetic wave traveling in a direction orthogonal to the mirrors will bounce back and forth between them and will be amplified on each passage through the active material. The mirror with partial reflectivity will allow a useful output beam to pass. It is important to realize that a certain threshold condition must be fulfilled. The oscillation will start only when the gain of the active material compensates the losses in the laser. Once the critical inversion is reached, i.e., once the number of electrons in the conduction band exceeds the number in the valence band, oscillation will build up from the stimulated emission[13].

There are several different kinds of lasers made from semiconductor material. In the Fabry-Perot edge-emitting laser, shown in Fig. 17 the reflecting mirror facets are formed at either end of the optical waveguide by carefully cleaving or etching the semiconductor along two parallel crystal planes.

In the Distributed Feedback (DFB) edge-emitting laser, developed in the early 80s, the reflections are distributed along the length of the waveguide by the creation of periodic index variations that individually reflect only a small fraction of the photons. DFB lasers have the advantage of a feedback mechanism that is far more sensitive to the wavelength of the light; as a result, the emitted light has a far narrower spectral linewidth than it does in a Fabry-Perot laser. Fig. 18 shows the construction of a DFB laser.

Like an edge-emitting laser, a Vertical Cavity Surface-Emitting Laser, or VCSEL, requires an active light-emitting region sandwiched between two mirrors. But, in this case, the laser light travels vertically through the device, and the mirrors are part of the epitaxial layer design. The length of the active region is four orders of magnitude shorter (typically 0.01-0.2m) than in a typical edge-emitting laser. While this limits the efficiency of individual photons to produce a second photon by stimulated emission on a single traversal, the very large number of highly reflective surfaces means that photons pass through the active region many times before they are emitted. The mirrors are Distributed Bragg Reflectors as above with each layer made from two layers with very different indices of refraction which makes them highly reflective. They are of a thickness to be quarter-wave plates, so that the reflected waves from all DBR surfaces add constructively. The structure of two typical VCSEL's is shown in Fig. 19.

There are several advantages to using VCSEL's rather than edge-emitting lasers for high speed data transmission in modern experiments. Because the light is emitted from the surface and is circular in shape the laser light can be easily coupled into optical fiber. This is in

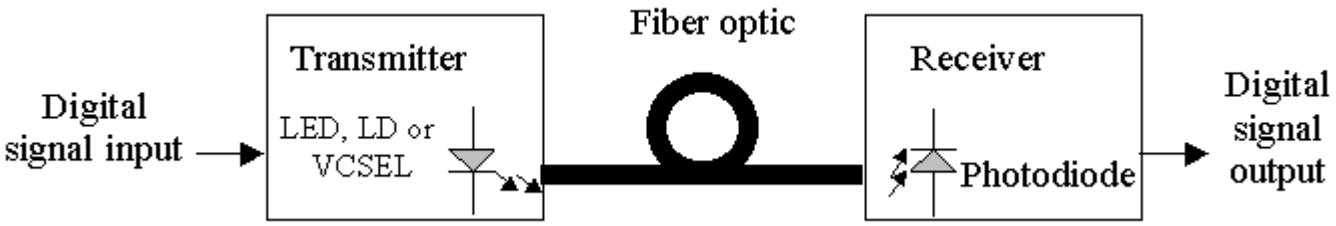


FIG. 10: Components of a Simple Optical Link.

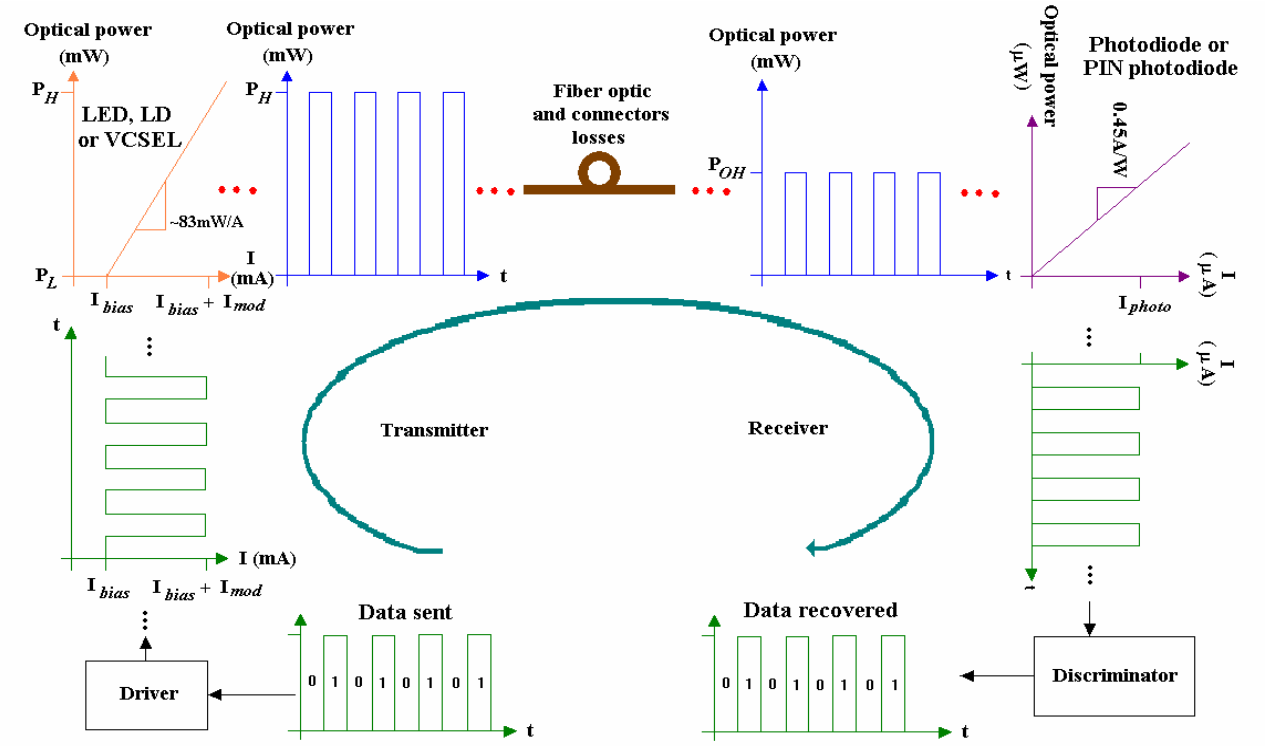


FIG. 11: Signal Flow through an Optical Link.

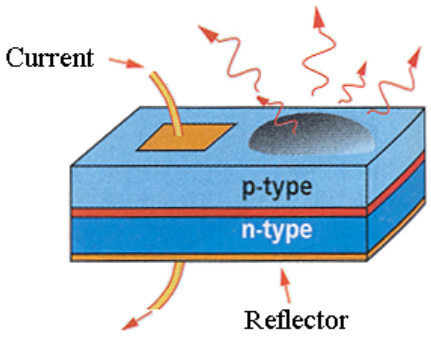


FIG. 12: Structure of an LED.

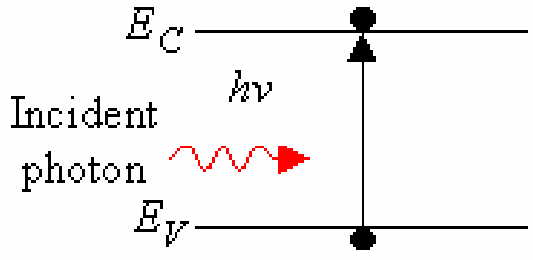


FIG. 13: The process of absorption.

contrast to the light pattern from edge-emitting lasers, which is elliptical and much wider in one dimension than the other. VCSEL's are also very efficient, i.e., consume very little power relative to the optical power they emit. They have the added advantage of low-cost wafer-scale fabrication and testing[14].

At each end of a fiber optic link is a device for converting energy from one form to another. At the receiver

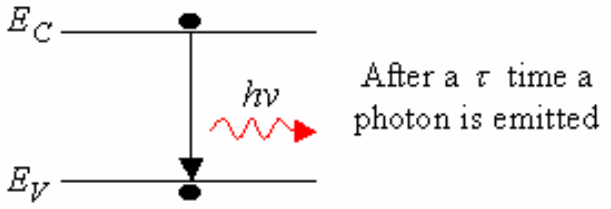


FIG. 14: Spontaneous emission of a photon by recombination of an electron-hole pair.

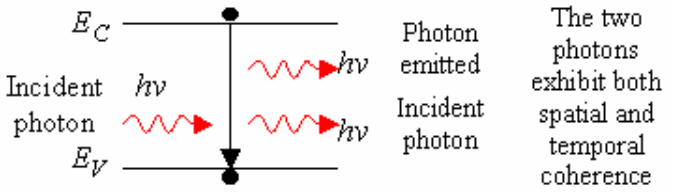


FIG. 15: Stimulated emission in which a second photon is produced in spatial and temporal coherence with the incident photon.

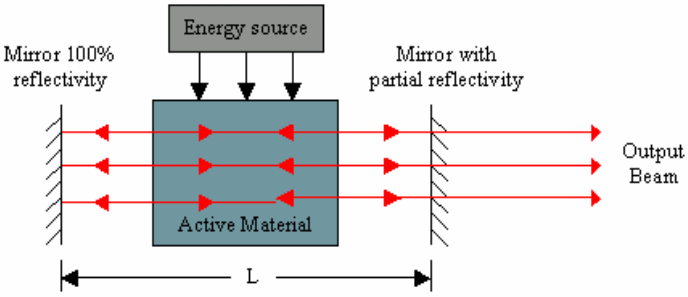


FIG. 16: The operation of a laser.

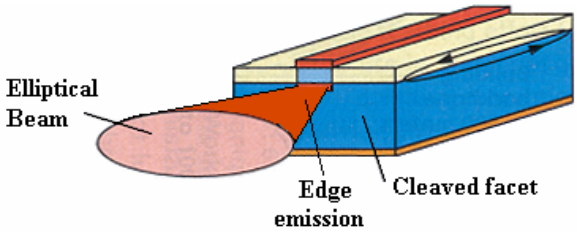


FIG. 17: Construction of a Fabry-Perot laser.

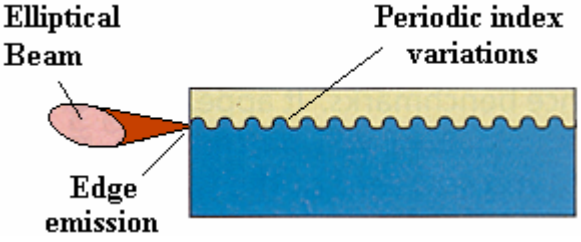


FIG. 18: Construction of a Distributed Feedback Laser.

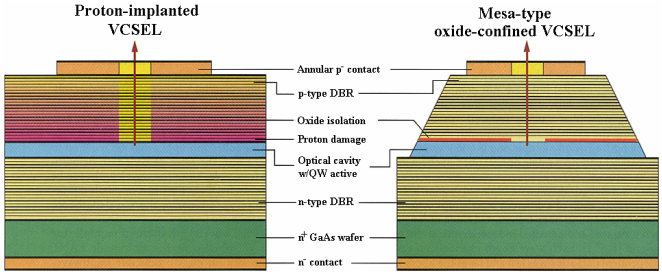


FIG. 19: Two typical Vertical Cavity Surface-Emitting Lasers.

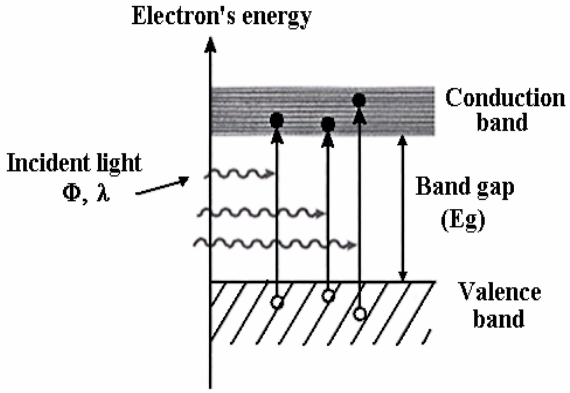


FIG. 20: A photoconductive detector.

end is a photoconductive detector, or photodiode, which converts optical energy back into electrical energy. The photodiode is the simplest of detectors and consists of a semiconductor p-n junction with a small enough band gap that the band gap energy is less than the energy of the photons to be detected. In this case the incident photons will be absorbed and produce electron-hole pairs as shown in Fig 20. Ideally the current that results should depend linearly on the optical power input as shown by the dashed curve in Fig. 21. The actual response is highly nonlinear as shown by the solid curve on the same figure for a real device made from silicon, which shows the responsivity, S, as a function of wavelength versus the optical power, P, input at that wavelength, $S(\lambda) = i_{FOTO)}/P(\lambda)$, where i_{FOTO} is the current.

To understand the interaction of photons with a p-n junction, we first show a p-n junction in the absence of illumination and without any external bias applied (Fig. 22). The majority carriers from both the n and p doped regions diffuse to the other side and recombine. This creates a region that is depleted of carriers, the so-called depletion region. The remaining ionized donors and acceptors form an electric field that counteracts the carrier diffusion. The only current that flows is the small current due to the electron-hole pairs that are generated thermally, which are collected by this electric field. This is known as the *dark* current.

Fig. 23 shows what happens when the p-n junction is il-

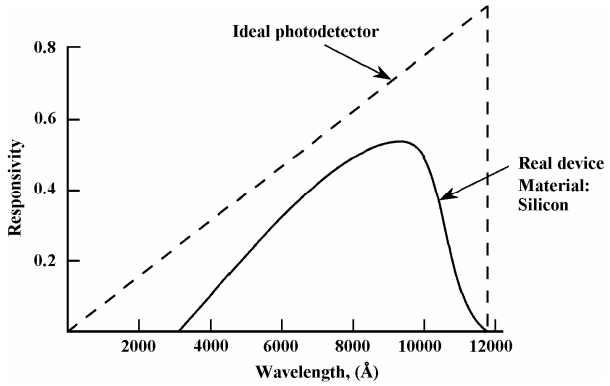


FIG. 21: Responsivity versus wavelength of the incident optical signal for an ideal (dashed curve) and a real photodetector (solid curve).

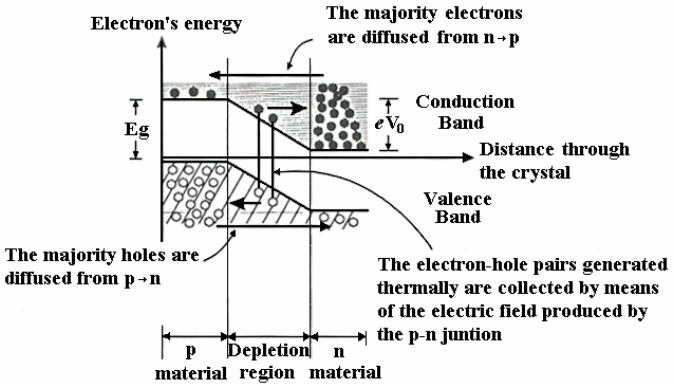


FIG. 22: A photodiode without illumination and with no bias applied.

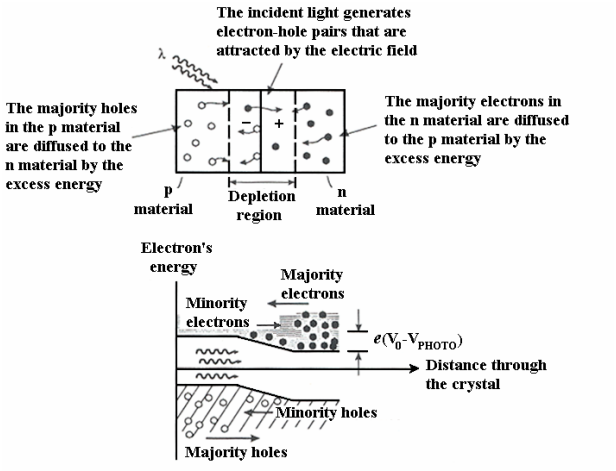


FIG. 23: A photodiode with illumination but with no external bias applied.

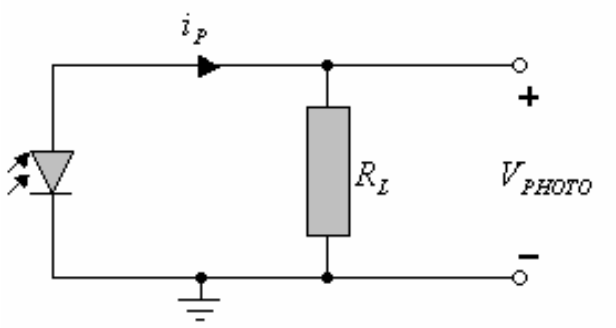


FIG. 24: Circuit for using the photodetector in photovoltaic mode.

luminated. The incident photon energy creates electron-hole pairs, which are collected by the fixed ions that produce the electric field in the gap. This reduces the field in the gap and enables more of the majority carriers in the n and p regions to diffuse to the other regions. When the illumination stops, the junction returns to the state shown in Fig. 22.

The electron-hole pairs that are created by the incident photons cause an electrical current to flow in the device even in the absence of an applied field because of the electric field produced by the junction itself. When operated in this way, the photodiode is said to be operating in photovoltaic mode. Fig. 24 shows a simple circuit for operating the photodiode in photovoltaic mode.

The response depends on the value of the load resistance (R_L). If $R_L = \infty$ (open circuit), then the photovoltaic response is logarithmic:

$$V_{photo} = C\ ln\left(\frac{SP_o}{i_o}\right),$$

where C is a constant, P_o is the optical power of the light impinging on the detector, S is the photodiode sensitivity, and i_o is the dark current. If, however, $R_L \leq 1K\Omega$, the response is linear:

$$V_{photo} = i_p R_L = (SP_o)R_L.$$

Since the carriers are collected by means of the electric field in the depletion region, the time response is usually slow and this means that photodiodes operated in this mode can not be used in high frequency applications.

The photodiode can also be operated in photoconductive mode as shown in Fig. 25. In this mode the photodiode is reverse-biased. Under this condition the electrons are attracted from the depletion region into the n material, and the holes are attracted from the depletion region into the p material. This means that more fixed ions of both kinds are present in the depletion region. The depletion region grows wider and the energy barrier increases as a function of the reverse voltage applied on the photodiode. The flux of the majority carriers of either kind is stopped. Thus, the only current that will be able to flow in the absence of illumination in the photodiode is the inverse current, i.e., the *dark* current. When the junction is illuminated, creating electron hole pairs, a current will flow as shown in the figure. The photocurrent can be converted to a voltage using a transimpedance amplifier as shown in Fig. 26.

A PIN photodiode takes its name from its structure, which is shown in Fig. 27. We can see from the figure

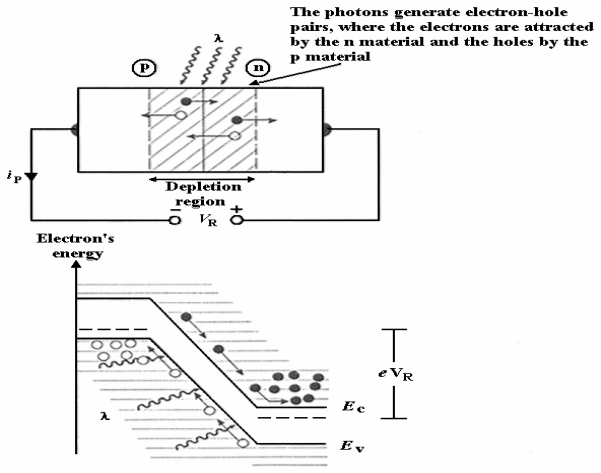


FIG. 25: A photodiode operated in photoconductive mode.

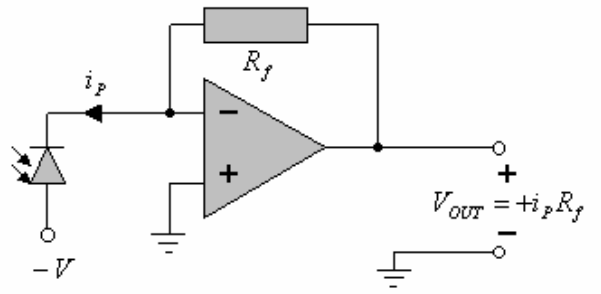


FIG. 26: Circuit for using the photodetector in photoconductive mode.

that the only difference (which is a **big** difference) between a PIN photodiode and a simple photodiode is that the PIN photodiode includes an intrinsic semiconductor between the p+ and n+ materials. This means that the depletion region (W) is wider than in a simple photodiode. The dynamic capacitance of this device is smaller than in a simple photodiode, which means that it gives a faster response. This is important when we want high bandwidth.

To take the optical signal from the output of the transmitter to the input of the receiver, we use an optical fiber. The main principle behind operation of an optical fiber is total internal reflection, as shown in Fig. 28. The maximum angle at which the light can enter and still be totally internally reflected, the *numerical aperture*, is:

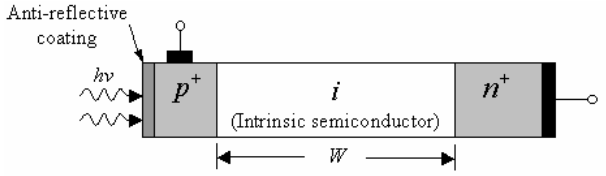


FIG. 27: Structure of a PIN photodiode.

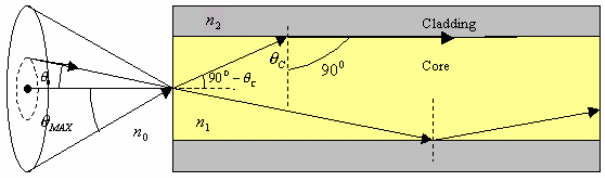


FIG. 28: Optical signal entering an optical fiber.

$$A_N = sin\ \Theta_{max} = \sqrt{n_1^2 - n_2^2}.$$

Fiber is basically classified into three groups: Glass (silica) which includes singlemode step index fibers, multimode graded index fibers, and multimode step index fibers; Plastic clad silica (PSC) fibers; and Plastic fibers. A table of the properties of the various types of fibers is shown in Fig. 29.

Fig. 30 shows the absorption versus wavelength for glass multimode optical fiber. The wavelengths at which there is good light transmission are pointed out on the figure.

In summary, we have come to the following conclusions regarding the design of a basic optical link. The VCSEL is the best option for the transmitter in an optical link because of its low power consumption, the fact that it can be coupled to optical fiber with high efficiency, and the ease of its manufacture. For the receiver, we recommend a PIN photodiode, which can be operated in photovoltaic mode at high and ultra-high frequencies. In this case, the relatively large dark current and the noise produced by a power supply used to do the biasing can be avoided. Also, multimode glass optical fiber is good enough to transmit at high and ultra-high frequencies over a few hundreds of meters.

Acknowledgments

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	Glass (silica) optical fibers						Plastic clad optical fibers	Plastic optical fibers
Core material	**Glass**						**Glass**	**Plastic**
Cladding material	**Glass**						**Plastic**	**Plastic**
Core diameter (μm)	8	200-1000	50	62.5	85	100	200-600	1000-3000
Cladding diameter (μm)	125	1035	125	125	125	140	1000	3000
Refractive index profile	Step	Step	Graded	Graded	Graded	Graded	Step	Step
Transmission mode	Single	Multi	Multi	Multi	Multi	Multi	Multi	Multi
Numerical aperture (NA)	0.11	---	0.2	0.29	0.26	0.3	---	---
Attenuation 660nm	---	---	---	---	---	---	6-10	150-250
(dB/km) 850nm	---	5-20	3	4	5	6	6-10	150-250
1300nm	0.5	---	1.75	2	4	5	---	---
1550nm	0.3	---	---	---	---	---	---	---
Bandwidth 660nm	---	10	---	---	---	---	25	0.3
(MHzkm) 850nm	---	10	600	230	200	100	25	---
1300nm	---	---	750	500	300	300	---	---
Common wavelength transmitted (nm)	1300 1550	660-1060	850 1300	850 1300	850 1300	850 1300	660-1060	660
Common source used to transmit	Laser	LED Laser	LED Laser	LED Laser	LED Laser	LED Laser	LED	LED

FIG. 29: Table of properties of the various types of optical fiber.

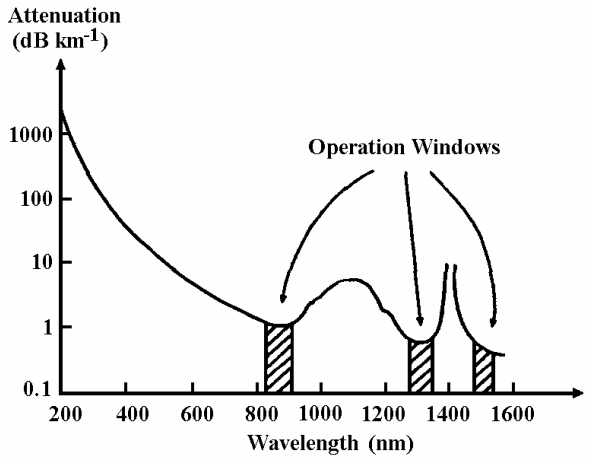

FIG. 30: Attenuation versus wavelength in glass multimode fiber.

[1] For information about the Quicklogic products available, including these, see www.quicklogic.com.
[2] See www.actel.com.
[3] See www.altera.com.
[4] See www.atmel.com.
[5] See www.cypress.com.
[6] See www.lucent.com.
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