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Digital LLRF controller for SSRF booster RF system upgrade*

ZHANG Zhi-Gang (张志刚),[1,2,3] ZHAO Yu-Bin (赵玉彬),[1,3] XU Kai (徐凯),[1,3]
ZHENG Xiang (郑湘),[1,3] LI Zheng (李正),[1,3] ZHAO Shen-Jie (赵申杰),[1,3] CHANG Qiang (常强),[1,3]
HOU Hong-Tao (侯洪涛),[1,3] MA Zhen-Yu (马震宇),[1,3] LUO Chen (罗琛),[1,3]
MAO Dong-Qing (毛冬青),[1,3] SHI Jing (是晶),[1,3] WANG Yan (王岩),[1,3] and LIU Jian-Fei (刘建飞)[1,3,†]

[1]*Shanghai Institute of Applied Physics, Chinese Academy of Sciences, Shanghai 201800, China*
[2]*University of Chinese Academy of Sciences, Beijing 100049, China*
[3]*Shanghai Key Laboratory of Cryogenics & Superconducting RF Technology, Shanghai, China*
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The low level radio frequency (LLRF) system for booster accelerator at Shanghai Synchrotron Radiation Facility (SSRF) was upgraded by a digital controller based on field programmable gate array (FPGA) technology. Parameters of voltage, frequency and field flatness in the two 5-cell cavities are controlled to meet the requirements of booster. In this article, the ramping curve of cavity voltage, amplitude and phase control loop with vector sum of the two 5-cell cavities, tuning loop and field flatness loop are analyzed and discussed in detail. A different method in tuning loop is adopted due to the limitations of ADC channels. The function realizes energy ramping of electron beam from 150 MeV to 3.5 GeV with a repetition rate of 2 Hz. With the new LLRF controller, the phase stability at ramping mode in 10 hours long operation is improved from $\pm 1.5^\circ$ (RMS) with open loop to $\pm 0.15^\circ$ (RMS) with close loop, while the detuning phase and field flatness are maintained to within $\pm 2^\circ$ and $\pm 1\%$, respectively.

Keywords: LLRF control, Ramping, Amplitude and phase loop, Field flatness, Tuning loops

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I. INTRODUCTION

The Shanghai Synchrotron Radiation Facility (SSRF) can be divided into two parts: a high efficiency injector and a high performance storage ring. The injector includes a 150 MeV electron linac, a full energy booster synchrotron, a linac-to-booster transport line (LTB) and a transport line from booster to storage ring (BTS) [1]. The energy of electron beam is ramped from 150 MeV to 3.5 GeV with a repetition rate of 2 Hz in the booster.

Stability of the amplitude and phase in the accelerators is controlled by low level radio frequency (LLRF) system. Analogue LLRF has been adopted in the booster of most light sources, such as SSRF [2], ALBL [3] and Diamond [4]. With the rapid development of digital technology, digital LLRF is widely used so as to have a better performance of the beam storage, such as the ALBL [5], SSRF [6], and SOLEIL [7].

The former LLRF controller of SSRF booster is an analogy one with the two 5-cell copper cavities. The problems encountered in its seven years' operation included: occasional stop of ramping to affect the top-up mode in operation, motor driver errors from frequent movements and undesirable beam performance of the booster with closed amplitude and phase loop. In addition, it is not convenient to replace hardware or to update software of peripheral component interconnect (PCI) extensions for instrumentation (PXI) boards in maintenance, and it costs a lot to have a spare set of the front end in analogy LLRF system. To improve the performance, the booster LLRF controller was upgraded in 2014 with the digital technology.

As shown in Fig. 1, the RF system of SSRF booster is composed of a 40 W pre-amplifier, a 180 kW continuous-wave plant (Klystron) with WR1800 waveguide lines, Magic T, two PETRA type 5-cell copper cavities and a LLRF controller [2].

The up-converter, down-converter, in-phase and quadrature (I/Q) demodulator [8, 9] and feedback control technology are adopted in the digital LLRF controller for SSRF booster. There are five loops to stabilize the two 5-cell cavities operation: an amplitude and phase loop with the vector sum of two cavities, a tuning loop and a field flatness loop for each cavity, which will be described together with the amplitude ramping curve.

Table 1 presents the performance of the new developed LLRF controller which achieves the requirements of SSRF booster RF system, where the data are measured since August, 2014 on-line operation with beam.

TABLE 1. Performance of SSRF booster RF system with new LLRF controller

Parameter	Value
Nominal RF frequency (MHz)	499.654
Repetition(ramping) (Hz)	2
the max of RF voltage (MV)	1.8
Phase control range ($^\circ$)	± 180
Phase stability during ramping[a] ($^\circ$)	± 2
Field flatness (%)	± 1

[a] Estimated for two cavities driven by on klystron

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† Corresponding author, liujianfei@sinap.ac.cn

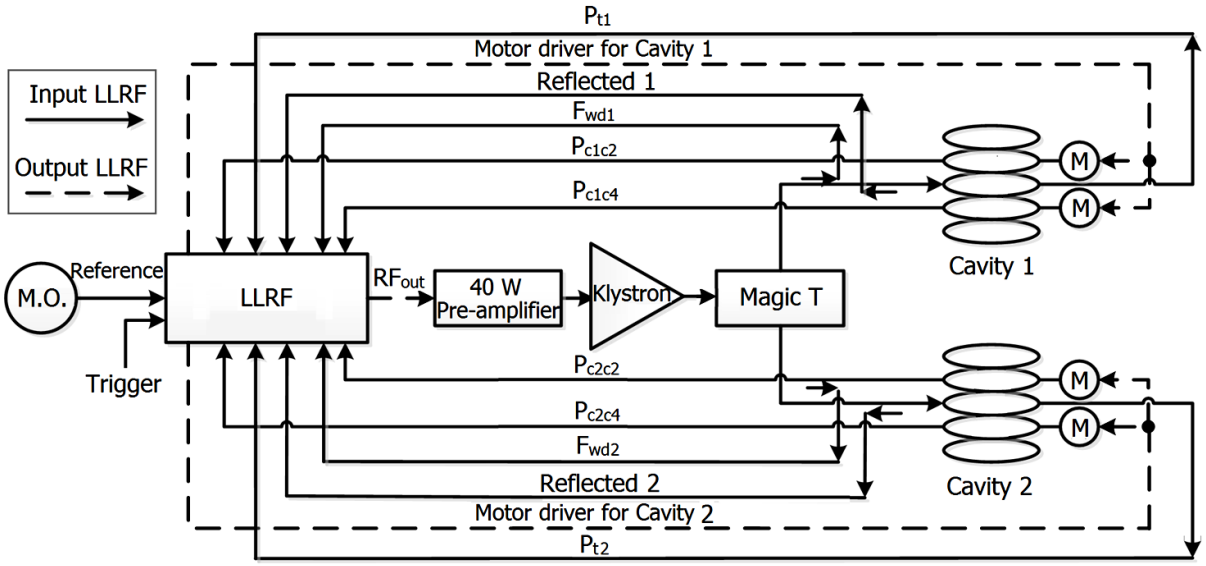

Fig. 1. Layout of the RF system of SSRF booster. The RF signals sampled and processed by the LLRF controller include the reference signal, forward power signal F_{wdi}, reflected power signal Reflected i, pick-up signals from P_{cic2}, P_{ti} and P_{cic4} (i denotes cavity number of the 5-cell copper cavities). M.O., master oscillator; Trigger, the timing with a repetition rate of 2 Hz.

II. DESIGN OF THE DIGITAL LLRF CONTROLLER

A. Ramping curve

The energy of electron beam in booster increases with the RF cavity voltage in the first 250 ms of a period. The RF cavity voltage is ramped to compensate the momentum variation due to the magnets ramping and the energy loss due to radiation, the latter becoming predominant at higher energies. The RF voltage is given by Eq. (1) [10]

$$V_{\rm RF}(t) = V_0 + K_1 {\rm d}B/{\rm d}t + K_2[E(t)]^4, \qquad (1)$$

where, V_0 is the capture voltage, B is the magnetic flux density of dipole, K_1 is proportional to the maximum energy variation, and K_2 is a coefficient related to the radiation losses and the condition on the quantum lifetime.

It is required that during the injection, the starting RF voltage of ramping should be considered reasonably to avoid strong longitudinal oscillation, which causes beam loss of injection. The results, calculated with the SSRF design parameters of energy and arrival time jitter of the electron beam from the linac, show that there is no beam loss if the starting RF voltage is below 600 kV at the booster; but if the starting RF voltage was less than 200 kV, Robinson instability would occur during injection because of the large impedance of the two 5-cell cavities, especially in multi-bunch mode operation [2]. The cavity voltage ramping curve adopted in the digital LLRF controller is shown in Fig. 2. The starting voltage at the injection time is optimized at 400 kV holding 0.04 s, before it ramps linearly to 1.8 MV in 0.18 s. At 1.8 MV it stays for 0.04 s, before extraction of 0.25 s after injection.

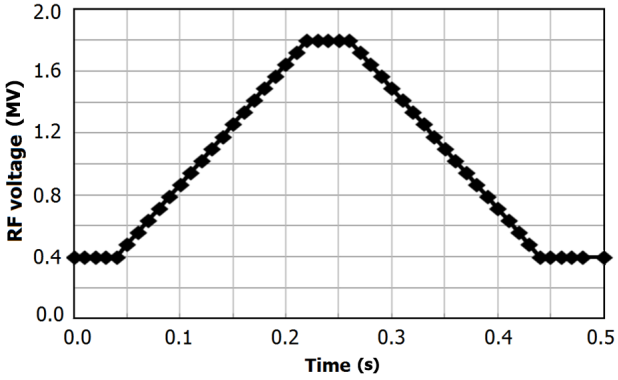

Fig. 2. Ramping curve of RF voltage of the digital LLRF at SSRF booster.

B. Amplitude and phase loop with vector sum of the two cavities

The amplitude and phase control loop, using a feedback method, is shown schematically in Fig. 3. With the ramping curve in Fig. 2, totally 50 sets of points are designed through the operation interface, which are amplitude of the vector sum of the two 5-cell cavities. By calculating with corresponding phase, 100 values including 50 I-data and 50 Q-data are obtained. The 100 values are downloaded to the 100 specified registers in FPGA through network, when the digital LLRF controller just reboot. The algorithms of the vector of signals, CORDIC (Coordinate Rotation Digital Computer) [11, 12], rotation, and PI are used.

The 5-cell cavity can be regarded as five magnetically coupled resonators. Due to the π accelerating mode, the whole

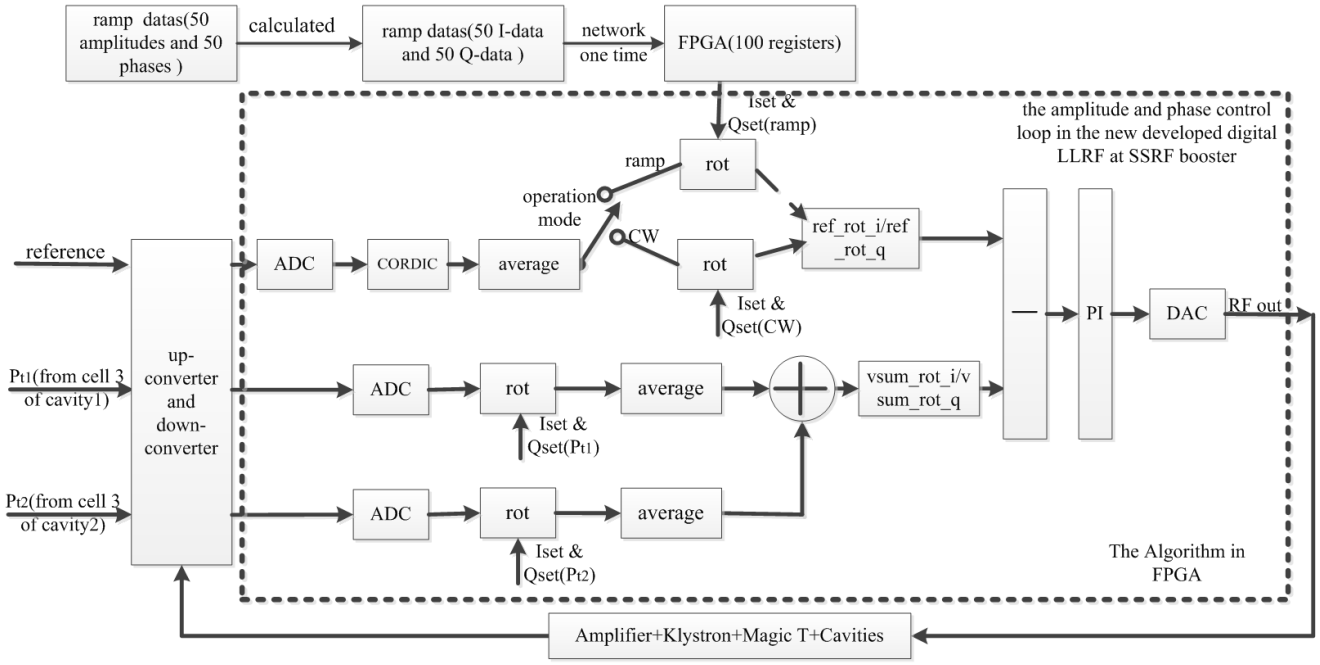

Fig. 3. Diagram of the amplitude and phase control loop in the digital LLRF of SSRF booster. CORDIC: coordinate rotation digital computer, Rot.: rotation by matrix, P.I.: proportional and integral.

5-cell cavity can be modeled as a single RLC parallel circuit [13] with the following transfer function [14]

$$G(s) = \frac{2\sigma R s}{s^2 + 2\sigma s + \omega_R^2}, \qquad \omega_R = \frac{1}{\sqrt{LC}}, \quad \sigma = \frac{\omega_R}{2Q}, \quad Q = R\sqrt{\frac{C}{L}}, \tag{2}$$

where s is Laplacian, ω_R is the resonant frequency, σ is the damping rate (s^{-1}), and Q is the quality factor. Equation (2) can be simplified to a classical first-order low-pass filter when the cavity is centered at the resonance frequency [6, 14]

$$G(s) = \frac{\sigma R}{s + \sigma}. \tag{3}$$

The transfer function of the cavity model with feedback is shown in Fig. 4, where k_p is the gain value of the proportional and k_i is the integral in PI algorithm. The feedback model can absorb the forward delay (τ_f) and reverse delay (τ_p), which limits the gain loop.

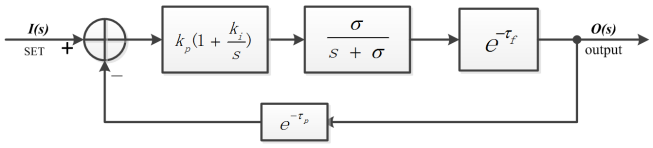

Fig. 4. The feedback model of the transfer function.

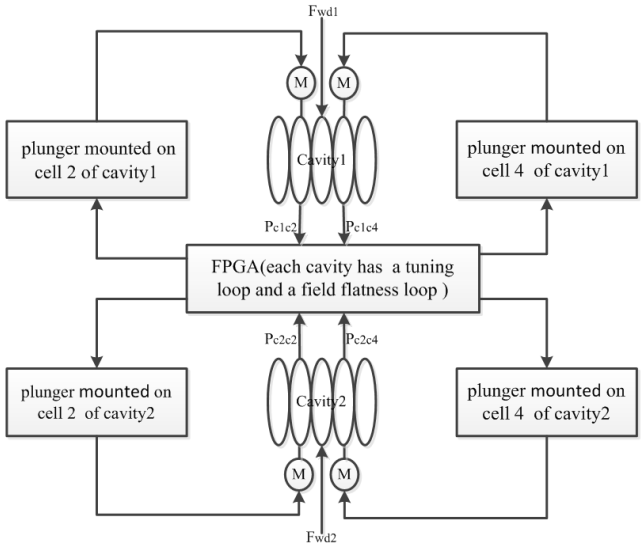

Fig. 5. Diagram of the tuning loops and field flatness loops at SSRF booster.

C. Tuning loop and field flatness loop

The tuning loop and field flatness loop of the digital LLRF controller is shown schematically in Fig. 5. Each cavity has a tuning loop and a field flatness loop. Tuning loop controls the resonance frequency of the 5-cell cavity, while the field flatness loop is for the 5-cell cavity to equalize the amplitude of the electric field in all the cells [15, 16].

With the tuning loop, two plungers mounted on Cells 2 and

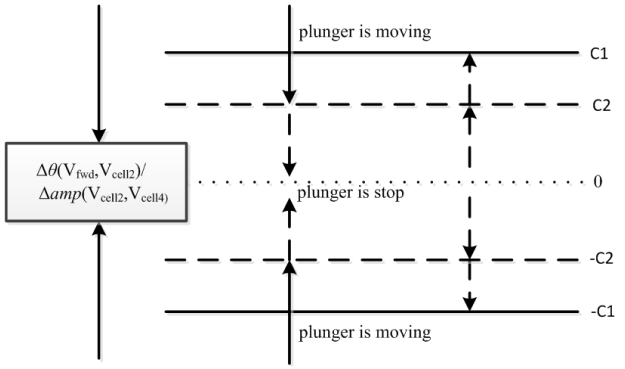

Fig. 6. Tuning thresholds and status of plunger. Solid arrow: the plunger moves; dotted arrow the plunger stops.

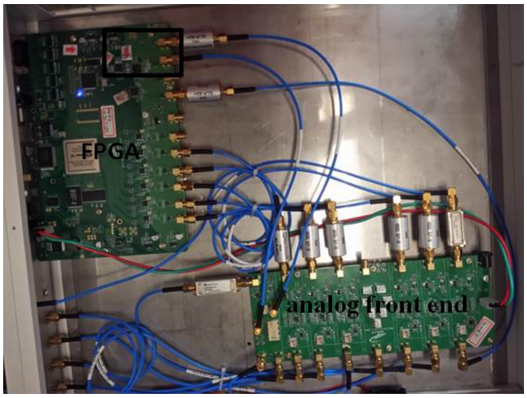

Fig. 7. (Color online) Chart of the digital LLRF controller box.

4 of the 5-cell cavity are driven in the same direction, the phase difference between the forward power and cavity voltage should remain as close as possible to the value of reference phase, which is chosen as having the minimum reflected power from the cavity and providing stable Robinson operation. Regarding to the field flatness loop, the two plungers of a cavity are driven in opposite directions, and the voltage difference between the Cells 2 and 4 should remain as small as possible.

The tuning loop and field flatness loop in the digital LLRF are also based on digital IQ technology. The FPGA board has six ADCs. Six RF signals (F_{wd1}, P_{c1c2}, P_{c1c4}, F_{wd2}, P_{c2c2} and P_{c2c4} in Fig. 1) are sampled by the LLRF controller. The phase difference between the voltages of forward and Cell 2 in a cavity is calculated using Eq. (4), and the normalized

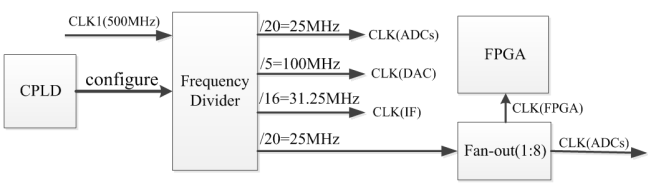

Fig. 8. The clock distribution system.

amplitude difference between the signals of Cells 2 and 4 in a cavity is obtained by Eq. (5):

$$\Delta\theta(V_{\rm fwd},V_{\rm cell2}) = \arctan 2(I_{\rm fwd},Q_{\rm fwd}) - \arctan 2(I_{\rm cell2},Q_{\rm cell2}), \tag{4}$$

$$\Delta amp(V_{\rm cell2},V_{\rm cell4}) = \frac{\sqrt{I^2_{\rm cell2}+Q^2_{\rm cell2}}-\sqrt{I^2_{\rm cell4}+Q^2_{\rm cell4}}}{\sqrt{I^2_{\rm cell2}+Q^2_{\rm cell2}}}. \tag{5}$$

According to the $\Delta\theta(V_{\rm fwd},V_{\rm cell2})$ and $\Delta amp(V_{\rm cell2},V_{\rm cell4})$ values for a cavity, three signals of enable, direction and pulse are sent to each motor driver from FPGA. The drivers move the two plungers (for a cavity) in right direction independently, making the $\Delta\theta(V_{\rm fwd},V_{\rm cell2})$ be as close as possible to reference value and the $\Delta amp(V_{\rm cell2},V_{\rm cell4})$ as close as possible to zero. This is done by defining two windows with thresholds of $\pm$C1 and $\pm$C2(C2 resides within C1). C1 defines acceptable range of the parameter, and C2 ($-$C2) defines the range the parameter shall be reduced to when it exceeds the C1 ($-$C1) thresholds. This is illustrated in Fig. 6 for tuning thresholds and the status of plunger.

D. Hardware

As mentioned above, there are eleven signals should be controlled and monitored (Fig. 1). Because of the lack of ADC channels on the digital signal processing board, the digital LLRF controller system was divided into two controllers, the amplitude and phase loop controller, and the frequency and field flatness loop controller.

Two different control cards are used in the updated LLRF controller 7. One is the RF front-end card, the other is the data processing card. The former is in charge of the local oscillator (LO) signal, the down-converter and the up-converter. The latter is integrated with the ADCs, the DACs, the I/O connectors and the clock distribution part. The gain value of the down-converter is greater than 10 dB, while the up-converter is greater than 12 dB. The isolation value of all channels is more than 80 dB.

As shown in Fig. 8, three different types of chips, such as the complex programmable logic device (CPLD), the frequency divider and the fan-out chip ($1:8$), are used in the clock distribution system. The CPLD is used to save the configuration program for frequency divider where the configuration program can be downloaded automatically when the power is switched on. The frequency divider is the main chip to generate various different frequency clock signals (i.e. the ADCs signal (25 MHz), the DAC signal (100 MHz), the FPGA signal (25 MHz), and the intermediate frequency (IF) signal (31.25 MHz)) by dividing the reference signal. And the fan-out chip can output eight clock signals for FPGA and ADCs from one input signal with the same frequency .

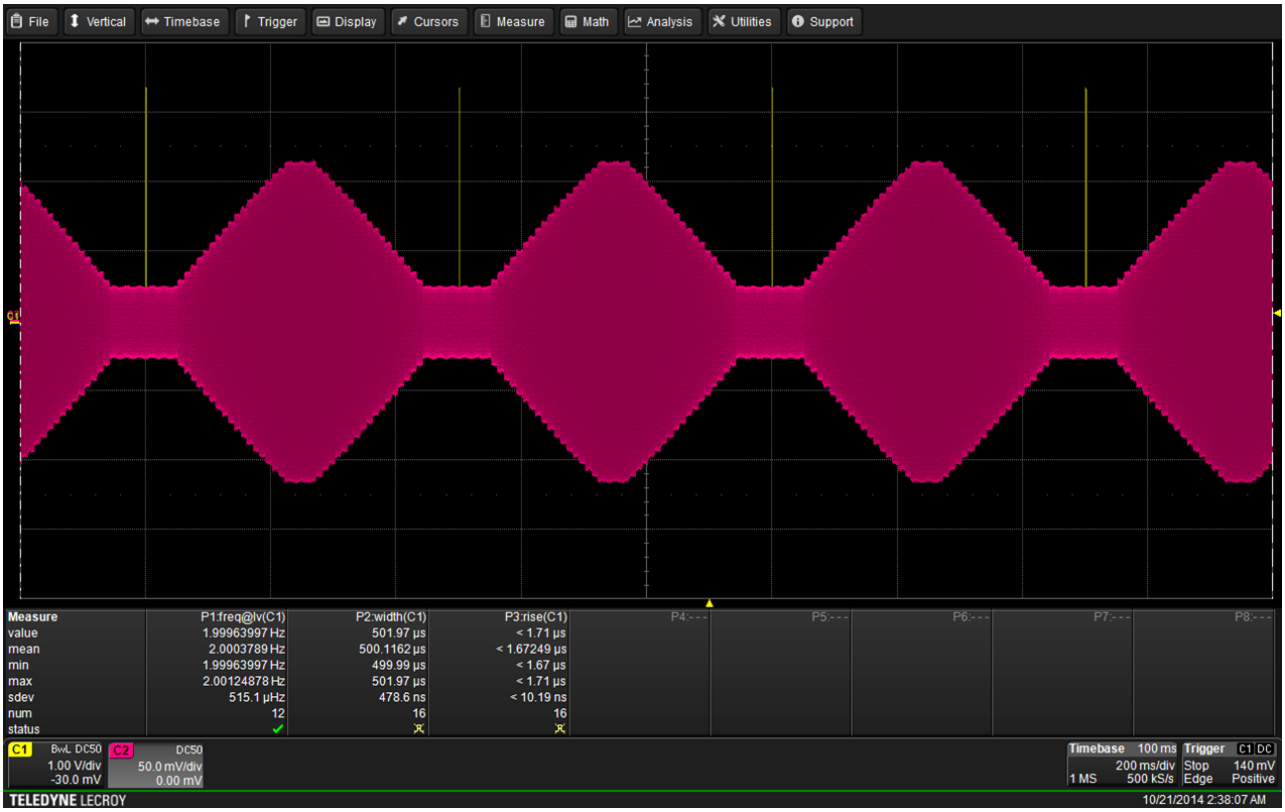

Fig. 9. (Color online) The RF output form DAC and the trigger traced by oscilloscope. C1: the trigger, C2: RF output.

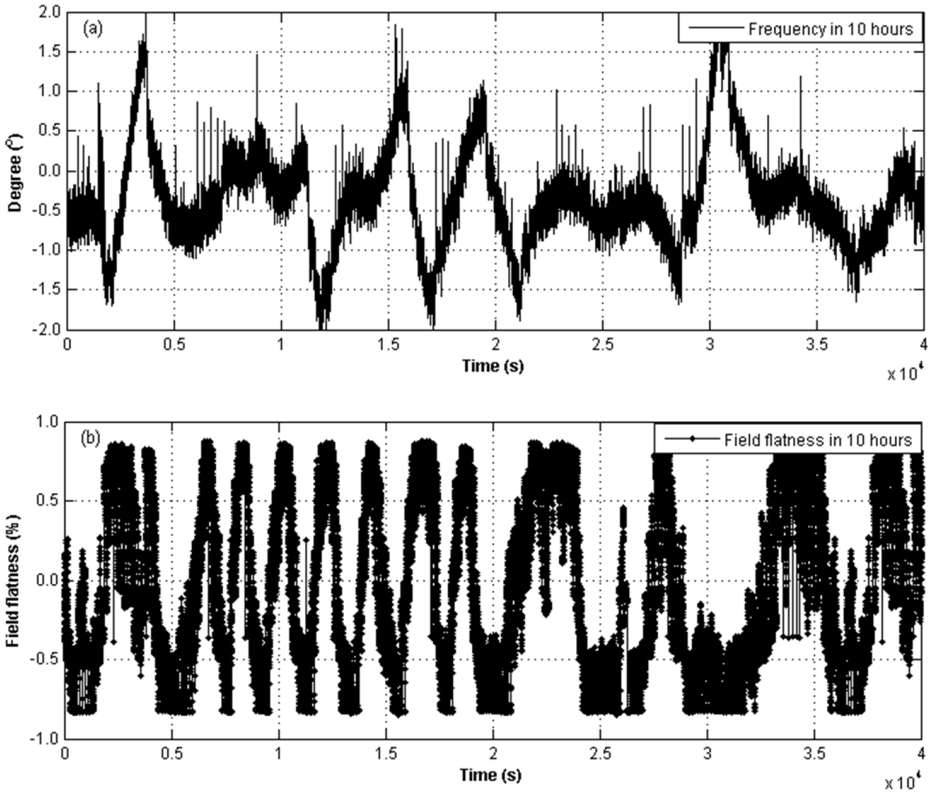

Fig. 10. Stability of the frequency (a) and field flatness (b) at ramping mode. The data were recorded every second in ten hours.

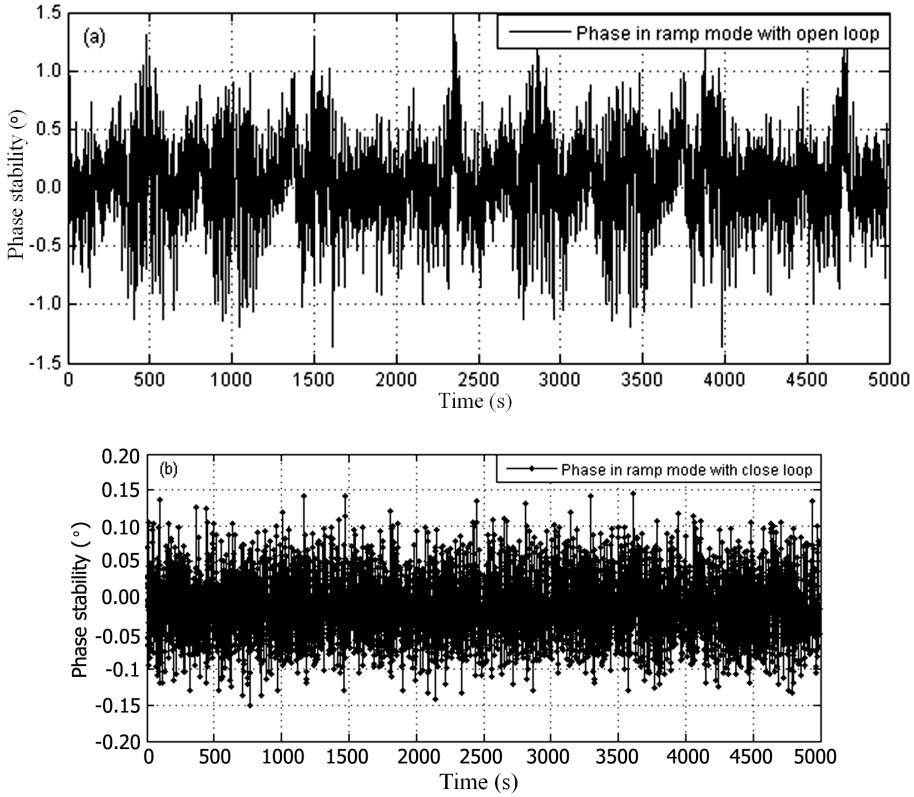

Fig. 11. The phase stability at ramping mode with open (a) and closed (b) loop in ten hours.

III. RESULTS AND DISCUSSION

The digital LLRF controller was put into operation with beam at SSRF booster RF system in August 2014 at ramping mode. The maximum reflected power is less than 300 W for each cavity. Two signals are traced by oscilloscope (Fig. 9). C1 indicates the trigger from timing, which is 2 Hz in repetition rate. C2 is the RF output from DAC, which is the input signal of 40 W pre-amplifier. In full energy operation, the power is ramping from 3 kW to 60 kW, corresponding to 0.4–1.8 MV across the sum of two 5-cell cavities.

Stability of the frequency and field flatness at ramping mode in ten hours are shown in Fig. 10. The frequency stability (Fig. 10(a)) is better than $\pm 2°$and the field flatness stability (Fig. 10(b)) is better than $\pm 1\%$.

Stability of the vector sum of phase at ramping mode with open and closed loop in ten hours is shown in Fig. 11, where we can see the stability is improved from $\pm 1.5°$ with open loop (Fig. 11(a)) to better than $\pm 0.15°$ (RMS) with closed loop (Fig. 11(b)) which is better than requirements of booster RF system ($\leq \pm 4°$). And there is no beam loss with closed loop which means the problem from old analogue LLRF controller has been solved.

IV. CONCLUSION

A new digital LLRF controller based on FPGA technology has been developed to replace the old analogue controller. The function to ramp the electrons energy from 150 MeV to 3.5 GeV with 2 Hz repetition rate is realized. Long time online operation with beam at SSRF booster under the new controller shows the stability of frequency, field flatness and phase is better than $\pm 2°$, $\pm 1\%$ and $\pm 0.15°$, respectively. Furthermore, the beam loss when control loop is closed with the old analogue controller has been solved. In general, the performances of the digital LLRF controller have reached the requirements for the SSRF booster RF system.

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