FRONT END ELECTRONICS DEVELOPMENT FOR SSC DETECTORS

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1 Introduction

1.1 The Challenges

The electronics for signal detection, event selection, and data recording for an SSC detector will be one of the most sophisticated electronics systems ever built. Signal processing must be performed on an astonishing 10^{12} analog signals per second. While the required performance and characteristics of an individual "channel" of electronics, i.e., the electronics for the readout of one detecting element, are very similar to some of the systems utilized today, the very large number of detectors, the high interaction rate, and the environment pose a number of severe challenges. Foremost among these are:

1. *Density and Power Dissipation*—For some of the detector systems very large reductions in the area and power will be required. For example, if wire drift chambers are to be utilized effectively the power dissipation per channel must be reduced by about a factor of 100, from the approximately 1 Watt per channel in existing systems to approximately 10 mW. The speed of silicon microstrip readout systems, which are already implemented with integrated circuit techniques, must be increased approximately ten-fold with little increase in power.

2. *Radiation Hardness*—A number of the electronics systems must be radiation hard. For example, the readout of silicon strips or wire chambers must operate without significant degradation to doses of 10^6 rads and $> 10^{14}$ n/cm^2. Preamplifiers, which are located inside liquid ionization calorimeters to enable optimum readout speed, must be resistant to nearly 10^7 rads.

3. *Level 1 Buffering*—Because of the very high interaction rate and the minimum time required to generate an effective first level of event selection (Level 1 trigger), data must be stored on the front end for 0.5–2 μseconds.

4. *Level 2 Buffering*—To reduce the rate at which data must be moved off the detector from $>$ 50 Gigabytes/sec to $<$ 0.5 Gigabytes/sec, it is useful to include a second level of data buffering on the front end chips. Only the information associated with events passing the second level of event selection (Level 2 trigger) needs to be readout.

5. *Noise Immunity and Crosstalk*—The likely requirement of simultaneous analog and digital activity during the data collection process implies great care must be taken to minimize the generation of noise by the readout system and to minimize the sensitivity of the input to external noise sources.

6. *Fault Analysis and Reliability*—The size, complexity, and relative inaccessibility of the electronics imply that high standards for fault analysis and reliability must be imposed if installation time and "down-time" is to be kept to a minimum.

Significant progress has been made during the last two years by groups working (largely independently) on front end systems for liquid ionization calorimeters, wire drift chambers (both drift time and pad readout), and silicon strip and pixel detectors. Much of this work has been funded under the SSC Generic R&D program and it will continue at least through 1990. However, because of the large number of difficult problems that need to be solved, a number of which are system level problems that are not currently being systematically addressed, a significantly broader, more coordinated effort on front end electronics systems is required in addition.

1.2 Scope of the Proposal

We propose to establish a comprehensive R&D effort on the front end electronics for SSC detectors. The scope of the proposal includes:

1. *Front End Circuits*—Detailed design and prototyping of the front end circuits for

   (a) liquid ionization calorimeters

(b) wire chamber drift time measurement

(c) pad readout of wire chambers

(d) analog readout of silicon strip detectors.

2. *Level 1–Level 2 Buffering*—Studies will be made of the optimal data buffering during Level 1 and Level 2 trigger processing. While it is very likely that analog storage will be used for the Level 1 Buffer, both analog and digital data storage will be considered for the Level 2 buffer. Prototypes will be built and tested at least for the analog storage. The optimal storage and processing will be determined for each of the detector systems.

3. *Optimal readout Architecture*—Because of the potential crosstalk between the circuits generating and transmitting digital data and the preamplifier and detector, it is essential that local readout be considered an integral part of the front end design. In addition to the minimization of crosstalk, one of the primary goals will be to determine the architecture(s) and readout protocol that most simplifies the design of the front end chips while achieving the goals for speed and reliability. Emphasis will be on the assembly of data prior to transmission over an optical fiber or other digital transmission medium. However, it is also planned that system-level simulations will include conceptual designs of the entire data collection system to ensure consistency of the assumed readout protocol at the front end with requirements on event building and distribution of data to trigger processors and the large parallel arrays of microprocessors used for final event selection.

4. *Interaction of Front End with Level 1–Level 2 Trigger System*–The impact of different conceptual designs for a Level 1–Level 2 trigger system on the front end chips will be investigated. As is the case for the readout, the characteristics of the trigger system and the interactions of the front end chips with the trigger system can have a big impact on the area and power required for the front end chips.

5. *Level 1 Trigger and Level 2 Trigger inputs*—Signals for the Level 1 trigger decision must be generated as part of the front end circuits. The most evident case is for the calorimeter system where fast local analog sums of the transverse energy (E_T)

detected locally, followed by digital sums to obtain global information will form the basis of $\sum E_T$, missing $E_T(\not{E}_T)$, jet, and electron triggers. The fast analog sums are in fact the most critical part of the circuit in terms of shaping and signal to noise. It may also be practical to calculate ratios, such as that of hadronic to electromagnetic energy, at the local level.

It is not clear at this point whether tracking information will be required in the level 1 trigger; some recent studies have indicated that cuts on calorimeter information alone should be sufficient. However we intend to study this issue further and to investigate methods for including tracking information at Level 1 should it prove necessary or desirable.

It is also important to investigate whether the desired inputs to the Level 2 triggering system impose any requirements on the front end circuits beyond those of Level 1.

1.3 Motivation for a Broad Effort on Front End Electronics

It may be argued that the electronics development rightly belongs as part of proposals for detector development. While it is clearly essential that the electronics be optimized for any given detector, we feel that there are a number of reasons that argue strongly for a large coherent effort on front end systems in addition to the numerous smaller efforts.

1. *Completeness*—There are a number of difficult issues to be addressed that rarely get sufficient attention (largely because of lack of manpower) from smaller independent efforts. Such issues include (*a*) definition of optimal voltage levels, risetimes, and bus structure for readout (differential vs. single ended), (*b*) power distribution, (*c*) system initialization, (*d*) fault analysis, (*e*) calibration, and (*f*) testing.

2. *Common Problems and Efficiency*—Many of the circuits to be developed, such as charge preamplifiers, operational amplifiers, fast low power differential receivers, analog memory units, bus drivers, etc., are common to several systems. While the exact specifications may vary from one detector system to another, there is a large overlap in the knowledge and design techniques required for optimization of the circuits and in the measurement techniques for evaluation.

3. *Radiation Hardness*—A broad program that evaluates the radiation hardness of different bipolar, MOS, BiMOS, and JFET technologies must be carried out. For analog circuits in particular, the radiation damage of devices and subcircuits needs to be evaluated comprehensively so that the hardness of new circuits can be largely predicted. Simultaneous inclusion of devices and subcircuits from many different front end systems, and a sharing of the burden of device characterization and subcircuit evaluation after exposure, should significantly decrease the cost and time scale for these investigations.

4. *Common Architecture*—It is important that the readout architecture and the protocol for interaction with the trigger system be as similar as possible for all detector systems. Thus architectural designs that appear optimal for one type of detector must be evaluated for other major detector systems to ensure that the desired homogeneity will address the needs of all detector components.

1.4 Organization of Proposal

An overview of the front end architecture and a discussion of many of the systems issues that are common to different detectors are presented in Section 2. Performance goals, schematic diagrams, and a discussion of the most difficult design issues for each detector system are presented in Sections 3–6. Section 7 summarizes the wide variety of subcircuits that are required based on the preceding sections and discusses other common development issues such as the evaluation of radiation hard processes. Section 8 outlines possible approaches to the calorimeter Level 1 trigger and specifies those issues particularly relevant to the front end circuits. Plans for the study and simulation of the overall readout and data acquisition, at the conceptual design level, are presented in Section 9. Interactions with industry are discussed in Section 10 and liasons with other R&D projects (generic and subsystems) are discussed in Section 11. Finally, the required manpower and resources, as well as the division of responsibilities and milestones are summarized in Section 12.

2 Front End Architecture and System Level Design.

During the past few years, a number of workshops have been held on topics related to SSC detectors. The discussions in these workshops have resulted in a preliminary definition of the design of the large-scale detector systems required to do the physics for which the SSC is being built.

During these workshops, the capabilities, characteristics and architecture of the data collection electronics needed for these large detectors have also been discussed; any system satisfying the requirements will be a very significant extrapolation from the data collection systems of existing detectors. Although the basic architecture of the data collection system is evolving into a fairly stable design, there remain many details to be worked out. To guarantee the success of the SSC detector systems, it is essential to carry out a complete and carefully planned program of electronics development.

The term, "Front End Architecture", is broadly used to describe the topology and functionality of the system of electronics that is physically located on the detector. In the case of an SSC detector, this includes a major and extremely vital portion of the total electronics system. The design of this portion includes the implementation, in integrated circuit form, of some very sophisticated components. It also includes the implementation of a complex system of data and control signals to 'glue' these components into a cohesive system.

The data collection system will be almost completely imbedded within the structure of the detector. Many components of the system will therefore be relatively inaccessible for months at a time, while others may be inaccessible for years. It is extremely important that the design of the system take this factor into account. Some implications are:

- *Reliability and Failure Modes*—The reliability of all data collection components must be very high. Many required functions can be implemented in more than one circuit technique. The impact on reliability of the various techniques must be assessed, and recommendations for designing integrated circuit (IC) functions developed. The design of the complete Front End system must involve an assessment of the effect of failure modes (unreliability) in all components. The effects of failures must be localized to a small part of the system. Design techniques for accomplishing this

must be developed.

- *Controllability*—A study must be made to identify the features of the system and individual integrated circuits that must be controlled and/or monitored from outside the detector. These features must provide the means to circumvent the effects of failure modes; to monitor the vitality of the IC's; to calibrate the circuit response where necessary; and to anticipate changing physics requirements.

- *Verification*—Means must be provided to verify the proper operation of the complete data collection system. There should be the capability to execute a range of tests, from checks of the vitality of individual FE channels to verification of the mechanisms for collecting complete sets of data from events.

- *Power dissipation*—The removal of heat from inside the detector is a significant problem. The power dissipated by the IC's must be limited to values that are commensurate with practical cooling mechanisms. For tracking systems, the requirements of low mass may significantly limit the techniques for cooling.

- *Radiation hardness*—The level of radiation experienced by a data collection electronic component will depend on its location with respect to the collision center. For a five-year period, for example, the charged particle dose will be of order 200 Mrad/R^2, where R is the distance (cm) from the beam line. Many of the integrated ciruits to be used in SSC detectors must be implemented in radiation hard processes to withstand doses of this magnitude.

Figure 2.1 shows the basic organization of the data flow paths of the front end electronics. The portion above the dashed line–located on the detector–receives signals from the detectors, filters them with Level 1 and Level 2 triggers (trigger mechanisms are not shown), and delivers packets of digitized data off the detector to the event processing facility.

It is expected that two basic types of integrated circuits will be required–Front end IC's (FE's) and data collection IC's (DCC's). The need for other types of IC's may become evident as the development of the front end system proceeds.

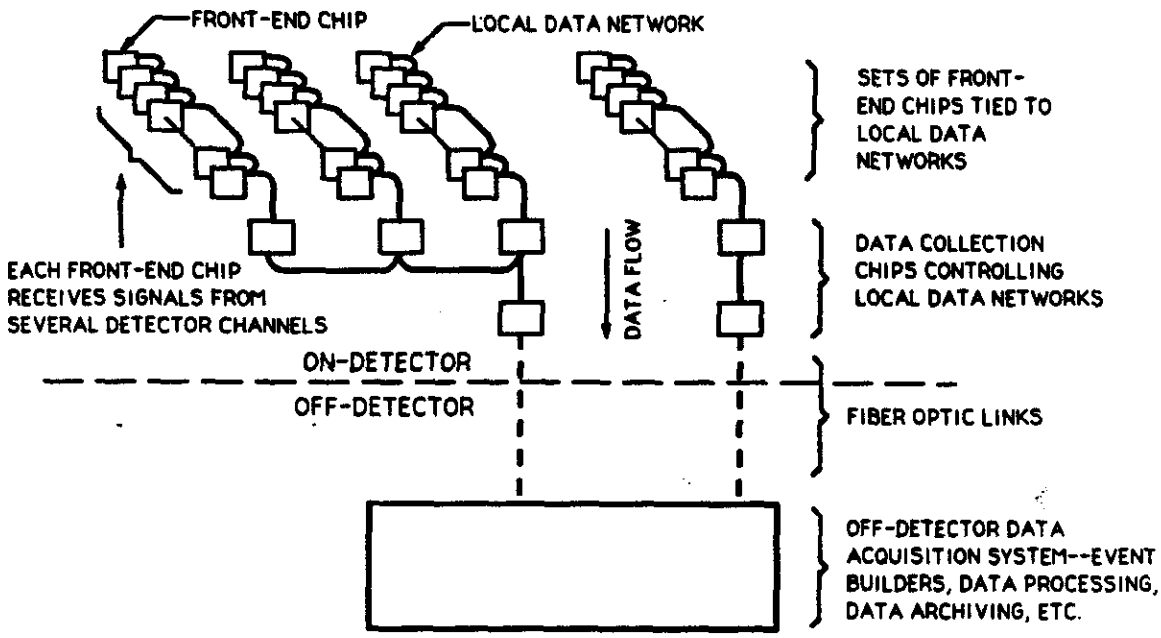


Figure 2.1: The basic organisation for the data collection scheme. The front end ICs (FEs) accept the signals from the detector and the Data Collection ICs collect the data from a set of FEs and prepare it for transmission.

Front end Integrated Circuits (FE's) accept signals directly from the detector elements; process and store the signals during the time necessary to process Level 1 and Level 2 triggers; and output digitized data selected by the Level 2 triggers. DCC's interface to a small data bus structure that interconnects a small number (*eg.* 16–128) of FE's. They control the collection of digitized (or in some cases analog) data from the FE's, and organize it for transmission off the detector towards the event builder.

2.1 Front End Integrated Circuits

The high beam interaction rate (one interaction per 16 nanoseconds) of the SSC imposes some very stringent requirements on the design of integrated circuits for the front-end system. Some of these requirements are:

- *Zero Deadtime*—Analog signals are continually being received by the FE's; digital data signals are continually being output;
- *Time Precision*—Collection of all data from a particular event requires that data be "tagged" to a precision of one or a few bunch crossings.
- *Data Compaction*—It is impractical (if not impossible) to move the data from every channel off the detector for every interaction. It is therefore desirable to process the data at least two ways while it still resides on the FE: 1) to filter the data through two levels of triggering; and 2) to sparsify (see below) the data . In the discussion that follows we assume two different levels or stages of triggering (event filtering). The architecture discussed could be utilized as well with a single trigger level if higher rejection factors are achieved with the Level 1 trigger or higher bandwidth of the readout is implemented. Similarly, the data could be stored on-chip during three successive levels of triggering. However, two trigger levels prior to the collection of all the data for an interaction appears to be the most likely scenario.

Figure 2.2 is a generalized block diagram of a Front End (FE) integrated circuit chip. Actual FE's will probably contain structures that are quite different from the structure in the figure; however, the illustrated structure is useful in visualizing the functions of the FE chips, and their interactions with the "standard" set of data and control signals.

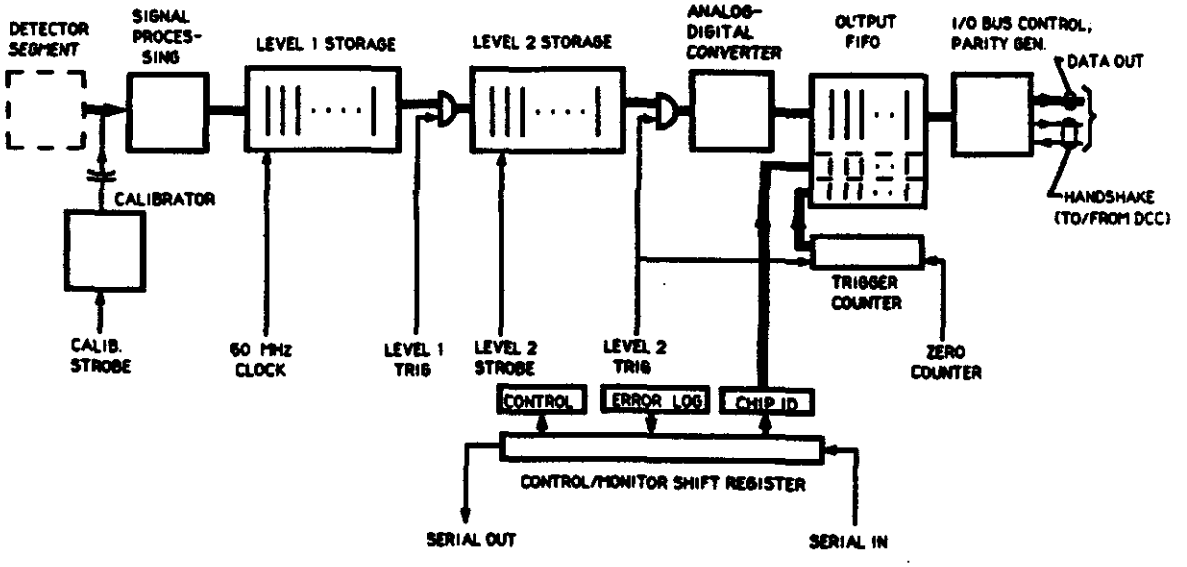


Figure 2.2: A design of a "classical" front end integrated circuit (FE).

The figure shows a single channel, which would process the signals from a single detector element. A typical FE chip will contain several channels; in a complete detector, there will be tens of thousands of FE's processing on the order of a 10^6 channels. The signal from the detector element is received on the left; digitized data exits from the right. The details of the circuit operation are given below.

2.1.1 Signal Processing/Preprocessing

The raw signals from detector elements inevitably require some processing to derive the desired information. The processing requirements are different from one class of detector to another; however, some general observations can be made.

- *Preamplification*—The raw signals are typically in the range of a few femtocoulombs to picocoulombs, and hence require preamplification with sufficient bandpass to preserve the time of arrival of the particle being measured.

- *Data Extraction*—Before the preamplified signals are input to the Level 1 pipeline, they typically must be processed to extract the desired information. There is a limited number of types of signal parameters to be extracted. These include: signal over threshold (hit); time-of-arrival; charge; amplitude; and waveform samples (time-slices). In addition, some detectors (such as liquid calorimeters) require shaping amplifiers to develop signals for the Level 1 trigger.

- *Sparsification*—To place a certain practical bound on the data flow from the detector, FE's will generally be required to continually determine when an input signal satisfying certain criteria is present, and to store or output data only if the criteria are satisfied.

- *Calibration*—A means must be provided to inject signals into the individual inputs of FE's to simulate, to some degree of accuracy, signals from the detector element. Depending on the type of detector, this can be used to verify the vitality of the signal channel and to calibrate the gain or temporal characteristics of the channel.

2.1.2 Level 1 and Level 2 Storage

A horrendous problem in data transmission could be created by demanding that the data from every detector element be moved off the detector every beam crossing. This problem is made tractable by two features of the front-end architecture:

1. Each FE "sparses" its data if appropriate–*ie.*, makes a decision as to whether signals representing data of significance were received at each beam crossing (or at each Level 1 or 2 trigger). For a calorimeter system, sparsification may be difficult due to the long resolution time and the interest in precise energy measurements.

2. Only data associated with events passing the Level 2 trigger criteria are transferred.

The latter feature requires storing candidate data in the FE's long enough for the Level 2 trigger to be processed–which may take several tens of microseconds. The storage capacity required for this is reduced by filtering candidate data with the Level 1 trigger, which is expected to take only 1 or 2 microseconds to develop. The storage is accomplished in the Level 1 pipeline and the Level 2 FIFO in the scheme of Figure 2.2.

The optimal design of the storage in the FE's for a particular class of detector requires the careful consideration of a number of factors. Some of these factors are discussed below.

1. *Analog/Digital Storage*—The FE is expected to deliver its output data in digital form, so data from most detector types will require a multi-bit analog-to-digital conversion. Because of the power/speed tradeoff of analog-to-digital converters (ADCs), it is advantageous (or perhaps necessary) to place the ADC function where the conversion rate is minimized. Thus, in most cases, it appears that the data stored in the Level 1 pipeline will be in analog form. The ADC will then be located either between the Level 1 and Level 2 storage devices or between the Level 2 storage and the output buffer–i.e., after the Level 2 selection.

2. *Storage Element Topology*—Shift registers can be designed to accomodate either analog or digital signals, and represent a simple solution to the Level 1 storage problem. The number of cells (storage elements) required is the Level 1 Trigger delay time divided by 16 nsec–125 cells for a delay of two microseconds. A "classical" shift register, in which the data in each cell is shifted to the next at each 60 MHz clock cylce is wasteful in power. An alternate implementation that consumes less power moves simple, digital address pointers instead of the analog data.

   Other, more sophisticated and more power efficient, schemes are under development. In one such scheme, discussed in detail in Section 5, the data sparsing operation occurs ahead of the storage. The number of Level 1 storage cells can therefore be reduced significantly. A determination of the required number of cells depends on: 1) the ability to reliably predict the rate at which the sparsing criteria are satisfied–i.e., the occupancy of the detector element; and 2) knowledge of the "time smearing" of the signal–*ie.*, the number of 16 nsec buckets that each datum must occupy because of uncertainty in correlating the datum with a bucket. Each datum accepted for storage is "tagged" with the time of storage to permit correlation with Level 1 Triggers.

   Similar considerations can be exercised for the Level 2 storage. Here the number of Level 2 storage cells required depends both on the occupancy of the detector element, and the Level 1 Trigger rate (Level 1 event rejection).

3. *Storage Element Technology*—Other considerations affect the detailed design of the Level 1/2 storage for an FE and/or the choice of technology used for its implementation.

   Analog storage devices typically store signals on individual, small ($\lesssim$ 1 pF or less) capacitors. It is essential that the stored signals do not drift in value during the storage time. Studies must be made of capacitor elements in various integrated circuit technologies to learn how to design small-value capacitors having the required drift characteristics under the full range of operating conditions– temperature, operating lifetime, radiation–expected for SSC front-end systems.

   The issues of accuracy and dynamic range must also be considered. Studies are required of the design of analog storage systems capable of storing signals with sufficiently low noise level to achieve an adequate dynamic range, yet capable of providing the required linearity of response.

2.1.3 Other Front End Design Issues

1. *Cross-coupling*—When the data collection system is in full operation, the FE's will be processing low-amplitude (few mV) signals at their inputs, and simultaneously delivering digital data signals at their outputs. Since the input and output signals are uncorrelated, there exists the possibility of introducing significant measurement errors if the digital output signals are allowed to cross-couple with the analog input signals. This cross-coupling could occur from effects on the IC, or from effects on the wiring external to the IC.

   The cross-coupling can be minimized, but not eliminated, by using only balanced signal modes for the digital signals. Further studies are necessary to identify the sources of cross-coupling and to develop design rules that keep the cross-coupling to acceptable levels.

2. *Power*—The removal of heat from the front-end electronics is a difficult problem. It is therefore essential to develop a library of circuit techniques, including analog storage systems, that operate efficiently with the minimum of power dissipation.

3. *Radiation Resistance*—The development of radiation hardened FE's requires the study of the effects of radiation dose on the analog performance of the IC's. The accuracy of the analog data must not be significantly altered by radiation dose.

2.1.4 Interaction With Level 1 Triggers

The correlation between an event and the corresponding Level 1 Trigger can be established by maintaining a constant delay in the Level 1 Trigger processing, and maintaining a matching delay within each FE chip. It is expected that this delay will be in the range of one to two microseconds. The actual value will be determined by how soon the Level 1 trigger decision is available to the FE chip.

It is conceivable that the value of this delay may not be firmly established until after certain FE designs have been stabilized. It may therefore be necessary to accomodate a small number of predetermined delays, with the actual delay chosen by control signals.

When a Level 1 Trigger is received by an FE, any valid data that corresponds to the crossing that the trigger refers to is transferred into the Level 2 storage element. For certain types of detectors, the amount of data transferred may be only one time sample. For detectors with resolving times that exceed the bunch crossing time, the data transferred may consist of information recorded by the FE several bunch crossings before or after the bunch crossing associated with the Level 1 trigger and so several pieces of data may be transferred to Level 2 storage. It must be determined whether the number of samples so transferred must be dynamically controlled, and if so, by what mechanism.

2.1.5 Interaction With Level 2 Triggers

Level 2 Triggers are expected to have an accept/reject protocol and be asynchronous (*ie.* the delay between a particular Level 1 Trigger and its corresponding Level 2 Trigger may vary from event to event). The accept/reject protocol means that there will always be a Level 2 signal for every previous Level 1 trigger. If it is an accept signal, then any non- sparse data stored in anticipation of this trigger are output by the FE; if it is a reject signal then the data are erased. An important issue is whether the Level 2 triggers are generated monotonically, *ie.*, whether the Level 2 triggers always occur in the same

order (in event number) as the Level 1 triggers. Such a scheme greatly simplifies the data collection process, but may require a longer Level 2 storage time.

Once accepted by a Level 2 Trigger, valid data are digitized, if not already in digital form, and are stored temporarily in the Output FIFO Buffer. The Output Buffer holds the data until it is read out via the output bus structure (this process is described in more detail below). The size of the FIFO must be chosen carefully to ensure that there is always room to hold the data for the next Level 2 trigger. One issue to be studied is how to best "throttle" the data collection system to avoid overrunning this buffer and the Level 1 and 2 storage buffers in the FE's.

An important issue that must be resolved is how to handle events in which there are two Level 1 triggers within the resolving time of the detector. The corresponding data must somehow be shared with each of the triggered "events."

2.1.6 Outputting Data

The process of moving data from the FE's Output FIFO toward the downstream entities– optical fibers, event builders, etc.–is controlled by a handshaking protocol between the FE and the Data Collection Chip (DCC). This is described in more detail below, but some aspects that affect the FE design are discussed briefly here.

Data that are to be moved off the FE must be digital and organized into "packets." The packet will probably include additional information regarding the time (event or trigger number) and location (channel number and FE chip ID) from which the data originated. Whether the packet contains a single measured value from a single channel or several values from several channels remains to be determined.

It is essential that all FE's agree on event numbers– *ie.*, the data associated with a given event from each FE must have the same event number. In the present plan, all FE's have an Event Number Counter, which counts pulses in a common signal, such as the Level 1 Trigger or the Level 2 Accept signal. A means must be provided to synchronize the counters (the Zero Counter signal in figure 2.2) so that they all have the same count for the same event. Other schemes for making this correspondence will be considered.

Each FE must be provided with a number, the chip ID, which provides a means for

identifying data from that chip. The chip ID is stored in an on-chip register, previously loaded by the host computer.

The FE raises a Data Ready flag whenever the Output FIFO Buffer contains data that is ready to be transferred outside the FE. When the FE receives a Send Data signal, it must prepare a data packet and output it.

2.2 Local Data Network

As shown in Fig. 2.1, the readout of data from FE's is organized by connecting a group of FE's and a single Data Collection Chip (DCC) via a local data network. This network provides:

1. A byte-serial path for moving event data packets off the FE toward the downstream system;
2. A bit-serial path by which the downstream system can send control data to the FE's, and can also extract status data from the FE's.
3. Transmission of fast trigger and timing signals to each FE chip.

Groups of DCC's may be organized in a tree structure, as suggested in the figure. The result is that the event data packets from a group of FE's are funneled onto a single data path that connects to the off-detector electronics–the event builders, event processors, data storage, etc.

A proposal for the detailed design of the local data network– signal definitions, functions, etc.–is given in a report being prepared by an ad hoc working group. The following brief discussion concentrates on functionality, particularly as it indicates the need for further study and development.

2.2.1 Network Structure

Figure 2.3 shows schematically one possible local data network; it has two components that are respectively called the "parallel bus" and the "serial bus".

The parallel bus includes a 9-bit wide (eight data bits plus a parity bit) byte-serial path for moving event data packets.

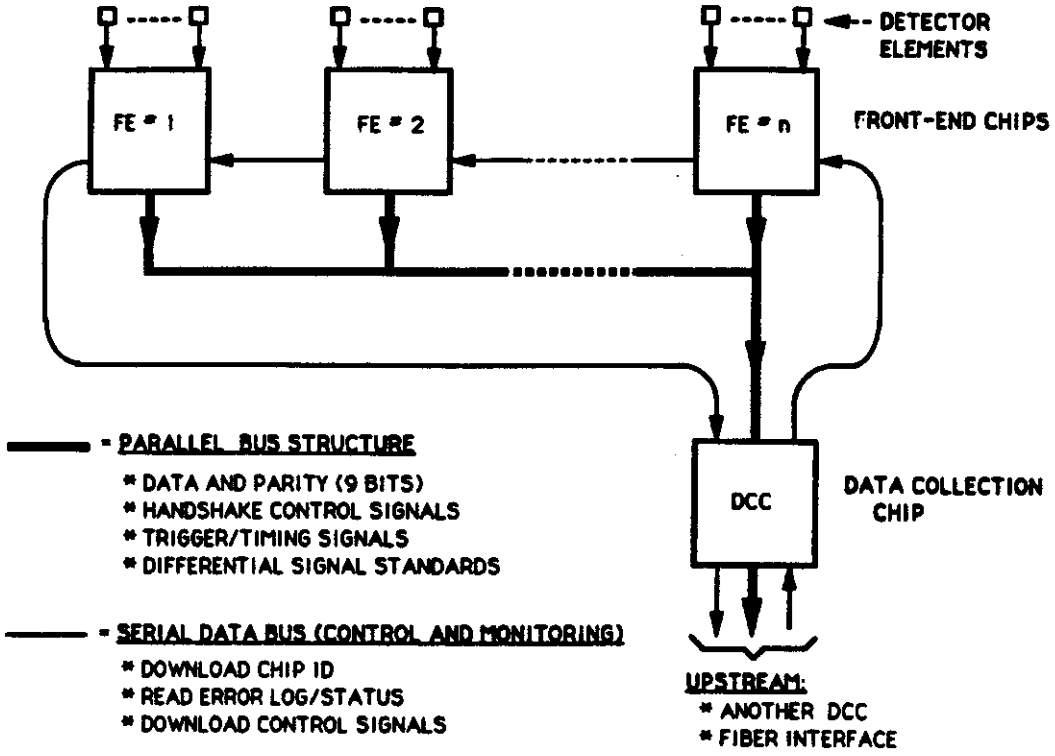


Figure 2.3: The bus structures that are used to control and read out the FEs.

The serial bus provides a bit serial path that threads all chips of the local data network. This path carries control information (such as Chip ID) to the FE's, and also carries status information from the FE's back to the control computer.

2.2.2 Readout Protocol

The design of the algorithm for transferring data packets from the Output FIFO of each individual FE onto the parallel bus requires careful study. Two possible choices can be briefly described as follows:

1. *Read Complete Event*—In this protocol, all data packets associated with a particular event are read from all FE's in the local data network before any data packets for the next event are read.

2. *Transfer When Ready*—In this protocol, data packets are moved from any FE that is ready according to a local priority (or token-passing) scheme.

Protocol 1 results in a flow of packets off the detector that has a more convenient organization for the Event Builder than 2, but may result in a lower data throughput. Protocol 2 results in a flow of packets off the detector that are misordered both in FE serial number and event number.

Other protocol variations can be defined. The evaluation of these protocols can only be done by simulation. It is important that simulation tools be acquired at an early stage, and that the work of simulating the data flow under various protocols be started as soon as possible (see section 9).

2.3 Distribution of Fast Signals

There are a number of fast digital timing signals that must be delivered to each FE on the detector with a timing precision of a few nsec. This precision is necessary to synchronize all of the FE's throughout the detector to the same beam crossing. This set of timing signals includes:

1. 60 MHz Clock;
2. Level 1 Trigger;
3. Level 2 Trigger (two signals–e.g., Strobe and Accept);
4. Calibration Strobe.

In addition, some FE's must generate trigger data signals that are to be transmitted off-detector to the Level 1 and/or Level 2 trigger processors; the timing precision of these signals must also be a fraction of the bunch crossing time.

The distribution of the timing signals must include adjustment of propagation delays to account for:

1. The propagation delay of particles coming from the beam collision point to the detector element;
2. Delays inherent in the detector–drift times, propagation delays along wires, etc.;
3. Delays in extracting information from the signal delivered by the detector element.

This may require a distribution system having remotely controlled propagation times. A study of this problem must be made.

2.4 Digital Signal Standards

As mentioned above, an SSC detector will require a deadtime-less front-end system. This means that digital data and fast timing signals will be flowing on the local data networks at the same times that the FE's are receiving low-level analog signals from the detector elements. There is therefore a serious potential for cross-talk between these two sets of signals. This cross-talk can occur both on and off the FE chip. The on-chip cross-talk must be controlled by proper IC design techniques. Off-chip cross-talk can be reduced by proper choice of signal standards and proper wiring practice.

The following are some possible choices for digital signals that will minimize crosstalk to the analog front ends:

1. differential signal modes;
2. low voltage (e.g., 200 mV) swings; and
3. controlled rise times.

Studies must be made to choose a practical set of these signal standards, and to develop designs for the wiring techniques for the local data networks.

2.5 Power Up, Reset and Initialization

Procedures for putting the entire front-end system into a state of readiness must be developed. To illustrate the problem, the following is suggested as a tentative procedure for doing this:

1. *Power Up*—Power is applied to the front-end system.
2. *Reset*—A Reset signal is sent to all elements of the system. In response, all FE's and DCC's clear all internal registers and data buffers. The serial buses for all local data networks are read to verify that all FE's and DCC's and other elements have responded to Reset.

3. *Initialization*—Via the serial buses of all local data networks, control data are downloaded into all FE's and DCC's. This includes chip ID numbers, for example. The serial buses are then read again to verify that the data were properly received.

4. *Start Clock*—The 60 MHz clock is now started.

5. *Test System*—Via the serial buses, test data are downloaded into the DCC's. The DCC's are then commanded to output this test data over the normal event data route. The results are checked.

6. *Enable Trigger Processors*

2.6 Fiber Optic Signal Transmission

It appears that the transmission of digital signals via fiber optics may play a important role in SSC detectors. The transmission of acquired event data from the front end system to the rest of the data collection system will probably be via fiber optics. Other applications within the front end system are possible, but further study is needed to determine their feasibility.

Collaborations with appropriate segments of industry are needed to investigate the following topics:

1. *Integrated Optoelectronics*—It would be highly desireable to integrate the optical transmitters and receivers directly on the front end IC's that are generating or receiving data.

2. *Fiber Optics in Local Data Networks*—The possibility of using fiber optic signal transmission within the local data networks that interconnect the FE's and DCC's is intriguing. Conceivably, the analog/digital crosstalk problem could be eliminated if clock, trigger, and data signals could be moved from the FE's over fibers. Many problems need to be solved to make this feasible, but some effort should be expended to follow the developing technology.

3. *Analog Transmission over Optical Fibers*—The techniques for improving the linearity in transmitting analog data over fibers should be investigated.

2.7 Other System Level Issues

There are a number of other system level issues that must be considered.

2.7.1 Substrates for Chip Mounting

Collections of IC chips, such as the FE's and the DCC's constituting a local data network, will be physically mounted on a substrate that also provides the wiring interconnections. Some design rules for such substrates will need to be formulated. Factors to be considered include: chip packaging; methods for mounting chips to the substrate, *eg.* surface mounting; heat removal; and conductor configurations to minimize cross-talk.

2.7.2 Interconnection of Substrates

The data collection tree structures and the distribution of control signals and power will require the consideration of practical methods for interconnecting the substrates. This will require investigation of miniature multi-wire connectors and cables.

2.7.3 Fault Analysis and Reliability

A major part (if not all) of the front end system will be buried within the detector structure, and will be inaccessible for months or years at a time. Inevitably, some components will fail during this time. It is therefore essential that the components be designed so that the effects of these failures are isolated to a small part of the system– in particular, a small enough part that its loss does not compromise the quality of the physics data.

This issue should be pursued in the several ways:

- *System Test Facilities*—The system architecture design must include consideration of facilities for completely testing and verifying the performance of the system. For example, there should be a mechanism for realistically simulating data from detector elements in a way that can be followed through the entire electronics system, including the rest of the data collection system. There should also be ways of injecting data patterns at various intermediate points in the system (the study of the DCC chip referred to above includes such a capability).

- *Failure Effects on Physics Data*—The architecture should be designed to minimize the effect on physics data of any single failure. This consideration may effect the combination of detector channels that are read out via a particular local data collection network.

- *Failure Effects Within Local Data Networks*—The effects of failures within the influence of a local data network should be analyzed. Mechanisms for reducing the effects should be formulated. For example, a mechanism for powering-down a specified FE chip, under remote control, should be investigated.

2.7.4 Chip Design

General recommendations for the design of integrated circuits for the front end should be developed. These should address the methods of assessing inherent reliability of chip designs, and the methods of assessing failure effects.

Certain circuit features will need particular attention. For example, there is a need to develop a library of output drivers that do not hang the local data network when the chip is powered down.

2.7.5 Testing of Integrated Circuits

The integrated circuits required for the SSC may have operating characteristics that are not amenable to the test stands at typical silicon foundries. There may therefore be the need for test stands with specialized equipment to perform adequate tests of the IC's before they are installed.

2.7.6 Error Detection/Correction Practices

A study should be made of the practical level of error detection and/or error correction features that should be required in the transmission and reception of data packets. For example, one must decide at what level active error detection (such as the use of checksums) should be employed to ensure the integrity of the data.

3 Calorimeter Front End

3.1 Scope and Requirements

The goal of this part of the project is to develop readout electronics for calorimetry. The effort will be concentrated on ionization calorimeters, and in particular on liquid ionization calorimeters with liquid argon and with "warm" liquids. However, we emphasize that some of the circuits may be identical or very similar for silicon ionization calorimeters and for scintillator calorimeters. Liquid ionization chamber calorimeters have the potential to be the best calorimeter technology with respect to uniformity of response, accuracy of intercalibration, stability of response and radiation resistance. This development of electronics will thus be oriented toward high precision calorimetry.

The requirements on the electronics will be derived from the requirements on calorimetry. As these requirements evolve from the physics of interest, simulations, and assessments of the detector state-of-the-art, the requirements on electronics will be further refined. Some calorimetry requirements compiled from the Calorimetry Workshop, March 1989, University of Alabama, are given in Table 3.1. These requirements serve as a guide to the electronics performance in the areas of radiation resistance, calibration, dynamic range, noise and speed.

The basic components of the signal processing chain are illustrated in Fig. 3.1. Its functional elements are:

1. Preamplifier with capacitance matching and charge calibration.
2. Data recording chain, with additional gain (xl and x64), 1st and 2nd level buffer and multiplexed readout.
3. Trigger forming chain, with additional gain, summing amplifiers, fast pulse shaping, and timing and pileup inspection circuits.
4. Control circuits for calibration, sampling, memory and multiplexing

Each calorimeter segment has circuits 1 and 2 and there may be $2\text{–}3 \times 10^5$ such channels for the entire calorimeter. Various trigger sums result in a much smaller number of fast outputs, of the order of $3 \times 10^3\text{–}10^4$, as explained in Section 8.

- **Radiation Resistance:**
  - $\approx 10^6$ rads/year; $\approx 10^{12}$ neutrons/cm^2 year

- **Energy Resolution:**
  - EM , $\approx 0.15/E^{1/2}$, constant term $\approx$ 1% (low PT electrons)
  - Hadronic , $< 1.0/E^{1/2}$ sufficient, $\leq 0.5/E^{1/2}$ very good

- **Systematics, Calibration, Uniformity, Stability:** 1% if easy, 2% if hard

- **Electron/hadron Response:** $\leq$ 1.1 direct response, or by weighting (quark compositeness signal!)

- **Dynamic Range:**

  EM, 5 TeV lepton ($\approx$ 2.5 TeV in one channel) — 2.5×10^4
  Lepton isolation test $\approx$ 100 MeV/channel — $\sim 10^3$
  Hadronic, QCD jets $\approx$ 5-6 TeV in one jet cone

- **Noise (electronic-, uranium-):**
  - Lepton isolation $E_T < 4$GeV in $\Delta R \approx 0.4$
  - Missing PT $\sigma_{el} < 20$ GeV

- **Speed and Pileup:**
  - Timing (associate events and bunch crossings), $\sigma_t \approx$ 1-2 nsec
  - Integration time (hadron response) $t_m \approx$ 100-150 nsec
  - Pileup time, impact of overlap of n (e.g., 10) bunch crossings

Table 3.1: Calorimetry Requirements

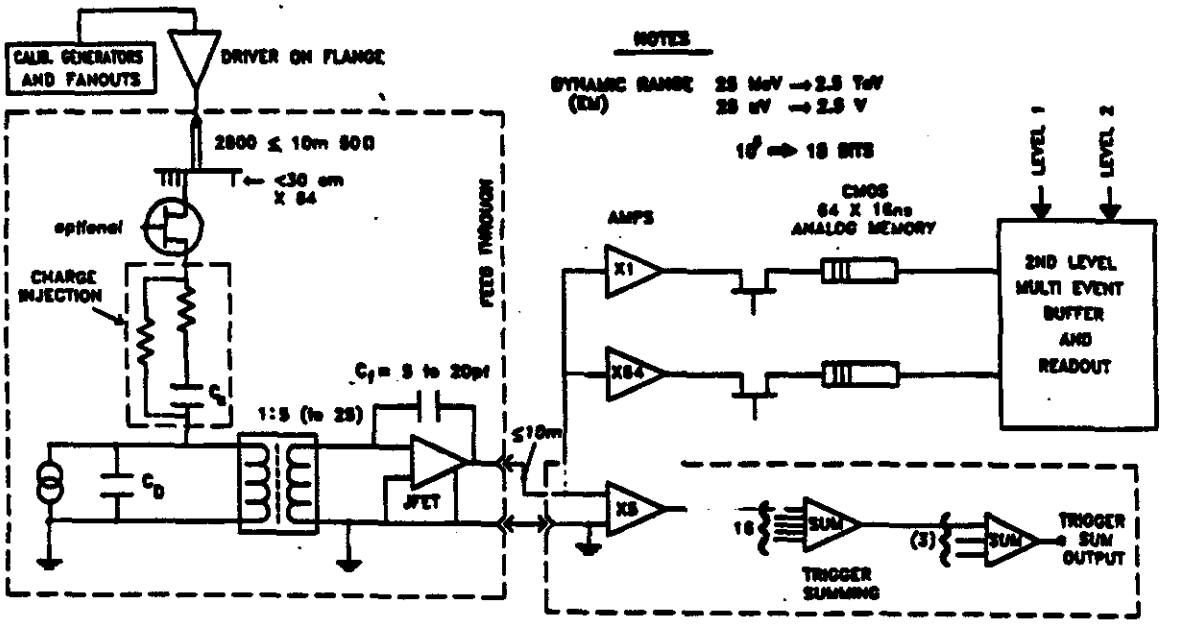


Figure 3.1: The components of the calorimeter front end electronics.

The pulse shaping in the data recording chain may best be performed by an appropriately weighted sum of several consecutive samples (taken at bunch crossing intervals, *ie.* 16 nsec). This allows programmable shaping according to the counting rate and the requirement on noise.

The pulse shaping of trigger signals may be "hard wired" with several integration times (e.g., 50, 100, 150 nsec), so that pileup and electronic noise can be minimized for different experiment conditions. An example of some of the requirements on electronics and on particular circuits is given in Table 3.2.

We discuss in the following the outline of the proposed work on various parts of the signal processing chain. Our approach is to explore various fundamental and technological limits and the tradeoffs among those limits, such as speed, noise and power. The values of some of the parameters may have to be chosen only at the time when the experiment requirements are better known.

GENERAL REQUIREMENTS:

- SPEED: 50 NSEC INTEGRATION TIME FOR OVERALL SYSTEM
- DYNAMIC RANGE: 2.5 TEV/100 MEV = 2.5×10^4 MIN.
- NONLINEARITY: $\leq$ 0.25%

MONOLITHIC CIRCUITS:

- SIGNAL AMPLIFIERS (HIGH GAIN, LOW GAIN), τ_I = 10 NSEC
- SUMMING AMPLIFIERS FOR TRIGGER SIGNALS, τ_I = 5 NSEC
- ANALOG MEMORY 64 X 16 NSEC, DYN. RANGE = 3×10^3
- CONTROL CIRCUITS FOR SAMPLING, MEMORY AND MULTIPLEXING

SIGNAL AND SUMMING AMPLIFIERS - BIPOLAR

ANALOG MEMORY AND CONTROL CIRCUITS - CMOS

SIGNAL SHAPING (FILTERING) BY WEIGHTING OF 16 NSEC SAMPLES.

THIS PART OF THE SYSTEM IDENTICAL FOR LIQUID ARGON, WARM LIQUID, SCINTILLATOR AND SILICON CALORIMETRY.

Table 3.2: Requirements for Calorimeter Electronics

3.2 Preamplifiers

Charge preamplifiers for ionization chamber calorimeters must have low noise, a short response time and low power dissipation. In addition, their apparent input resistance created by the feedback circuit should be within a certain range to provide an aperiodic transfer of charge in the presence of inductance in the connections between the ionization chamber and the preamplifier. One of the most difficult requirements is a very large dynamic range. In the electromagnetic (EM) part of the calorimeter the dynamic range will be at least 2×10^4 and may be as high as 10^5. A linear response over a large dynamic range requires currents and voltages that result in high power dissipation. Matching of the detector capacitance (for noise optimization) by increasing the size of the input transistor rather than by a transformer also results in higher power dissipation. It appears that a power dissipation in the range between 75 and 200 mW is necessary depending on the type of capacitance matching.

The preamplifiers will have to be located at the detector electrodes for optimal speed and noise levels. Any remote location of the preamplifiers would result in significant increases in the noise and the charge transfer time. Location at the electrodes requires a minimum power dissipation and a high resistance to the radiation in the calorimeter. For liquid argon, the preamplifiers should be able to operate immersed in the liquid.

The input amplifying device should have the device time constant C_{FET}/g_m as short as possible (< 5 nsec), the equivalent series noise resistance should be close to the theoretical value of $\approx 2/3\, g_m$, and the parallel shot noise should be negligible. Presently junction field-effect transistors are the only type of device that satisfy all these requirements. However, their optimum operating temperature range with respect to the noise is $120°K < T < 300°$. Development of devices which could operate at $\approx 90°K$ (directly in liquid argon) will be pursued in collaboration with industry (INTERFET, Corp.).

Preamplifier circuits will be explored and developed with a particular goal to minimize power dissipation. The question of monolithic versus hybrid technology will be thoroughly explored. A process with dielectrically insulated transistors will be explored first.

Preamplifier hybrid circuits, with JFETs developed for the HELIOS uranium-liquid argon calorimeter, have been irradiated with ^{60}Co gamma rays (both at room temperature

and at $77°K$). At a total dose of 5 Mrads, no increase in the noise of JFETs made by INTERFET has been observed. This study will be continued as it constitutes a crucial part of the program on calorimeter electronics.

Preamplifier circuit and JFET studies are already a subject of a generic R&D project, and they should remain so. However, funding is requested as a part of this subsystem's project for the work performed by industry on the development of JFETs and monolithic amplifiers with JFETs.

3.3 Transformers and Series Coupling of Electrodes

For ionization chamber electrodes with a capacitance > 1 nF, ferrite core transformers have been the best solution for the capacitance matching providing minimum noise, minimum power dissipation and protection of the preamplifier from discharges in the chamber. Ferrite core transformers saturate in a magnetic field strengths > 0.03 T. For operation of the calorimeter in a strong magnetic field (0.5 to 2 T), two potential solutions have to be investigated: a) magnetic shielding; and b) the series connection of electrodes known as the "electrostatic transformer." The total electrode capacitance in the barrel calorimeter may be 500–700 μF. With 2×10^5 readout channels this gives an average capacitance per channel of 2.5 to 3.5 nF. In the EM calorimeter, the sections will be smaller (~ 0.5 nF) and in the hadronic (HAD) calorimeter they will be larger. Series connection of electrodes may provide a solution for the EM calorimeter, but it would leave HAD sections mismatched (because of the limit of how many electrodes can be connected in series). In any case, preamplifiers will have to be placed at the electrodes to minimize the noise and the charge transfer time. The series connection of electrodes precludes interleaving of absorber-readout cells into separate readout channels for redundancy.

The technology of transformers and their shielding will be investigated in this project and in the Subsystems Proposal on Liquid Argon Calorimetry. The series connection of electrodes will be investigated in the subsystems proposals on Liquid Argon Calorimetry and on Warm Liquids.

3.4 Calibration, Gain Control and Testing

In order to realize the potential of liquid ionization chambers for very high uniformity and accuracy of intercalibration (in the range of a few tenths of a percent) accurate charge injection into the electrode- preamplifier circuit is mandatory. This is possible to achieve with either precision resistors (0.1%) or capacitors, with pulse waveforms corresponding to ionization chamber signals. A more serious problem is the generation of sufficiently large amplitudes to cover the dynamic range. A real challenge is to develop a pulser distribution system where individual channels and arbitrary groups of channels can be pulsed under computer control. Intercalibration of all channels can be achieved by a relatively simple system. However, to test the functioning of the data storage and recording channels and to test the trigger electronics a more elaborate pulser distribution system is essential. Switching circuits and some buffer amplifiers for this system will have to be near the chamber electrodes in order to minimize the number of cables required.

The gain of each signal channel will have to be equalized prior to forming trigger sums. The linear and weighted trigger sums will be formed by precision resistor networks with their outputs directed into summing amplifiers. The gain equalization can be performed by either the control of tolerances of the gain elements (feedback capacitors and resistors), or by microprocessor control of the gain of the amplifier prior to the summing networks.

Development of pulser distribution and gain equalization circuits will require a substantial effort in this project and a close interaction with all projects dealing with simulations, trigger system and data acquisition.

3.5 Post Amplifiers, Shaping and Level 1 Analog Memory

The data recording chain contains memory units required to store data during Level 1 and Level 2 trigger decisions. The data are initally stored for each sample taken at 16 nsec intervals. None of the known techniques for analog storage and fast analog-to-digital conversion can cover the large dynamic range required (15 to 17 bits). Thus at least two data storage channels per signal channel with partly overlapping scales are needed, each covering 11-12 bits. Preamplifiers are followed by two fast amplifiers with different gains, indicated as xl and x64 in Fig. 3.1, which drive the memory units.

The impulse response from the detector electrodes to the preamplifier output may have a rise time of no less than about 40-50 nsec, due to the charge transfer time from the electrodes to the preamplifier. In order not to further increase the response time of the system, the fast amplifiers should have a rise time of less than about 15 nsec. The fast amplifier response, together with the charging time constant of the memory unit, provide sufficient bandlimiting at high frequencies to satisfy the Nyquist criterion. Low frequency cutoff may be provided in the preamplifier and additionally in the fast amplifier, to provide a short enough decay time in the response that the pileup in any single channel does not restrict the dynamic range. Thus no elaborate pulse shaping would be performed prior to the memory. The actual optimal shaping for a given counting rate will be realized as a weighted sum of a number of consecutive samples. This shaping should be programmable so that the pileup and the electronic noise could be minimized for a particular experiment. This type of signal processing is equivalent to pulse shaping by conventional time invariant circuits. A wide range of weighting functions can be realized.

As discussed in Section 7.1.6, analog memories appear at present to be preferable to ADCs and digital memories from power considerations. The Level 1 memory would be a series of 16 nsec samples 1–2 μsec long, the exact length to be established later on the basis of the overall trigger system. The development effort on analog memories will be concentrated on the speed, dynamic range, and control of various imperfections. Those of paramount concern include the gain and pedestal variations from cell to cell, stability, dielectric absorption and charge retention. The monolithic circuits to be developed are fast amplifiers, probably in bipolar technology, and the analog memory in CMOS switched capacitance technology. A challenge in the state of the art is a 6-fold increase in the sampling rate compared to a recently developed memory with an equally large dynamic range (ZEUS collaboration).

3.6 Level 2 Buffer and Readout

The Level 2 Buffer will have to store the data selected by the Level 1 trigger for 20–50 μsec. The data flow into the Level 1 memory is simple and the choice of an analog memory appears to be obvious. In the case of the Level 2 Buffer there are many options

for the transfer of data from the Level 1 Buffer (and also some problems), and the choice of the analog or digital storage is less obvious. All the questions of the data transfer and readout involve the data acquisition architecture and the concept and design of the trigger system. Some of these questions are discussed in Sections 2 and 5.

We propose to concentrate here on the study of technology options and the necessary circuit development for the Level 2 memory. If the choice of the memory is an analog one, it will have to be developed within this project. If the choice is for ADC and a digital memory, we expect to rely on industry for ADC development and availability.

3.7 Fast Summing Amplifiers for Level 1 Trigger

Trigger sums will be formed of larger and smaller groups of channels that will make possible a measurement of the total transverse energy ($\sum E_T$), missing transverse energy ($\not\!\!E_T$), jets, and electrons within a short time from the event (100-150 nsec), as discussed in Section 8. These sums can be formed in the trigger channel of the signal processing chain as indicated in Fig. 3.1. Each signal channel contributes a current to several summing amplifiers. The current for various linear and weighted sums are defined by precision (0.1%) resistors. The signal from the preamplifier is first amplified (shown as $\times 5$) in order to make the noise from the summing resistors and amplifiers negligible compared to the preamplifier noise. The grouping for the sums may be as small as 8 channels for the HAD towers and 48 channels for the EM towers. One also needs a linear ($\sum E_T$) and a weighted sum ($\not\!\!E_T$) for the whole calorimeter. The number of inputs to one summing amplifier is limited mainly by the speed of response and the noise allowed. If we assume that 16 inputs is an acceptable number, then a cascade of three summing amplifiers would provide a sum of 4096 signal channels. The upper limit to this number is determined entirely by the location of circuits and necessary interconnections. Where longer connections (more than ≈ 5 meters) to the final sums become necessary, partial sums may be digitized (after final pulse shaping) with very fast ADCs, and the data transmitted by optoelectronic links. The number of such partial sums will be small ($\sim 3 - 10$ x 10^3) compared to the number of signal channels.

The summing amplifiers must not increase the response time and they should be linear.

To satisfy this, their rise time should be less than about 5 nsec. They should also have a low input impedance since their input is a current summing point. Such amplifiers will require advanced ($f_t > 7$ GHz) bipolar technology. The pulse shaping will be performed on the sum signals. Since the number of such shaping amplifiers will be small (several times 10^3), some degree of sophistication may be allowed in the design and implementation of the circuits. Several values of the effective integration time (e.g., 50, 100, 150 nsec) should be provided in order that the pileup effects and the electronic noise are minimized. The pulse shaping, which forms a short pulse from a long electron drift time in liquid ionization chambers, is shown in Fig. 3.2. These pulse shaping circuits can best be realized in bipolar transistor technology as a combination of monolithic and hybrid circuits.

3.8 Time Measurement and Pileup Inspection

Time measurement will be performed on all trigger sum signals to associate the signal with a particular bunch crossing. The signals in ionization chamber calorimeters are formed from very large numbers of ion pairs (typically $\approx 10^8$ electrons for 100 GeV of deposited energy) so that statistical fluctuations in the induced current waveform are very small. Thus the timing can be performed by centroid finding rather than by leading edge (as in gas and scintillator detectors). Bipolar pulse shaping provides centroid timing information which is energy independent (walk-free) at zero crossing. Timing resolution is dependent on the signal to noise ratio, and thus on the deposited energy and the trigger tower size. For jet-sized towers a resolution of a few nanoseconds at 100 GeV is expected. For individual towers, time resolution of a few nanoseconds can be obtained for $E_T > 5 - 10$ GeV. The timing measurement can be performed by a zero crossing discriminator on a bipolar waveform, or by several samples on a unipolar waveform. These are equivalent operations, but with different circuits.

Pileup inspection can best be performed by looking for some characteristic waveform distortion on trigger sum signals. For example, a simple indication of pileup is a discrepancy in the time between the peak and the zero crossing of the bipolar output signal from a standard single event signal.

The most severe design requirement for the sum signal circuits in any type of calorime-

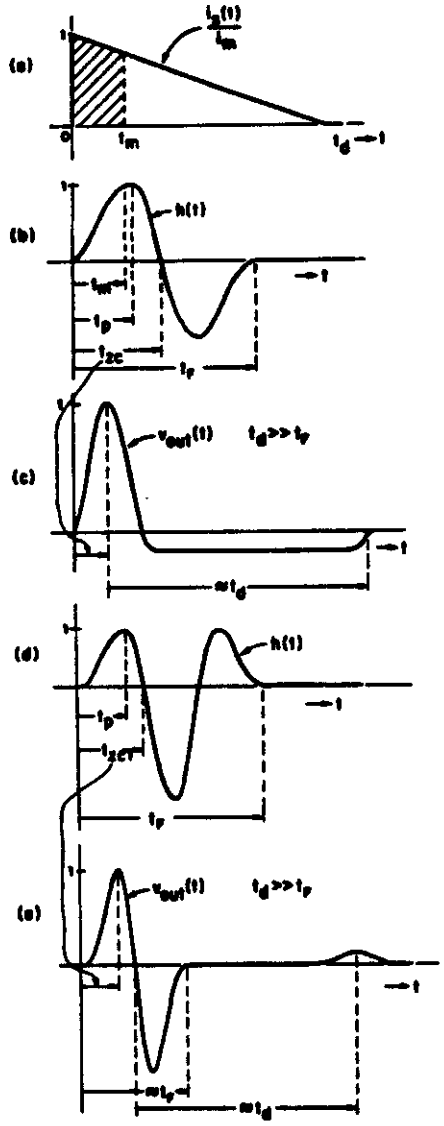
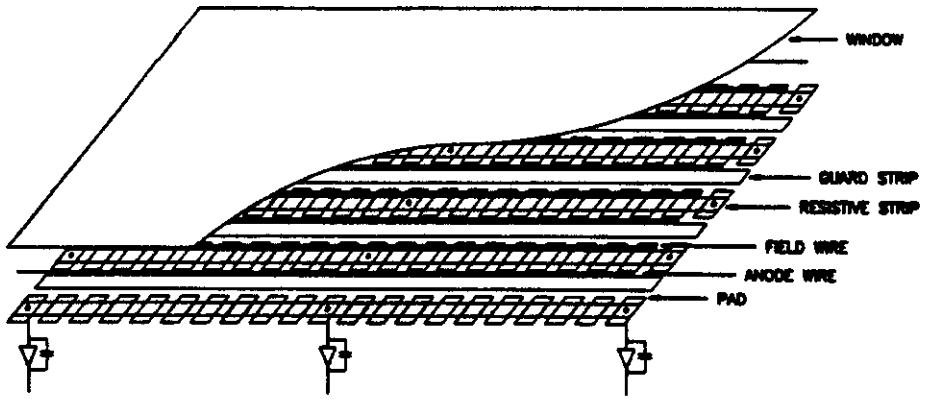


Figure 3.2: Processing of signals in ionisation chamber calorimeters. (*a*) Induced current waveform for ionising particles traversing the interelectrode gap (single-carrier collection as in liquid media). (*b*) A bipolar impulse response of the detector-amplifier system. (*c*) The output of the bipolar shaping driven by the signal in (*a*) for fast pulse shaping $t_f \ll t_d$. (*d*) A three-lobe impulse response. (*e*) The output of the three-lobe shaping driven by the signal in (*a*) for $t_f \ll t_d$. The term t_d represents electron drift time across the chamber interelectrode gap.



PAD CHAMBER STRUCTURE

Figure 4.1: The mechanical design of a pad chamber detector.

ter will be to equalize the time delay of all signal channels and the response of all calorimeter sections to a few nanoseconds (a fraction of the bunch crossing interval).

4 Readout Electronics of Proportional Chambers with Interpolating Cathode Pads

4.1 Scope of Detector

The gas wire proportional chamber with interpolating pad readout ("pad chamber") is intended as a low-mass ($< 0.1\%$ of a radiation length) detector with unambiguous 2-dimensional readout. A few pad chamber planes may be located in the central tracking region to ease the task of track reconstruction of other one-dimensional tracking detectors such as straw tubes in a high density of track environment. Interpolating pad chambers may be more appropriate for tracking in the forward direction.

A "pad chamber" detector (Fig. 4.1) [1] consists of a wire plane in between a pad plane

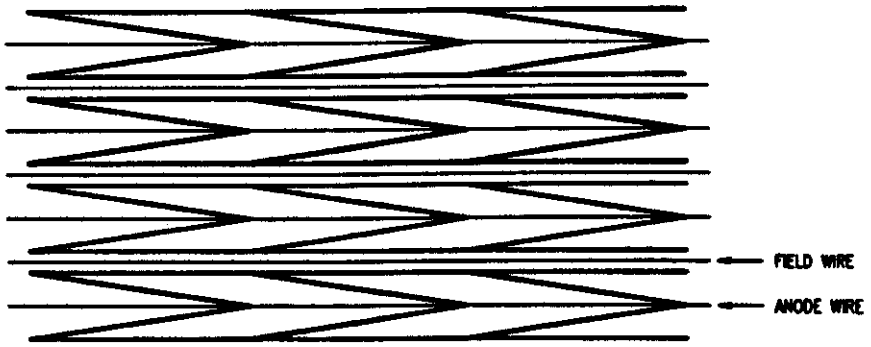


Figure 4.2: A chevron cathode pad geometry.

and a second cathode plane. The pad plane consists of pixel- like elements. Adjacent pad rows are separated by guard strips to reduce the "crosstalk" charge induced.

A resistive layer is silk-screened on top of each pad row to achieve resistive charge division. Depending on the desired resolution one out of every N pads (where $N \sim 10$) is read out.

A different method for achieving charge division uses chevron shaped electrodes (Fig. 4.2). This type of chamber has a coarser resolution, and may be used for tracking at larger radii from the interaction point. However, its manufacturing is greatly simplified since no resistive layers are involved.

4.2 Front end electronics

Assuming a cell size of $4\,\text{mm} \times 10\,\text{mm}$ the readout density will be 25000 channels/m^2. The solution of bringing such a large number of channels outside the active area by means of printed wires is not practical.

The amount of electronics to be placed on the cathode plane is dictated by the requirement of achieving a substantial degree of multiplexing and yet avoiding excessive

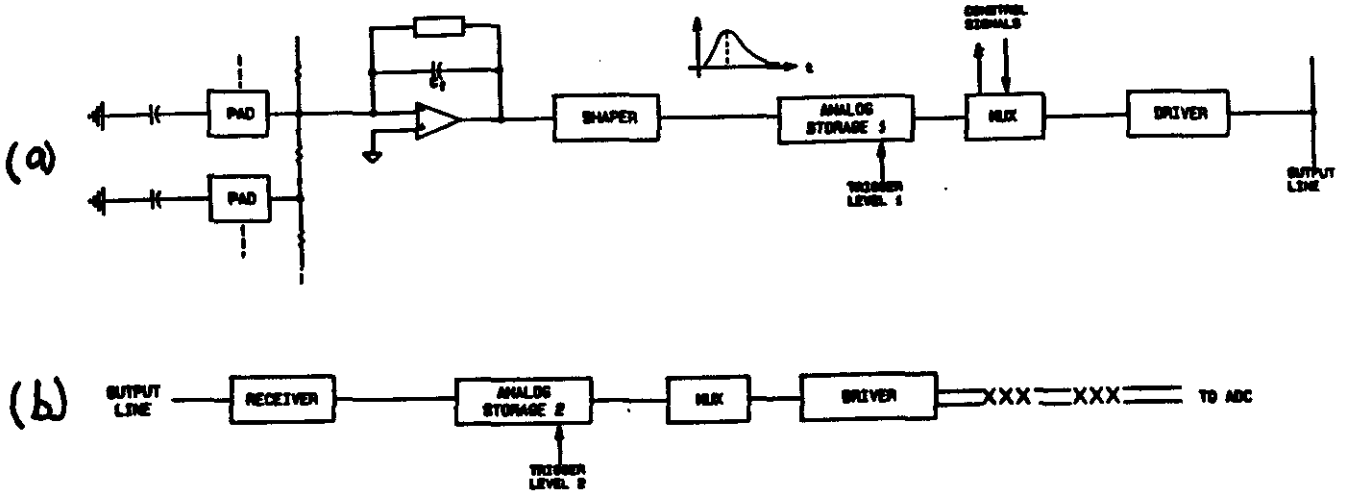


Figure 4.3: A possible configuration for the front end electronics for a pad chamber detector. Figure (*a*) shows the electronics that could be mounted directly on the pad chamber cathode. Figure (*b*) shows the electronics that would be mounted on the periphery of the chamber.

power dissipation in a region where heat removal is difficult. It is conceivable to locate the preamplifier, the shaper and the first level of storage on the cathode plane (Fig. 4.3). Only those channels showing some activity and selected by the Level 1 trigger are to be read out, thus allowing a substantial degree of multiplexing. The driver located on the front end circuit will drive only a short line ($\sim$ 1 m) to the periphery of a plane. The second level of analog storage, additional multiplexing and a driver for the long line which will send the signal to the ADC, will be located on the periphery of the chamber. If more efficient methods of cooling the backplane region are conceived or more power efficient front end circuits can be designed, it could be possible to locate even the second level of analog storage on the chamber itself. In this case a larger demultiplexing is allowed and the ADC could be located on the periphery of the chamber. Only digital-signals would be transmitted over a long distance, thus easing stray signal pickup problems.

Each component of the analog processing chain in the front-end circuit will be consid-

ered in more detail in the next paragraphs.

4.3 Preamplifier

Placing the front-end electronics right on the cathode plane will virtually eliminate all stray capacitances at the input.

Given the small detector capacitance ($< 2\,\mathrm{pF}/10$ pads row), the noise results may be quite good despite the poor noise properties of MOS integrated devices.

Operation of the chamber in a moderate regime of gas gain, thus allowing operation at high counting rates with respect to space charge effects and the chamber lifetime, will still yield space resolutions with $\sigma \sim 100$ microns. CMOS technology for the front-end circuit will allow sophisticated control logic and analog storage to also be integrated into the circuit.

Since adjacent preamplifiers are connected by a resistor of $\sim 10^5$ Ohm, the input offset must be controlled within to $\sim 10\,\mathrm{mV}$ in order to avoid stray currents, or AC coupling must be employed. An important point to study will be the DC biasing of the preamplifier: a $\sim 1\,\mathrm{MOhm}$ resistor in feedback is the most desirable solution circuit-wise, but may be difficult to integrate for a large dynamic range. The impact of active DC restoration techniques (which imply some deadtime) on the performance of the detector must be evaluated.

4.4 Shaping Amplifier

Some rudimentary shaping (~ 50–$100\,\mathrm{ns}$ peaking time, unipolar) is used for noise filtering and bandwidth limitation. Further shaping is provided by a combination of weighted samples.

4.5 Level 1 Analog Storage

To resolve multiple tracks and achieve good position resolution, the readout cell size is chosen so only a small percentage ($< 1\%$) of the channels have a signal. Sparsing techniques can thus be employed to reduce the amount of information being stored. For example (Fig. 4.4), the information may be stored only when a signal exceeds a given

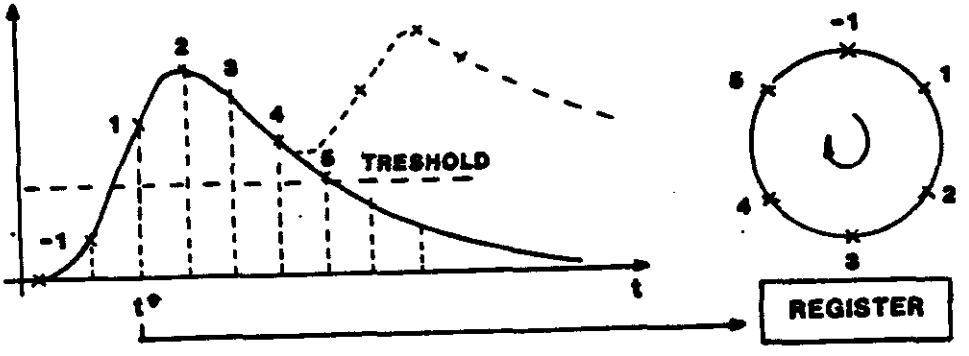


Figure 4.4: A typical signal from a cathode pad, showing schematically where the threshold might be set and the analog levels that would be stored in the shift register for that signal.

threshold. Memory capacitors may be continuously overwritten until a signal is detected, which would preserve one or two samples before the threshold detection. The time of the first sample above threshold or some other time reference must be stored in a digital register. The control logic must also be able to recognize the presence of a second event partially superimposed on a previous one and record it too. For centroid reconstruction, it is necessary to store sub-threshold signals in adjacent channels.

4.6 Multiplexing and Driver

Only active channels for those events selected by the Level 1 trigger will be transmitted to the second level of analog storage. This allows a substantial multiplexing of signals from different channels to a single output line. The driver will drive only a short line in order to avoid excessive power dissipation in a region where heat removal is a problem.

4.7 General Issues Concerning the Design of Front End Circuitry

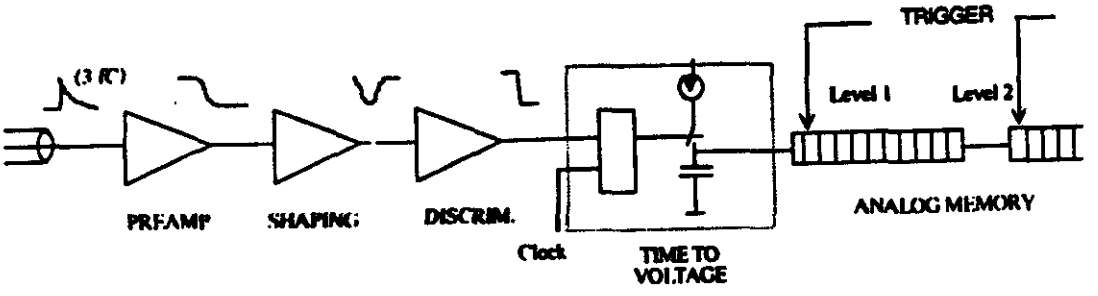
Radiation levels are substantial in the central tracking region, given the proximity to the interaction point. The choice of a radiation-resistant process is essential, and the failure mechanisms must be firmly established, including the effect of radiation on noise. Once the effect of radiation is understood, radiation-resistant circuit topology must be evaluated. Reliability of prototypes and test circuits in a radiation field must be studied.

Another worrisome point is the resistance to electrostatic discharges (ESD), which are an unfortunate reality for gas proportional detectors. The thin gate oxides used to increase the radiation resistance are particularly prone to ESD damage. Active and passive protection schemes must be studied and evaluated in order to achieve the desired reliability.

Packaging of the circuit must be addressed in order not to compromise the low density of the detector and yet protect the electronics and the delicate connections to the integrated circuits.

REFERENCES:

[1] Debbe et al. Multiwire Proportional Chamber with Highly Segmented Cathode Pad Readout; Proceedings of 1989 Wire Chamber Conference, Vienna, 13-17 February 1989.



REQUIREMENTS:

TIME RESOLUTION:	< 0.5 ns
DOUBLE PULSE RESOLUTION:	20-30 ns
MEMORY STORAGE:	1 us
ENC:	700-1000 e-
POWER:	< 10-15 mW
RADIATION HARD:	1-10 Mrad
SIZE:	< 1 sq. cm/channel

Figure 5.1: The functional elements of the readout electronics for a drift chamber.

5 A Complete System of Drift Chamber Electronics

We now discuss a prototype design for a complete system of drift chamber electronics (see Fig. 5.1). The goals of the system are a time resolution of < 0.5 nsec, a double pulse resolution of 20–30 nsec, full Level 1–Level 2 buffering and nearly deadtime-less data acquisition. The guiding principle of the design is the desire to minimize the power consumption wherever possible without sacrificing the rather ambitious performance goals. Since drift chambers come in a wide variety of shapes and sizes, it is necessary to make some assumption about the detector characteristics. For the purpose of the signal to noise discussion presented here, we will assume that each drift chamber wire may be represented by a source capacitance of 10 pF. For chambers in which the wires are significantly longer than 2 m, it is probably desirable to terminate the wire at the far end in its characteristic impedance. In this case, the detector is perhaps better represented as a resistive load. Calculations of signal to noise made with this detector model yield very similar results to those presented below, though longer wires imply higher noise.

Because of the short measurement times and relatively large capacitance of the detector, bipolar transistors are superior to MOS for the preamplifier and shaping amplifier. We also choose to implement the comparator in bipolar because of the better matching obtained with bipolar transistors. For the analog memory and associated control logic, CMOS is clearly the technology of choice. The current switching for the time-to-voltage converter (TVC) could probably be implemented equally well in bipolar or CMOS; we have chosen to include it on the CMOS chip because of the close association with the analog memory. It is anticipated that the entire system may be implemented in two chips, one bipolar and one CMOS, though it remains to be seen whether the high speed comparator may be included on the same piece of silicon as the low noise preamplifier. It may be necessary to package it separately.

We proceed to discuss the design issues of each of basic circuit elements and comment in some detail on the architectural issues, as this system provides a good specific example of some of the general issues raised in Section 2. A number of conclusions reached in this design are relevant to the electronics for other detector systems; in particular aspects of the overall architecture that minimize power dissipation, such as a "data driven" analog memory and "virtual" Level 2 storage, are likely to be relevant to the readout of wire chamber pad and silicon strip detectors.

5.1 Signal Processing

5.1.1 Preamplifier

For a bipolar preamplifier, the most common choices for the configuration of the input transistor are common base or common emitter with resistive and/or capacitive feedback. Since the noise sources of the transistor itself are identical, differences in the noise performance will arise primarily from the biasing network. It is sometimes argued that a common base is a poor choice since there is no current gain between the input and the collector where both the collector resistor and the emitter resistor contribute noise. On the other hand it may also be argued that common emitter with resistive feedback is a poor choice since the feedback resistor contributes significant noise. While the exact choice will depend on the details of the application, it may be said that for detector capacitance of

order 5–10 pF and shaping times of less than 10 nsec, one may choose R_c and R_e or R_f to to be sufficiently large that the contribution to the noise is less than 10%. In this case the signal to noise ratio obtained with either the common emitter or common base configuration is nearly identical. However, for the common base configuration the combination of relatively large I_c (of order 0.5 mA) and R_c, $R_e > 15$kOhm implies rather large power supply voltages and hence significantly higher power consumption. The common base does provide a greater degree of stability when it is desired to use the preamplifier with a wide range of detector capacitances and with detectors that may introduce significant phase shift into the fedback signal. We choose (at least initially) the common emitter configuration for the lower power dissipation.

5.1.2 Shaping Amplifier

The shaping amplifier must provide additional gain and determine the overall bandwidth and pulse shaping that is required for the desired signal to noise ratio and double pulse resolution. Typically pole-zero cancellation is used to cancel the dominant pole of the preamplifier and additional stages of integration are used to provide a transfer function of the form

$$H(s) = \frac{k}{(1+sp)^n}.$$

(For very advanced techologies, it may not be necessary to include the pole zero cancellation). This corresponds in the time domain to an impulse response of the form

$$h(t) = A\frac{t^{n-1}}{(n-1)!}e^{-tp}.$$

The output waveform is shown for several values of n in Fig. 5.2. For the purpose of the following discussion we define the "peaking time", t_p, to be the time from the application of an impulse charge at the input to the time of maximum voltage at the output. We define the "measurement time", t_m, to be the time delay for the output voltage to go from 10% of the maximum value to the maximum value.

For applications in which the average time between detector signals is much larger than the desired measurement time (*eg.* pad chambers or silicon strip detectors) simple RC-CR shaping, which corresponds to $n = 2$, is usually adequate. However, in cases where the counting rates per detector element are sufficiently high that double pulse

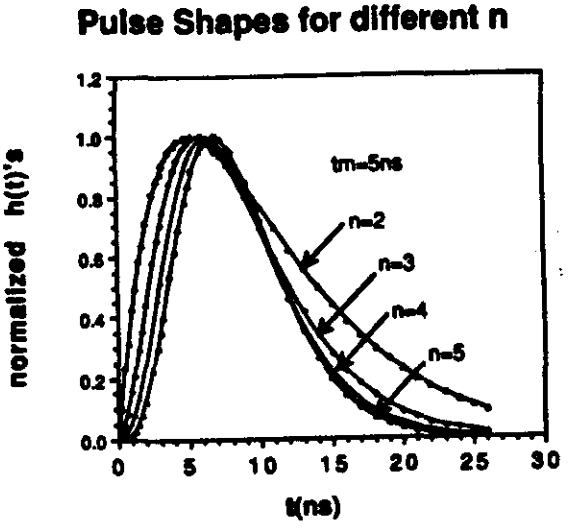


Figure 5.2: Impulse responses for a preamplifier/shaping amplifier with n pole transfer functions.

resolution is critical, such as is true for wire readout of drift chambers for which the occupancy is anticipated to be 5–10%, it is advantageous to use shaping with $n = 3$–4. The improvement in the double pulse resolution due to larger number of integrations is illustrated in Figure 5.3. Here the double pulse resolution is defined to be the time duration between the leading and trailing edge of the pulse attaining an amplitude that is 2.5% of the peak amplitude. The lines of constant t_m correspond to nearly constant noise, though there is some improvement as n increases.

To achieve a given double pulse resolution, one may of course choose to use $n = 2$ with a smaller value of t_m than would be the case for $n = 4$; this however will lead to somewhat larger noise.

An example of a simple shaping circuit that yields $n = 4$ is shown in Figure 5.4. The four integrations arise from the pole-zero of the first differential stage, and from integrations due to the parasitic capacitance at the collectors for each of the three differential stages. The circuit is similar in functionality to a single ended version developed by Radeka et al. The differential version was developed for integrated circuits for bias stability, to minimize

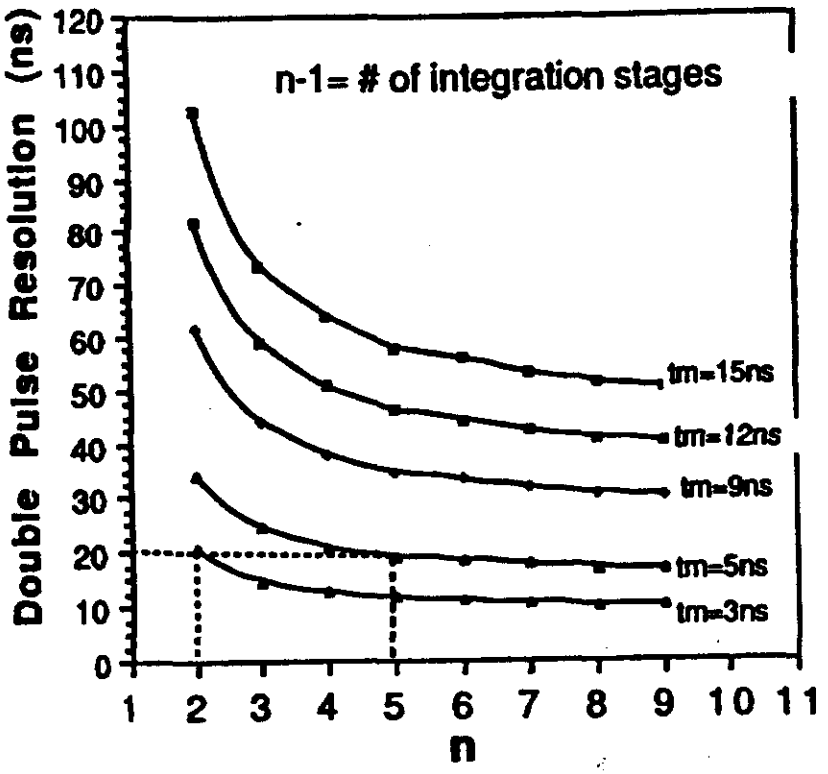


Figure 5.3: Double pulse resolution versus number of integrations (n) for various measurement times t_m.

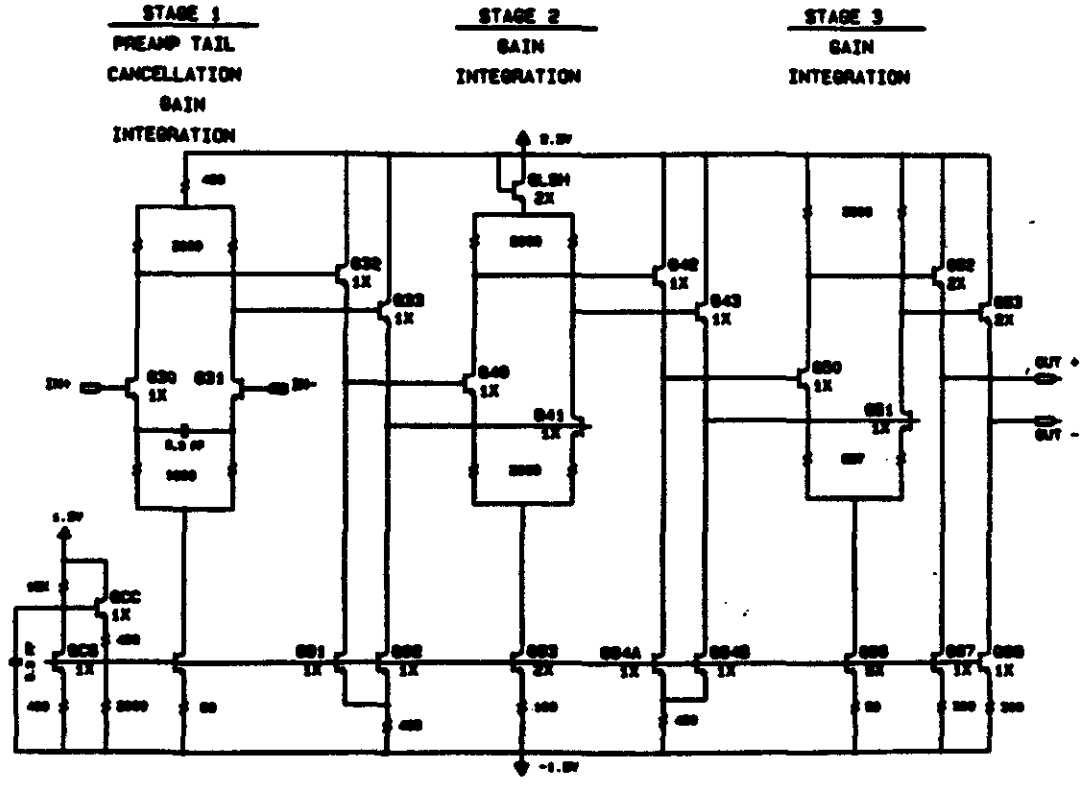


Figure 5.4: An example of a simple shaping circuit that yields n=4.

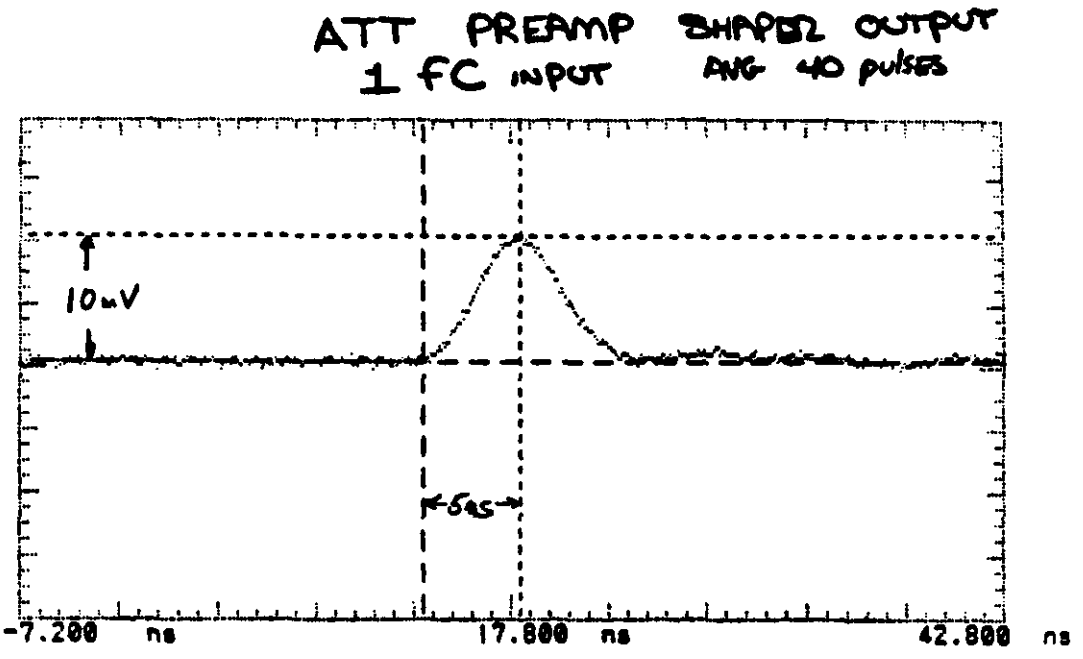


Figure 5.5: The measured impulse response of the preamplifier/shaper fabricated with an AT&T process to a 1 fC input.

feedback and crosstalk on chip, and to increase the radiation hardness of the circuit. This circuit has been implemented in an AT&T process; the measured impulse response of the preamplifier and shaper to a 1 fC input is shown in Fig. 5.5. A comparison of the calculated and measured noise is presented in Fig. 5.6.

In the last stage of the amplifier an additional pole-zero stage will be included in future versions to approximately cancel the $1/t$ tail on the pulse due to the motion of positive ions in the drift chamber.

5.1.3 Comparator

For leading edge timing applications, a fast comparator is required. While this could in principle be implemented in either CMOS or bipolar, the latter has been chosen primarily because of the lower offsets that can be obtained with bipolar. One can readily obtain matching of bipolar transistors to approximately 1 mV while matching for simple CMOS comparators is more typically 5–10 mV. In addition, a comparator with output risetime

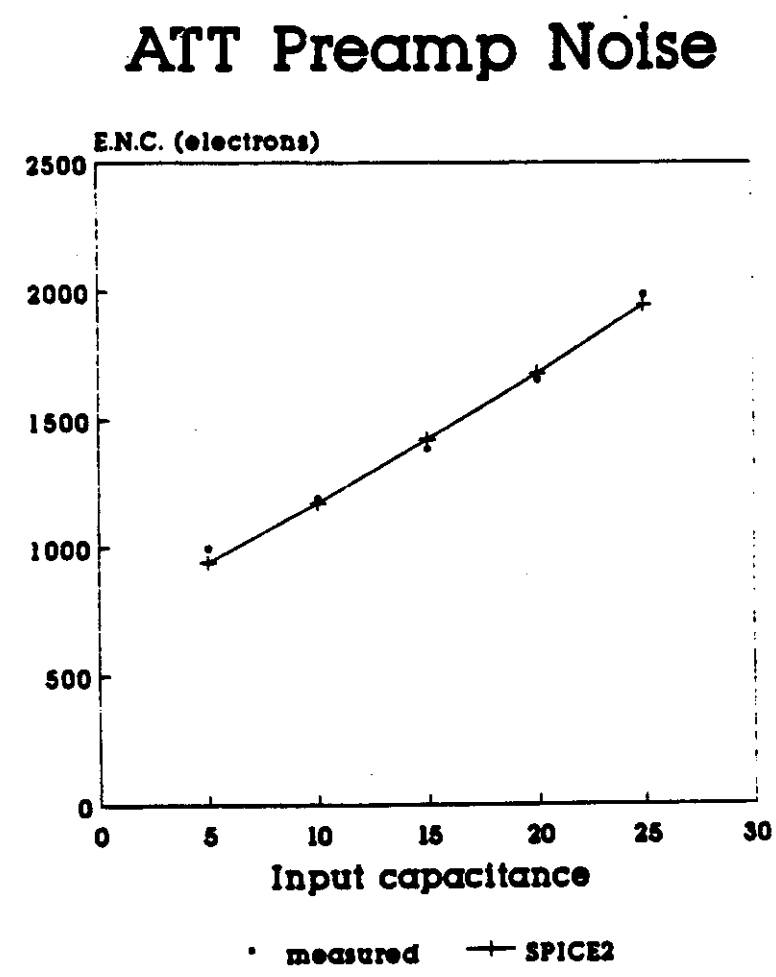


Figure 5.6: A comparison of the measured (points) and calculated (line) noise for the preamplifier/shaper circuit fabricated with the AT&T process.

of 2–3 nanoseconds is likely to consume less power when implemented in bipolar rather than in CMOS.

5.1.4 Interconnection between Comparator and Time to Voltage Converter

Because the preamplifier, shaping amplifier, and comparator are implemented in bipolar, and the time to voltage converter, Level 1–Level 2 analog memory, and readout are implemented in CMOS, the minimum system consists of two chips. It is desirable to locate the two chips rather close together both to increase the packing density and to reduce the power in the output driver of the comparator by reducing the capacitance of the interconnects. At the same time, one of the most significant challenges is to prevent the comparator output and the signals on the CMOS chip from coupling back to the preamplifier with sufficient amplitude to cause oscillations or spurious signals. That this is a nontrivial problem is seen by the following simple calculation. If one assumes a 1 cm trace going from the wire to the preamplifier, 1 cm trace leading from the comparator output to the TVC, and an average spacing of order 1 cm, the capacitive coupling from the comparator output to the input is of order 10 fF. If the output of the comparator were single ended, (the risetime 1 nsec), and the voltage swing 3 volts (to drive the CMOS chip), the induced charge at the input of the preamplifier, solely due to the capacitive coupling, would be 30 fC, more than 20 times larger than that required to trigger the comparator. A far more reasonable approach is to use a comparator with fully differential outputs, a risetime of 2–3 nanoseconds, and a voltage swing of 200 mV. This should reduce the crosstalk from comparator output to preamplifier input by a factor of several thousand compared to the single ended, large voltage swing.

5.1.5 Time-to-Voltage Converter

We now consider a system for measuring the time of pulses. If the resolution required is not smaller than 1 nsec, it is possible to use fully digital systems, as recently demonstrated by the development of a fully digital time memory system in an advanced CMOS process. We have chosen to develop a mixed analog-digital system both because superior time resolution may be obtained, and because we believe that such an approach may provide a

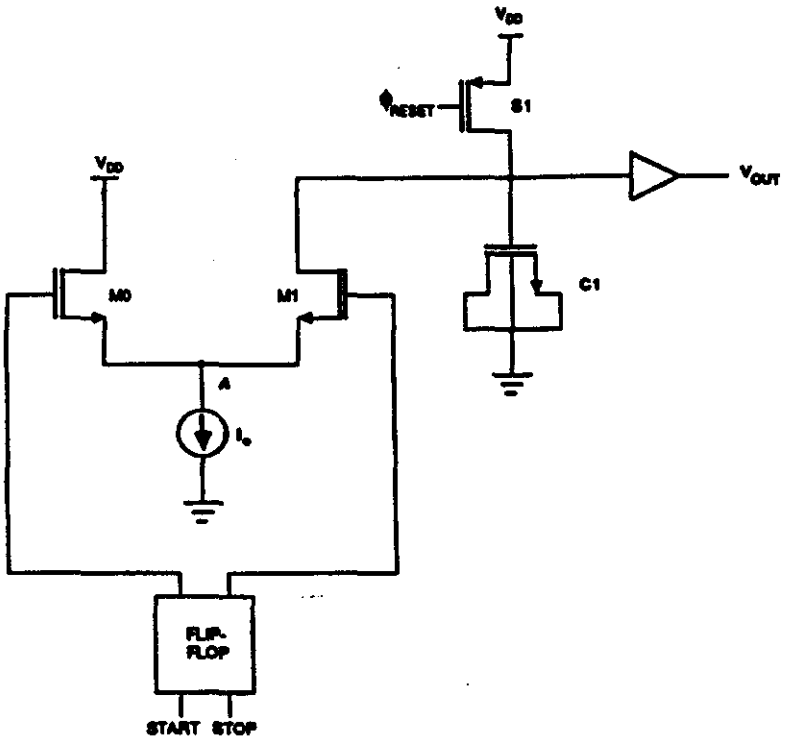


Figure 5.7: Schematic diagram of the time-to-voltage converter.

lower power solution. This belief has been substantiated by the fact that the digital system recently developed dissipates approximately 100 mW for time resolution of 1 nsec and a Level 1 storage time of 1 μsec. By contrast, we anticipate that the total power dissipation for the system we are proposing will be less than 5–10 mW. In this system the time of a signal pulse relative to a reference clock system, such as the bunch crossing frequency, is measured with a TVC and the time of the pulse on longer time scales is provided by counting the number of clock pulses or simply identifying the crossing number.

A schematic of the time to voltage converter is shown in Fig. 5.7. In the quiescent state, all of the current i_o flows through M0. A pulse from the comparator sets the flip-flop thereby turning M0 off and M1 on. The current i_o then flows through M1 and begins to discharge the capacitor. The trailing edge of the next clock pulse resets the flip-flop switching the current back to M0. The result is a voltage stored on the capacitor which is proportional to the time difference between the time of the signal of interest and the trailing edge of the clock pulse. This prototype TVC circuit has been implemented in a 1.6 micron CMOS process; the measured response showing the change in voltage on the

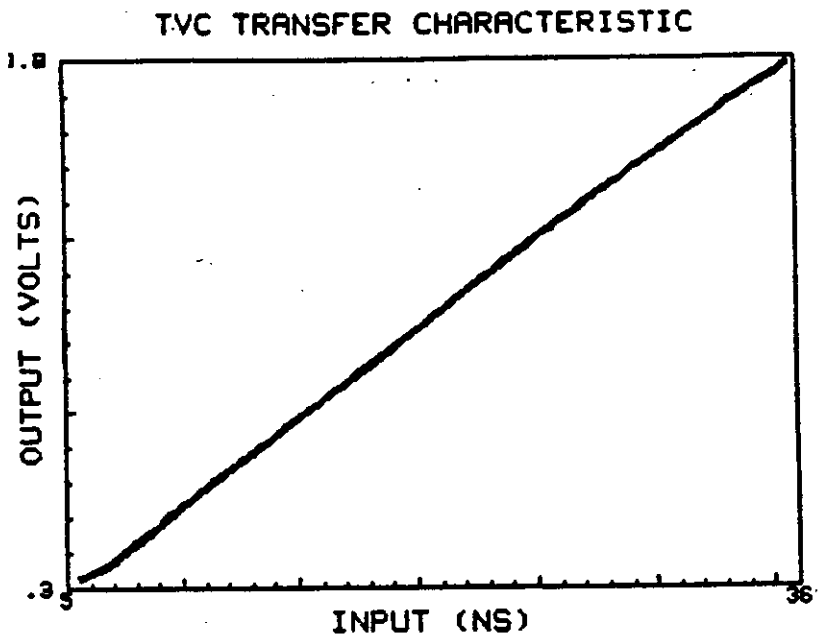


Figure 5.8: Measured response of the time-to-voltage converter. The response is superimposed for all eight capacitors used in the analog memory.

capacitor versus the time difference is shown in Fig. 5.8.

5.2 System Architecture

We now consider each of the other elements required for a complete system; these include:

1. Level 1 - Level 2 Buffering
2. Interaction with trigger system
3. Event identification
4. Calibration
5. Event readout -analog or digital

5.2.1 Level 1 Buffering

Given the very high interaction rate and the fact that a time interval of approximately 1 μsec is likely to be required for the Level 1 decision as to whether a given event is interesting or not, it will be necessary to store data temporarily on chip.

A number of techniques exist for storing analog data, the most notable being that of charge-coupled devices (CCD's) and the use of switched capacitor techniques. CCD's possess a number of attractive features, in particular the fact that the time of the event is directly correlated at any given instant with the location of the data in the CCD. In a system where the CCD is clocked at the crossing rate, the crossing with which data is associated may be readily identified. CCD's also have the advantage that all signals are propagated along the same path thus greatly reducing the problem of different offsets and gains for different measurements. However, CCD's are very inefficient in terms of power since they are clocked continuously, whether data is present at a given time or not, and all storage elements are clocked each crossing.

We therefore consider a capacitor array, such as has already been utilized in analog memory units developed for other experiments. In the simplest mode of operation, which would be applicable to voltage "waveform sampling" as well, a new capacitor is selected at regular intervals, for example at the 60 MHz crossing frequency. This scheme, which might be referred to as an "analog ring buffer", is essentially the same as that employed in the SLAC analog memory unit, in a voltage sampling circuit developed for the ZEUS calorimeter at HERA, and in a recent analog memory unit developed at LBL. For the case of 60 MHz and a 1 μsec delay, 64 storage locations would be required. The regularly clocked sampling preserves the correlation between crossing number and the location of the data as was true for CCD's. However, since only one switch is clocked at a time, the power consumption will be much less than that for a CCD. The primary disadvantage compared to CCD's is that each storage location will have a different offset, since different switches are used for each, and possibly a different gain if the capacitors are not well matched. The first problem, that of variable offsets due to different charge feedthrough from different switches, can be minimized by using very small switches which are laid out in a way to be as identical as possible; of course the use of nearly minimum size devices

memory is to cycle through the storage elements at regular intervals, either sampling the voltage from a charge integrating circuit for charge measurement or selecting a new capacitor for a time-to-voltage conversion. This approach is not without its costs however. If one samples each 16 nanoseconds, then 64 storage locations are required to achieve a total memory time of 1 μsec. While the area occupied by this many locations is not inordinate, it becomes difficult to use techniques such as common centroid layout to achieve optimal matching of the capacitors. In addition, the total capacitive load presented by the drain-substrate capacitance of all the switches is not small. For example, in the 1.6 μ CMOS process referred to above, the total drain substrate capacitance for 64 switches of size $4.8\mu \times 1.6\mu$ is 0.4 pF. For the TVC application such a large capacitance would result in 5–10 nsec being required before the circuit comes to equilibrium. Finally, if the actual signal rate on a given detector element is of order 3–5 MHz (the maximum for most systems) and if the pulses are relatively short, e.g. 20–30 nsec, then one might ask why it is necessary to sample at such a high average rate.

An alternate approach, which one might call a "data-driven" architecture, is to only store a voltage if useful information is present. This approach has been applied to the time-to-voltage to voltage converter system as shown schematically in Figure 5.10. Assume that initially one of the capacitors, e.g. that with an address of 0, is selected. Upon receipt of a signal from the discriminator, a time to voltage conversion is initiated measuring the time interval between this pulse and the trailing edge of the next clock pulse. A four bit counter, the Level 1 Input Address, is incremented thereby selecting a new capacitor to be used for the next pulse from the discriminator. Since this counter is incremented at an average rate of 3–5 MHz, only 8–16 capacitors (allowing for fluctuations in the input rate) are required. This drastically reduces the total capacitance presented to either the TVC or to the output stage of the shaping amplifier for a charge measurement application.

To identify the time of an input pulse over a time interval of several microseconds, it is necessary to identify the clock pulse with respect to which the time to voltage conversion was made. A straightforward scheme for doing this is to include a counter which is incremented by the reference clock and a digital memory with one word corresponding to each analog storage element Fig. 5.10). Each time measurement then consists of an

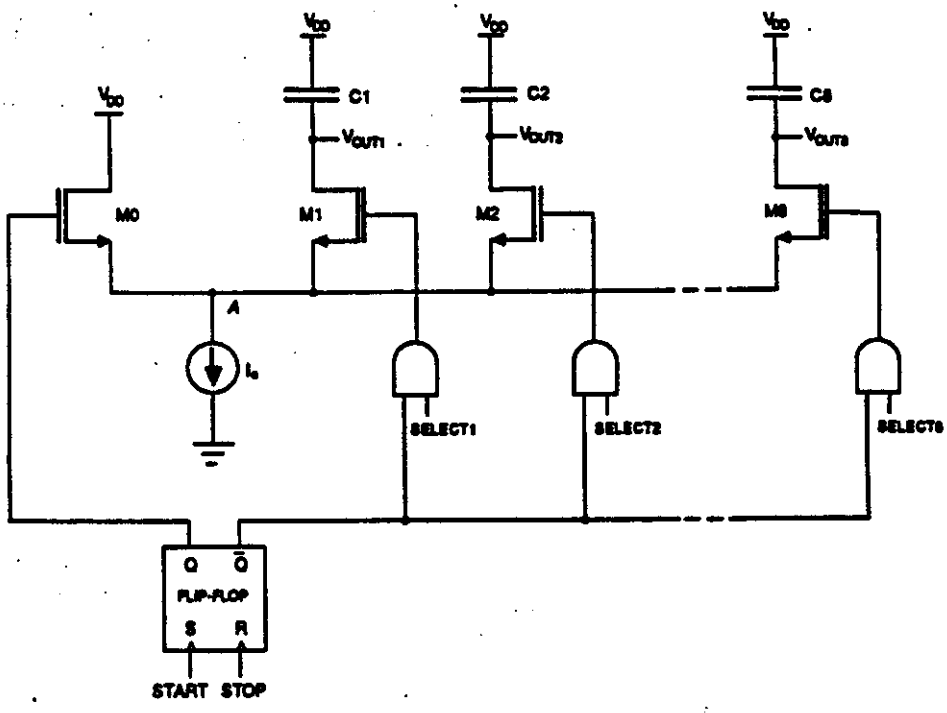


Figure 5.9: Schematic diagram of the time-to-voltage converter and analog memory.

limits the bandwidth obtainable. The second effect, gain variations, can be minimized by matching the capacitors as closely as possible, or for some applications, by the use of "charge- pumping" techniques in which only the charge on the capacitor is relevant and the absolute value of C doesn't enter to first order.

Application of the above ideas to the TVC is shown in Fig. 5.9. The right hand side of the source-coupled pair is replicated as many times as the number of storage locations desired. At any given time only one of the transistor-capacitor pairs is selected so that the circuit behaves essentially the same as described above. Switches of dimension $4.8\mu \times 1.6\mu$ were chosen (nearly the minimum size possible) and the capacitors were laid out in a common centroid geometry to optimize the matching. The transfer curve for all eight capacitors are shown superimposed in Fig. 5.8. The maximum variation is typically 11 mV which corresponds to an accuracy of 0.2 nsec. It is believed that much of this variation is due to variations in the large source followers used on the test chip and that the fundamental reproducibility is likely to be significantly better.

As noted above, the most straightforward application of the switched capacitor analog

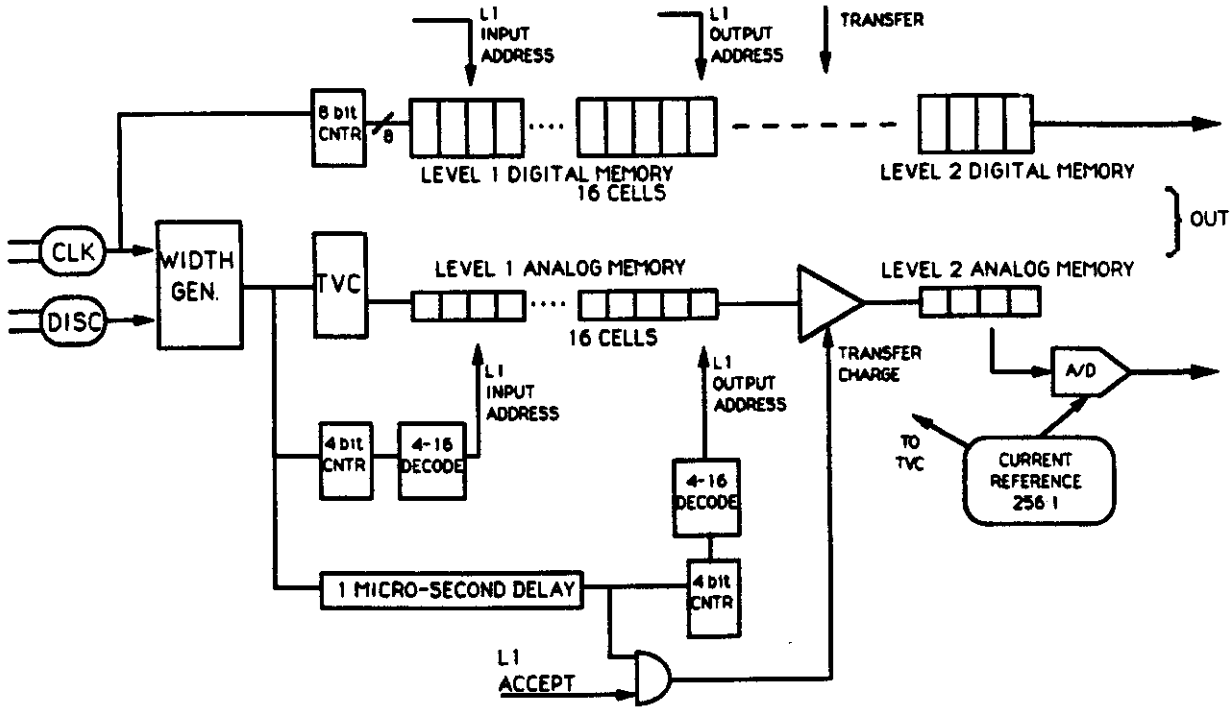


Figure 5.10: An implementation of the logic for the "data-driven" Level 1.

analog part and a digital part.

5.2.2 Level 2 Buffering

If the data corresponding to a given event passes the Level 1 criteria, it must then be stored for a substantially longer period, for example of order 30–50 μsec, while more sophisticated processing is carried out. The argument for analog storage in Level 2 is less clear than for the Level 1 storage since the average rate of data into Level 2 will be the Level 1 trigger rate (10^5–10^6) times the average occupancy for the channel in question (< 0.1); hence the average writing rate into Level 2 will be 10^4–10^5 Hz. However, if we require that the system be deadtime-less, that the Level 1 trigger system be synchronous (likely since information from different parts of the detector must be combined together at the 60 MHz rate), and if one assumes a simple real time transfer from Level 1 to Level 2 once it is established that the information corresponding to a given interaction has passed Level 1, then the data transfer to the Level 2 storage must take place at a very high instantaneous rate (in principle at 60 MHz). Said another way, if there is "interesting" data on chip

from two subsequent crossings, then the system must be able to transfer this data from Level 1 storage to Level 2 storage at the full crossing frequency. "Interesting" data in subsequent crossings may occur either from different interactions, each of which generated a Level 1 trigger, or from a single interaction passing Level 1 if the response time of the detector system in question is sufficiently long that it is desired to record the data for several subsequent crossings. It is of course possible to buffer the Level 1 Accepts, either on chip or in the trigger system, so that fluctuations in the instantaneous transfer rate from Level 1 to Level 2 are averaged out. In this case the power required for the transfer of information from Level 1 to Level 2 would be determined by the average rate rather than by the instantaneous rate. Implementation of this buffering on chip would require considerable additional control circuitry; implementation in the trigger system is probably trivial in terms of the amount of circuitry, but might yield additional complications in terms of the overall trigger design. We plan to consider this alternate approach further. However, for the present discussion, we shall assume that such buffering of Level 1 Accepts is not performed and that the Level 1–Level 2 transfer must be capable of taking place at instantaneous rates of 60 MHz.

It remains to be decided whether the Level 2 storage should be digital or analog. Commercially available six bit flash ADC's (FADC's) capable of operating at 60 MHz typically consume several hundred milliwatts which far exceeds the goal for the power dissipation for the entire system. In addition, if we are striving for mimimal power, there seems to be little point in performing analog-to-digital conversion on data 99% of which is to be discarded. We shall therefore assume that the Level 2 storage is also analog.

One must now answer the question of whether it is possible to transfer the voltage (or charge) from Level 1 to Level 2 in 16 nsec, to the desired level of accuracy, and at a reasonable power consumption. To answer this question we have designed several operational amplifiers in a 1.6 micron CMOS process with the goal of obtaining 150–200 MHz unity gain frequency for a load capacitance of 0.5 pF and with minimal power consumption. Of two circuit configurations studied in detail, the differential folded cascade configuration gives slightly better performance. Several different optimizations of this design yield the performance and power summarized in Table 5.1. While it is possible to

FOR $V_{DD} = -V_{SS} = 3V$ and $V_{in} = -1V$

	F (unity)	Power	Time to 1%	Time to 0.1%
OPAMP 1	123 MHz	0.95 mW	31 ns	42 ns
OPAMP 2	197 MHz	2.0 mW	22 ns	31 ns
OPAMP 3	232 MHz	5.3 mW	20 ns	29 ns

FOR $V_{DD} = -V_{SS} = 5V$ and $V_{in} = -1V$

	F (unity)	Power	Time to 1%	Time to 0.1%
OPAMP 1	138 MHz	1.6 mW	26 ns	34 ns
OPAMP 2	221 MHz	4.8 mW	16 ns	22 ns
OPAMP 3	272 MHz	8.9 mW	14 ns	20 ns

Table 5.1: Charge transfer times for various operational amplifiers (simulated).

obtain settling to 1% of the final value in 20 nsec with a rather modest power consumption of 4.8 mW, one must also make allowance for the switching times of the sampling and reset switches. It is then difficult at this power level to accomplish charge transfer in less than 40 nsec. It is of course possible to speed up the sampling considerably by increasing the size of the switches and the current in the operational amplifier. However, larger switches would lead to proportionately larger charge feedthrough and the resulting offsets and larger current in the operational amplifier would lead to higher power dissipation.

5.2.3 An Alternate Approach to Level 2 Storage

An alternate solution to the problem of rapid transfer from Level 1 to Level 2 storage is to decide not to move the charge, but to change the status of the storage location instead. In this case a given capacitor (storage location) can be in one of five states as shown in Fig. 5.11: (1) Available for data storage, (2) Data stored, waiting for Level 1 trigger decision, (3) Data stored, waiting for Level 2 trigger decision (4) Waiting for readout, and (5) Being Reset. Control logic must be provided which provides the following functionality: a list

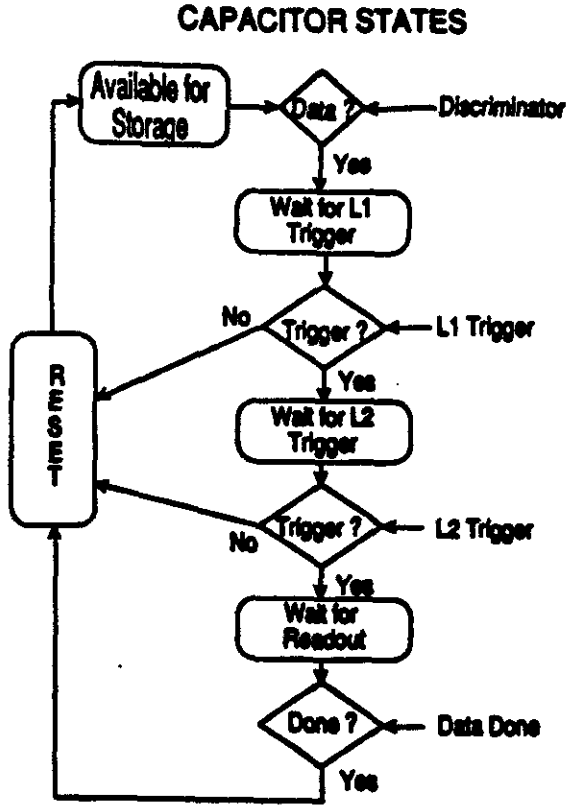


Figure 5.11: The capacitor states for "virtual" Level 2 storage; the charge is not moved until readout.

of the next available storage locations for data acqusition, a list of storage locations waiting for a Level 1 trigger decision, and a list of storage locations waiting for Level 2 trigger decision. A detailed discussion of a circuit to accomplish this is not appropriate here, but it may be stated that it is possible to provide this functionality with only moderate complexity. The goal of changing the status from Level 1 to Level 2 in less than 15 nsec is easily met with a much lower power consumption than is required for actual charge transfer. From a power point of view, the simultaneous requirements of a high instantaneous transfer rate but a low average rate are much better suited to digital operations than analog since no standing current is required.

5.2.4 Interaction with Trigger System and Event Identification

It is interesting to explore in a little more detail possible interactions of the front end circuitry with the Level 1 and Level 2 trigger systems, as assumptions made concerning this interaction can have significant impact on the front end circuit design.

At any given instant there will exist data stored in the Level 1 memory for a number of

events during the preceding 1 μsec. Each time a Level 1 Accept is received at the chip it is necessary to determine whether there exists any data on chip corresponding to the crossing with which that Level 1 Accept is associated. For the case in which clocked sampling at regular intervals is utilized, one readily can determine the appropriate capacitor as was noted above. However, for the "data driven" architecture this approach is lost and a different technique must be used. A simple solution is shown in Fig. 5.10. Each time a discriminator pulse occurs, and a time to voltage conversion is initiated, a 1 is entered into a 1 μsec delay element such as a shift register. This information, together with bits set by any other hits during the preceding microsecond propagates down the delay element and emerges from the output at the precise time that the corresponding Level 1 Accept for that event would occur. If the Level 1 Accept is True and there was data in the particular channel corresponding to that event (a condition which we will refer to as Level 1 OK), the information is transferred to Level 2 storage. As the data emerges from the delay element it increments a 4 bit counter, the Level 1 Output Address, which always points to the next address to be readout. If the Level 1 Accept signal corresponding to a given event is False, or there is no data present, then no transfer is initiated. Thus this approach automatically incorporates "sparsification" or "zero suppression".

When data is written into Level 2, it is necessary to give it some kind of event number or identification. In principle the bunch counter associated with the analog information could be utilized; however, if the total storage time through Level 2 is to be 30–50 μsec, this would require an 11 or 12 bit counter. Even this would probably not provide sufficient identification during the readout chain. Another approach is to include a counter on chip which counts the Level 1 Accepts. For any given event of interest, this Level 1 ID identifies the data with a given trigger. A six bit counter would then be sufficient to distinguish events over a 64 μsec interval.

The Level 2 Input Address counter is simply incremented each time charge is transferred from Level 1 to Level 2. However determination of the output address can be considerably more complicated depending on the assumptions made concerning operation of the trigger system. First, it will surely be true that decisions of the Level 2 Trigger System will be asynchronous. However, if these decisions are monotonic in time, then the

Level 2 Output Address can be simply determined by a counter which increments with each Level 2 strobe received at the chip. To implement this approach a signal indicating a Level 2 decision must be present each time a decision is made independent of whether the decision is True or False. This may be implemented by a Level 2 Strobe and an Level 2 Accept where the latter is either True or False depending on whether the event is to be kept or not. This contrasts with the Level 1 system where a single level is sufficient because it is a synchronous system.

5.2.5 Calibration

As anyone who has worked with large experiments is well aware, it is very desirable to reduce the number of calibration constants required to a minimum. This will be especially true in a system which has in excess of 100,000 channels and for which each channel will have of order 16–64 separate storage locations. It was already noted that for the combined analog-digital system discussed above it has been proven to be possible to match the switches and capacitors sufficiently well for a given channel that timing resolution of order 0.5 nsec may be obtained without calibrating each storage locations. However, one must still address the question of how the TVC response varies from channel to channel.

Each channel has a separate current source and a set a capacitors. One might well believe that on a given chip these may be matched sufficiently well that the response of all channels would be identical within the desired resolution. This would already be a considerable accomplishment since out of the total of 1.6 to 6.4 million independent measurement locations, only 6000 sets of gain and offset would be required. Nonetheless wafer to wafer and lot to lot variations in the current source or capacitance might be sufficiently large to cause uncomfortable variations in the response. It is therefore useful to inquire whether the circuit can be designed in such a way as to minimize the effect of these variations.

An approach which makes the measurement independent (at least to first order) of the current i_o used for the initial time to voltage conversion, and independent of the individual capacitances, is to perform an analog to digital conversion on chip using a current which

is a fixed ratio of i_o. Assume that a charge $i_o \times t$, corresponding to measurement of time interval t, is stored on one of the capacitors. The time for this capacitor to be fully discharged by a current $i_o/256$ is then $t_c = t \times 256$. This time may be measured simply by incrementing a counter with the 60 MHz clock during the conversion time. The result is an 8 bit measurement of t that is independent of i_o or any of the capacitances; the accuracy is determined by the accuracy of the current ratio. The maximum conversion time for an 8 bit result is 4 μs. The rate of conversions is the rate of events passing Level 2 times the average occupancy or $(10^3 - 10^4) \times 0.1 = 10^2 - -10^3$ Hz. Hence the conversion rate is comfortably fast and the power consumption very small.

5.2.6 Event Readout

We shall not discuss in detail the readout other than to note approximately the rate of information transfer. If one assumes the nominal rejection factors of 10^3 for Level 1, 10^2 for Level 2, and a 5% occupancy, then the initial signal input rate of 5 MHz is reduced to 50 Hz per channel. If we assume eight channels per chip and, to be conservative, 16 bits for the time measurement and 16 bits for event ID and address, the total output rate per chip would be 1.6 kbyte per second. Even a readout rate 10 times this is sufficiently small to allow the use of slow risetimes on the output signals which will be important to prevent the readout from generating too much noise on the inputs of preamplifiers.

5.3 Summary

The system described is a nearly complete prototype system for drift time measurements at high interaction rate colliding beam machines. Bipolar technology is most appropriate for the preamplifier, shaping amplifier and comparator, while CMOS is utilized for a time to voltage converter, analog storage, and control logic. Measurements of the time to voltage converter and simulations of the bipolar circuits indicate that it is possible to achieve the design goals of < 0.5 nsec time resolution, 20–30 μsec double pulse resolution, Level 1 storage for 1 μsec, and Level 2 storage exceeding 50 μsec. In addition, inclusion of on chip analog to digital conversion should enable a system in which no calibration is required to meet the accuracy of 0.5 nsec. The total power dissipation is less than 20 mW;

this represents a reduction of approximately 50 compared to existing systems.

6 Silicon detector Front end electronics

6.1 Background

The use of microelectronics to readout silicon vertex detectors is entering the second generation of development. The first generation initially used NMOS and subsequently CMOS microelectronics to readout strip detectors using an architecture developed at SLAC. In its latest form this type of readout is implemented in 3μ CMOS, each chip typically contains 128 low noise ($\sim$ 800 electrons for detector capacitances $C_d \sim 15$ pF) charge amplifiers multiplexed to a single output. The power dissipated by the chips vary from 0.4 - 2 mW per channel. Several big systems are currently being commissioned using this generation of design and the characteristics of the electronics and detector systems are well understood. All designs have been implemented in bulk CMOS and the radiation hardness required for the present generation of accelerators can just be obtained without special processing.

The second generation of architecture also uses CMOS technology, but introduced data sparsification on the readout chip. A large vertex detector system using this design of electronics is being installed on CDF at Fermilab and during the next year this system will be commissioned and will take data.

The present designs have obtained a signal to noise ration of $\sim 15:1$ which provides good spatial resolution by measuring the centroid of the charge distribution of 50 micron wide silicon strips. Charge integration times of several hundred nanoseconds are not uncommon.

6.2 The Needs of SSC

Initial designs of silicon vertex detector for SSC experiments have concentrated on fast charge integration times to resolve beam crossing information and have designed preamplifiers using bipolar technology. Analogue readout has been discarded in favour of a comparator on each channel and detector strip widths have decreased to 25 μ to restore

spatial resolution to $\sim$ 7 microns. However with 10^7 channels of readout electronics it is clear that power dissipation is a major issue, not only in removing the heat, but also in supplying the current and maintaining mechanical stability. Hence the issues for silicon detector front end electronics are not dissimilar form other sub systems: power, speed, noise, packaging radiation hardness and system design.

This proposal will work closely with the groups working on the design of silicon vertex detectors for SSC and will ensure that complementary activities are pursued.

CMOS solutions to the fast amplifier and comparator architecture will be reviewed in an attempt to reduce the power consumption to less that 1mW/channel. With an average occupancy for each strip of $\sim 10^{-3}$ it is clear that data driven storage systems at level 1 have much to offer. Methods of achieving a power efficient solution will be analysed and prototype hardware produced. Both analogue and digital schemes will be reviewed. A low power analogue pipeline has been designed at RAL which increments an address pointer rather than moving the charge. This approach will be generalized to meet the requirements of S.S.C.

The problems associated with design of the frontend electronics system, including testing, calibration, and engineering system reliably, are similar to that described for both calorimeters and drift chambers. Likewise radiation hard electronics is crucial close to the interaction region, and developments for the silicon vertex detector will be shared with the other front end systems. Silicon Vertex detectors do have unique interconnection problems which although not part of this proposal will have an impact on both reliability and system performance.

7 Common Electronics Issues

7.1 Circuits

As is apparent from the preceding sections, there are many circuit design issues which are common to different detector systems. In some cases designs which have been developed for a subcircuit in one system will be readily applicable to another system. In other cases, the specifications for the subcircuit may be different but the circuit topology and the

techniques for optimizing the design for a given set of specifications may be applicable. We list below a number of the common subcircuits and the systems in which they are likely to be utilized.

7.1.1 Low Noise Transistors and Charge Preamplifiers

Liquid ionization calorimeters, drift time and pad readout of chambers, and silicon strip detectors will all require low noise transistors for optimal performance of charge preamplifiers. For the calorimeter, JFET transistors currently promise the optimal performance both in terms of S/N and in terms of radiation hardness. For the drift time readout bipolar provides the optimal performance because of the fast risetimes (1 nsec) required. For silicon strip and wire chamber pad readout systems, it is not yet completely clear whether bipolar or CMOS will be optimal. If a shaping time of 15–20 nsec is used, which readily provides timing with a resolution of a few nanoseconds, bipolar transistors will probably prove superior. However, to meet power goals of approximately 1–2 mW per channel it may be necessary to utilize shaping times of order 50–70 nsec; in this case CMOS may be superior. These longer shaping times should still provide time resolutions less than the bunch crossing separation (16 nsec) and should prove adequate in terms of pileup for systems of very low occupancy.

7.1.2 Fast Comparators

Fast comparators will be utilized in each of the systems. For the wire chamber drift time system a bipolar comparator with time resolution of 0.5–1 nsec will be used. For the calorimeter trigger, it is likely that bipolar comparators of the zero-crossing variety will be used and time resolutions of 2–3 nanoseconds will be required. For the silicon strip detectors, wire chamber pad readout, and for the ADC in the TVC, the time resolution need only be sufficient to resolve the bunch crossings and CMOS comparators will probably be used in each of these cases. A prototype CMOS comparator has been designed for the ADC in the TVC, and it is possible that with minor variations it may be suitable for the other systems. Given their widespread use, and the priority for low power, it will be important to make a thorough study of comparators to determine the optimum design.

7.1.3 Operational Amplifiers

Operational amplifiers will be used for gain, buffering, summing, and analog memory units. Hence they will be utilized in one form or another in the wire chambers, silicon strip, and calorimeter systems. Preliminary designs and prototypes have been produced for low power (5 mW) CMOS operational amplifiers of 230 MHz unity gain frequency (C_L = 0.5 pF) and for a 300 MHZ amplifier capable of driving 10 pF (80 mW). These designs, with minor modifications, may well be suitable for systems of limited dynamic range (8 bits). However, considerable effort will be required to determine the optimal design for the large dynamic range, small offset, and high speed CMOS amplifiers required for the calorimeter system. In addition it will be necessary to develop the fast summing amplifiers used for deriving the calorimeter trigger; these will probably be implemented in a bipolar technology.

7.1.4 High Speed Receivers

Each of the systems will derive timing information from the 60 MHz clock or from other reference timing signals, and one of the important tasks is to determine the optimal method for distributing these signals. It is likely that these signals will be distributed locally as differential signals of voltage swing $\pm$200–300 mV. Each chip must then have a receiver for translating this signal into on-chip voltage levels. For some applications, such as drift time measurement the risetimes must be sufficiently fast to preserve timing accuracies of 1 nsec. For many other applications, such as driving on chip bunch counters or the switching speed of low accuracy analog memories the timing accuracy can be less. However, it is worth noting that for high precision voltage sampling timing reproducibilities as small as 0.05–0.1 nsec may be required to prevent distortion. These high speed receivers typically consume significant amounts of power and in applications where power dissipation is very important the receivers must be carefully optimized for minimal power dissipation and adequate speed. A prototype high speed CMOS receiver for the TVC system has been designed and fabricated; modifications of this design, as well as new designs, will be evaluated for each of the CMOS chips requiring timing information in the other systems.

7.1.5 Bus Drivers

For each of the systems incorporating on-chip ADC's, or which produce directly digital information, bus drivers are required to transmit this information during readout. While the design of such bus drivers is not particularly critical for many conventional applications, the requirements of minimal power dissipation and minimal generation of noise imply that these drivers must be carefully designed for the SSC environment. Low voltage levels ($\pm$200–300 mV) will probably be utilized and the signal risetimes should be controlled to be the minimum required for the designed readout speed. For some applications serious consideration may need to be given to the possibility of differential buses.

7.1.6 Analog Memories

As noted above the data for any system must be stored during the 0.5–2 μs ec required for the first level trigger decision. While flash ADC systems operating at this speed will probably exist with at least 10 bit accuracy, the high power required both for the ADC and for the subsequent storage imply that use of FADC's will be impossible for systems where very low power dissipation is required and uneconomic even in those applications where high power dissipation is allowed. Since the Level 1 storage is of relatively short duration, analog memory units should be well suited to this application. For silicon strip detectors and for pad readout of wire chambers, radiation hard (1 MRad) AMU's of 8-9 bit accuracy will be necessary. For the calorimeter, dynamic range of 11-12 bit accuracy will be required (assuming a "split-scale" or "high-low" readout system is utilized); fortunately it is likely that the circuits will not need to be radiation hardened.

For the Level 2 buffering, storage times will be much longer, of order $10 - -50\,\mu$sec. It is quite possible that digital storage might be utilized at this level since the analog to conversion rate required when transferring data from Level 1 to Level 2 buffers should not exceed 1 MHz. However, in applications where power dissipation is extremely critical and only 8–9 bit accuracy is required, analog storage may be utilized for the Level 2 buffering as well.

7.1.7 Additional Circuits of General Utility

There are a considerable number of additional circuits, or circuit techniques, which will be required. These include:

1. RAM's
2. FIFO's
3. Logic for event selection from Level 2 Buffers
4. Low power fast ADC's

Implementations of these in one system will often find application in the other sytems.

7.2 Radiation Effects

A number of the electronic systems, in particular those for the readout of wire chambers and silicon track detectors located near the vertex, and preamplifiers for the calorimeter if they are located inside the calorimeter, must be radiation hard.

The required total dose hardness due to ionizing radiation for silicon or wire chamber detectors varies from less than 100 krad at radii greater than 1 m to the order of 1 MRad for systems within 15–20 cm. It should be noted that considerable conservatism should be allowed both because of uncertainties in the estimates of the radiation level and also because of the high reliability required for the total system. Neutron doses are estimated to be relatively uniform over the entire volume inside the calorimeter (except perhaps for very near the forward calorimeter where they may be higher) and approach 10^{14} n/cm^2 over ten years of running.

The front end electronics for drift time measurement will certainly be implemented in a bipolar technology. For the pad readout of wire chambers and for silicon strip detectors, the front end may be bipolar or CMOS depending on whether the shaping time used is closer to 15–30 nsec or 50–70 nsec. Initial measurements on several bipolar technologies have indicated that there are relatively advanced bipolar technologies which are hard to total doses of 1 MRad and neutron doses of 10^{13}–10^{14} n/cm^2. For example, Fig. 7.1 shows the degradation in beta for an NTT process. Preliminary measurements

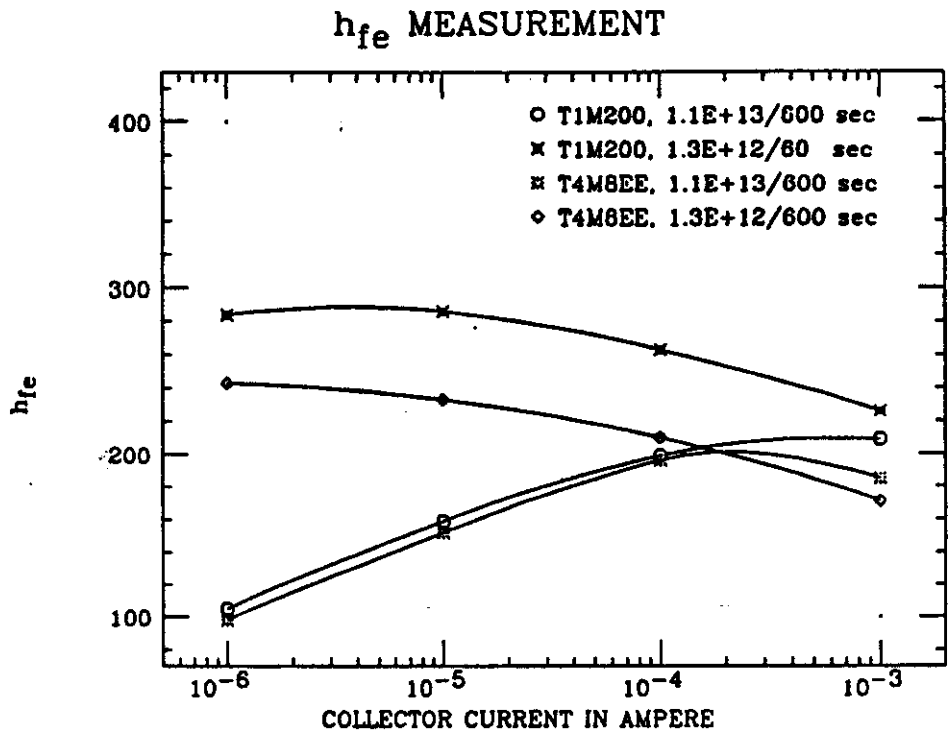


Figure 7.1: Measurements showing the degradation in h_{fe} after exposure to neutrons for some bipolar transistors produced in the NTT SST process.

for an AT&T process show little change in beta for n fluxes of $10^{14}/cm^2$. While more measurements must be made, it appears quite possible that one of these processes will provide sufficient radiation resistance for wire chamber and silicon readout systems at distances from the beam greater than 15–20 cm. However, it remains to be demonstrated that one has sufficient radiation resistance for the most advanced technologies, i.e., those which provide $f_t > 5$ GHz at collector currents of 50–200 μA. It is with these technologies that the lowest power dissipation can be achieved. We therefore intend to systematically study the radiation resistance of a number of advanced bipolar technologies.

As far as CMOS is concerned, there exist several foundries with radiation hard processes. The process of United Technologies Microelectronics Center (UTMC) is particularly encouraging with threshold voltage shifts of only a few hundred milliVolts after 1 Mrad doses of ^{60}Co gamma rays, and almost no voltage shifts (< 20 mV) after neutron exposures of 9×10^{14} n/cm^2. Thus the UTMC process should provide sufficient radiation resistance for the digital portion of any of the circuits being considered and shows promise of being suitable for analog circuits that do not require two layers of polysilicon. However this process, and most of the other rad-hard CMOS processes, are in general intended only for digital circuits and it is not yet clear whether they are really suitable for analog circuits. In particular, the utility of the process for analog memory circuits and the behavior of the transistor noise as a function of radiation is unknown at this time. We therefore plan to perform a systematic and complete evaluation of this and other rad-hard CMOS processes. The performance of transistors of varying w/l ratios will be characterized as a function of radiation. In addition to the usual measurements of threshold voltage shift, particular attention will be paid to characteristics important for analog design such as transistor noise, threshold matching for identical devices, degradation of transconductance, increase in output conductance, leakage currents, etc. It is particularly important to thoroughly understand the sources of all leakage currents because of the interest in analog storage.

The characteristics of the capacitors and resistors will also be measured and special devices (such as gated diodes) will be included so that one may understand the buildup of oxide charge and the interface state density. Important subcircuits such as current sources,

charge preamplifiers, operational amplifiers, and simple switched capacitor circuits will be evaluated so that one may more readily predict the performance of more complicated circuits. Finally, it is intended that full prototypes of readout systems for wire chambers and silicon strip detectors will be fabricated and tested for radiation resistance.

The preamplifiers for liquid ionization calorimeters must withstand total doses of nearly 10 Mrad if they are located internal to the calorimeter, which is quite likely if the optimal speed and noise is to be obtained. For this application, JFET's are particularly appropriate both because of their low noise and also because they are intrinsically very resistant to radiation.

Given a technology which is relatively radiation resistant, one must still exploit circuit design techniques which further increase the hardness of the final design. This will be true both for analog circuit functions and for digital functions. Again we note that techniques that work for one system will often provide solutions in other systems as well. It is particularly important to investigate single event upset (SEU) since the spurious modification of information in counters and address pointers can compromise the data for many events. Thus different conceptual designs for the front end readout architecture must be evaluated in terms of their overall functional resistance to radiation.

7.3 Other Common Development Issues

There are a number of other areas of development that are common to each of the systems. We simply list them here without commenting in detail on each of them. They include:

1. Design Techniques for minimizing power and crosstalk
2. Fault Analysis and Reliability
3. Packaging
4. Substrates for chip mounting
5. New Interconnect Technologies
6. Computer Aided Engineering: compatibility, inclusion of new technology files, etc.

8 LEVEL 1 TRIGGER

An integral part of the front end electronics is the generation of the Level 1 trigger; by this we mean the first level of decision-making on the basis of which a significant number of events are rejected. While considerable work needs to be done to fully define and optimize the Level 1 trigger system, a reasonable consensus has developed concerning a number of its basic characteristics. We outline those assumptions that we believe are reasonably well founded at the present time.

1. Goal: to provide in a time of 1–2 μsec a decision as to whether a given event is interesting or not. The acceptance rate will be 0.001–0.01.

2. It will be a synchronized, pipelined system operating at the crossing frequency of 60 MHz.

3. The delay between the time of an interaction and the decision time for that event will be fixed during operation. However, the capability may exist in the front end chips to select one of several different delay times. We anticipate that the trigger time would be changed only infrequently, e.g. if a major upgrade or modification of the trigger system took place.

4. As currently envisioned, the primary information input to the Level 1 trigger will concern the possible existence in an event of

   (a) Sum E_T

   (b) Missing E_T

   (c) Jets (clusters of energy)

   (d) Electrons

   (e) Muons

5. The Level 1 trigger should be as simple and unbiased as possible, subject to the constraint that sufficient rejection of uninteresting events takes place. We note that portions of the Level 1 system, particularly regarding the generations of signals, will be rather unaccessible.

6. Each system delivering inputs to Level 1 (e.g. calorimeter, track segments, preradiators or TRD for electron identification, segments in muon chambers, or scintillation counters in muon systems) must either possess timing information accurate to 1 crossing or possess a very strong correlation with another system that has accurate timing information.

7. The minimal system of inputs would consist of information from the calorimeter sufficient for including objects (a)–(d) in (4) above plus information from the muon system.

In this proposal we will concentrate on the minimal Level 1 triggers required to keep objects (a)–(d) while achieving sufficient rejection. That is, we do not propose to investigate at this time a muon trigger system. The emphasis then is on the calorimeter triggers, plus the development of segments or other track-finding information if it is required for the Level 1 trigger. However, it may also be that certain types of information should be generated in the front end chips for the Level 2 trigger, even though this information is not used in Level 1. We will consider the generation of this information. We do not propose to consider in any detail the nature of Level 2 processors or the types of algorithms that might be used in Level 2 triggers.

8.1 Calorimeter Triggers

The calorimeter will provide the basis for most of the Level 1 triggers, in particular those based on the Sum E_T in the calorimeter, the missing E_T as measured in the calorimeter, jet clusters, and electron candidates. For the purposes of discussion we will assume a segmentation in the EM calorimeter of $\Delta\eta \times \Delta\phi = 0.03 \times 0.03$ and in the HAD calorimeter of 0.06×0.06; a segmentation of this order, while by no means final, has been supported by a number of studies. We also assume three longitudinal segments in the EM calorimeter and two in the HAD calorimeter. For a calorimeter that spans $|\eta| < 5.0$, this results in a total of 195 510 channels. Given these inputs, a wide variety of triggering schemes is possible. We outline here one of the simplest configurations.

We assume initially that a granularity of 0.12×0.12 in $\Delta\eta \times \Delta\phi$ and one longitudinal segment for the hadronic and electromagnetic is sufficient for triggering. Thus there will

be a Level 1 sum over 48 of the EM towers and 8 of the HAD towers; this yields 3491 trigger towers for both the EM and HAD calorimeters. The primary electron trigger will consist of demanding a minimum energy in a single tower coupled with the requirement that the ratio of energy in the hadronic and electromagnetic compartments, H/EM, is less than a certain fraction, e.g. 0.125. Preliminary, but reasonably detailed studies, have indicated that these simple criteria should be sufficient for the Level 1 electron trigger. It is nonetheless interesting to see what additional gain would be obtained from including some tracking information, e.g. the existence of a high Pt track segment pointing to the calorimeter cluster in the central rapidity region ($|\eta| < 1.5$) and the existence of a track segment or a minimal number of hits in a "road" from the calorimeter cluster to the interaction region for larger rapidities ($1.5 < |\eta| < 3$). The primary function of any track requirement at Level 1 is to eliminate triggers from pi-zeros.

To determine the $\sum E_T$ and missing E_T triggers, it is necessary to sum over the entire calorimeter. We intend to investigate a number of different techniques for performing these sums. As an example three different options are:

1. "Shift register sum"—In this scheme the quantity of interest for each trigger tower, e.g. E, $E \sin\theta$, $E \sin\theta \cos\phi$ is passed to the neighboring tower, which in turn passes the partial sum to the next tower. The system would be clocked at the 60 MHz clock rate and one could sum initially over slices of constant η or ϕ.

2. "Star" sum at the detector—In this scheme, one might sum four neighboring towers, then sum those results, four at a time, and repeat this until the total sum is derived.

3. Sum at central Level 1 location—In this approach, which may well be the simplest and most flexible, all information of the minimal trigger granularity would be sent directly to a central Level 1 trigger system and all further sums and processing would take place there. For the above simple example, this would require the transmission of the EM and HAD E_T sums from each of the 3491 towers. This approach has the advantage that all of the secondary sum and additional processing logic is located in a relatively accessible location. This provides the maximum flexibility for modifications to the Level 1 trigger.

For each of these configurations (as well as other possiblities), one can readily evaluate the total time for generation of the Level 1 trigger, total capacitance at each stage of summation, requirements on intermediate analog and digital sums, cables, etc.

9 Interaction with the Data Acqusition System

9.1 Introduction

The Front End (FE) Electronics design discussed above cannot be considered separately from the Data Aquisition (DAQ) System, which after a Level 2 trigger decision moves the digitized data from the detector front end to any higher Level trigger systems and the eventual storage media. The scope of this proposal focuses on the design and prototyping of the FE electronics and excludes a detailed study of DAQ architectures and implementation. However, considerable attention has to be paid to the interface between the FE electronics and the DAQ system so that the resulting read out system performs in an optimal manner.

Different conceptual designs of DAQ systems for SSC detectors have been discussed at several recent workshops. Most of the designs assume that the data for an event is available in digitized form after the event has passed a Level 2 trigger. Furthermore, it is assumed that the data is stored in components that are distributed over the detector and that these data must be collected into a coherent event record by the DAQ system. A conceptual design for a DAQ system has to address the details of the interaction of these components with the trigger and the other devices in the data collection architecture. This interaction impacts the complexity of the resulting system, as well as its overall bandwidth and flexibility.

As has been pointed out earlier, the design options for the FE system influence the design of the DAQ system. It is imperative that the constrains implied by the FE electronics design on different DAQ architectures be understood, and design options that have undesirable implications on the DAQ system be avoided. It will almost certainly not be possible to design a FE electronics system without also making design choices for the DAQ system as well. However, the evaluation of the implications of the FE electronics design

on the DAQ architecture will ensure that a complete readout system with the desired capabilities can be constructed using the FE technology resulting from this work. We propose to make these evaluations by developing a detailed simulation model of the FE system design, along with higher-level models for those DAQ architectures that appear most promising.

9.2 Models for DAQ Systems

There are various system-wide issues that affect both the FE and the DAQ systems, primary among them being the definition of the control signals that are exchanged among the components of the readout system, and the manner in which the system is controlled, initialized, and diagnosed. Experience with the CDF and other large readout systems has shown that it is difficult to reliably estimate how the performance of the data collection system is effected when the specifications of the system components are modified. This is particularly true in an SSC DAQ system, which is a complex, multi-stage pipeline. The behavior of such systems, however, can be accurately characterized by stochastic simulations that embody the performance characteristics of each component in the system.

The DAQ systems that have been considered for SSC detectors have many features in common:

1. they employ a high degree of parallelism in the readout of an event in order to achieve the necessary data bandwidths;
2. they separate the data pathways from those used for control; and
3. they embody some level of data-driven control, *ie* control signals are minimized by having the existence of data ready for transfer be the condition used to control the transfer of data from one component in the system to the next.

However, there are still many possible conceptual DAQ architectures and implementations. This arises from the uncertainties in many of the crucial performance parameters of the readout system, and because the relevant technology is rapidly evolving. Examples of these uncertainties are:

1. the rate of events that have to be moved through the DAQ system, which is defined by the rejection used at the Level 2 trigger system;

2. the amount of data associated with each event, which is determined by details of the detector and the amount of data processing that takes place in the FE electronics;

3. the technology available for data transmission, which is rapidly evolving with the advent of low cost optical fiber devices; and

4. the cost of real-time information processing, which is falling rapidly with the introduction of special processors for data manipulation (Digital Signal Processors, or DSP's) and general purpose microprocessors.

However, despite these uncertainties, the design of the FE electronics must be placed in the context of a design for the entire readout system, including a conceptual design for the DAQ system. This will ensure that the interaction of the FE and DAQ systems is well understood and the performance of the readout system is reliably characterized. The intent is not to design the "optimal" DAQ system, but to develop a reference design for the DAQ system that clearly specifies the interface between the FE electronics and the rest of the data collection system, and indicates how the interaction between the these systems takes place.

9.3 Simulation of DAQ and FE Architectures

Advancements in the field of simulation and behavioral modelling now provide the ability to take a specification for a complex system and model it at various levels of detail. Commercial programs (such as Verilog) can be employed to model the behavior and performance of different conceptual designs for a DAQ system with a given set of design parameters for the FE electronics. The FE system itself is already sufficiently complex that it requires simulation studies of a similar nature. Since it is possible to model different parts of a system with different levels of detail, such a simulation naturally would evolve from a very high-level "black-box" specification of the basic components to a detailed specification of the FE electronics leaving the DAQ system specification as general as possible.

As an example of this sort of approach, Fig. 2.1 and Fig. 2.3 show schematics of a conceptual design for a readout system that incorporates the basic philosophy for the FE electronics discussed earlier and a data-driven architecture for the DAQ system that employs an Event Builder, which collects the data from the DCC's and passes it to a Level 3 trigger system consisting of a farm of processors. The figures also show a subset of the basic control signals that have to be exchanged between the components. The digitized data assembled in the DDC's is divided into packets that contain various book-keeping features such as event number and detector ID. As soon as a data packet is ready to be sent from the DCC's, it is shipped up to the Event Builder where the entire event record is assembled and then written into one of the Level 3 processors. An example of a rather different architecture is shown in Fig. 9.1, which is a schematic of the CDF readout system.

Various schemes for implementing the control logic and data flow in the FE system will be evaluated using several different conceptual DAQ architectures. The behavorial models of these systems will quantify the performance of each system and allow one to explore other issues such as fault-tolerance and complexity. In this way, it will be possible to make reasonable choices for the FE electronics design and understand the implication of these choices on the DAQ architecture. From the simulation of the initial conceptual design, more details of the FE electronics would be incorporated into the simulation as the design develops, leading to as complete a simulation of the FE electronics as desired. At this stage, more details of the different DAQ systems could be included as specific designs for such systems emerge.

We intend to form liasons with the other groups that have already started developing simulation models, as well as those groups that are developing Level 1 and Level 2 trigger systems. In particular, we plan to work closely with the group at the University of Illinois that has already begun the task of developing high-level simulations of SSC data collection systems.

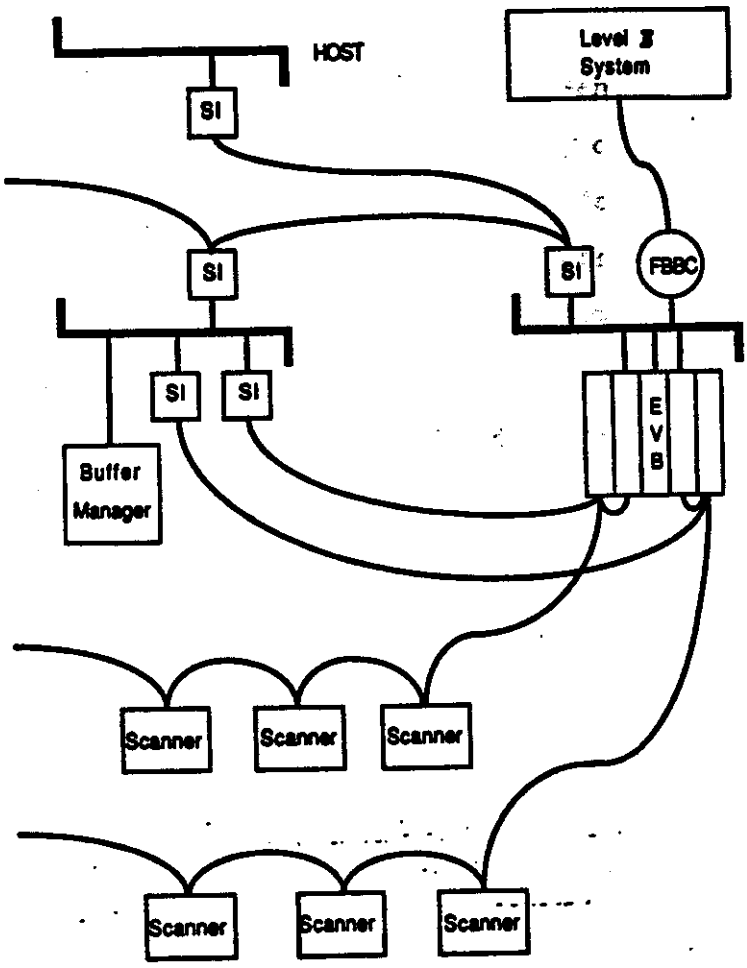


Figure 9.1: The CDF data acquisition system

10 Collaboration with Industry

Development of the electronics outlined will require a broad [illegible] industry in a number of areas.

10.1 Foundry Access

The most important initial interaction with industry, which is essential to the successful realization of the goals outlined above, is access to a wide variety of advanced semiconductor processes. Fortunately industry has proven quite receptive to the development of the electronics outlined above, and many of the important connections have already been established. The participants in this proposal currently have direct [illegible] llowing technologies:

1. AT&T 2 micron, complementary bipolar: 4 GHz npn and 2.5 GHz pnp
2. AT&T 0.9 micron CMOS, double poly, double metal
3. Plessey 1 micron bipolar: 18 GHz ft npn
4. UTMC 1.2 micron rad-hard CMOS
5. INTERFET, diffused junction JFETs, dielectrically isolated devices.
6. Bipolarics
7. MOSIS

In addition, through cooperation with Chuck Britton at Oak Ridge National Laboratory and H. Ikeda at KEK we have some access to prototype circuits manufa[illegible] with the following processes:

8. Harris rad hard CMOS
9. NTT SST Bipolar

The above processes are sufficient for design and prototyping of non rad[illegible]d versions of each of the circuits outlined above and may in fact be suitable for pr[illegible]tion in a number of cases. In particular the AT&T CMOS process is designed to [illegible] an analog

process and should be an excellent choice for operational amplifiers and analog memory units for the calorimeter system. The AT&T bipolar process, with the capability of high f_t npn and pnp transistors, should be excellent for the design of the summing amplifiers for the calorimetry. A new AT&T process promises even higher performance, 12 GHz npn and 5 GHz pnp transistors; however this higher performance is probably not necessary for the calorimeter shaping times.

It was noted above that at least one of these bipolar processes may even be sufficiently radiation resistant for use in applications for drift chambers and silicon detectors down to radii of 15–20 cm. However, as it is not yet known whether the most advanced bipolar processes are sufficiently hard, we intend to pursue contacts with a number of other foundries. In particular one small company, Bipolarics, has a very fast process and is quite willing (given support to cover the costs) to tune the process to achieve the maximum radiation hardness, as well as the optimal transistor parameters for the applications of high energy physics. BiCMOS may be the most advantageous (i.e. lowest power dissipation) technology for readout of pad chambers and silicon strips; we therefore plan to contact a number of companies that have advanced BiCMOS processes. Leading candidates are AT&T, National, Texas Instruments, and Signetics.

A close collaboraton with INTERFET is underway to develop integrated devices with noise performance approaching that of discrete devices and to produce a fully monolithic JFET preamplifier.

10.2 Circuit Design and Testing

To date much of the design of SSC related circuits has been performed by scientists within the high energy physics community. However there have also been a number of successful collaborations in which companies have participated closely in the design. We feel that it is important for this form of collaboration to increase during the next 1–2 years for a number of reasons:

1. Understanding within the particle physics community of the performance required for the front end electronics, and of the capabilities of the leading semiconductor technologies, has increased very significantly in the last 2 years. Thus one is much

closer to being able to write a set of specifications for circuits or systems that is both sufficient in terms of performance and realistic in terms of what technology can deliver. One of our goals is to develop at an early stage a set of specifications for many of the subcircuits; this greatly facilitates communication with industry and the letting of subcontracts.

2. Emphasis on front end circuit design will shift more and more during the next one or two years from particular subcircuits, such as preamplifiers or analog memory units, to the system level design. For systems such as the wire chamber or silicon strip readout, which require integration of the full system on one or two chips, the circuits become relatively complex. More sophisticated software is required for the simulation of mixed analog-digital circuits; design verification, documentation, and testing become more difficult; and layout becomes more tedious. While most of the institutions in the collaboration will have adequate access to the software and hardware necessary, collaboration with companies which have a high level of expertise in this area could significantly speed up some of the development. It also provides a good opportunity to begin the "industrialization" process and to learn which companies are the best candidates to ultimately deliver production quantities of circuits of systems for experiments.

3. Circuit designs must ultimately be evaluated not only in terms of performance for a prototype, but also in terms of reliability, testability (how easy it is to fully test all aspects of the design) , and manufacturability (yield, insensitivity to process variations, suitability for second source contracts, etc). This is an area that few of the many custom circuit projects in high energy physics has seriously addressed.

4. Systems ultimately consist not just of chips, but of substrates on which chips are mounted and interconnected. Most of the detector systems will benefit from, if not require, relatively advanced technologies for packaging, bonding, and interconnects. Examples of technologies that will be particularly important are "flip-chip" bonding, other very low capacitance bonding techniques, and new materials with low dielectric constant for minimal capacitance interconnects.

It is our intent, once reasonably accurate specifications are developed, to solicit proposals from a number of companies for the development of both subcircuits and system designs. Examples of subcircuits for which it might be particularly appropriate to solicit industry designs are very low power, high unity-gain-frequency, operational amplifiers in submicron processes (both bipolar and CMOS, rad hard and not), large dynamic range analog memory units, low power, 11–12 bit, pipelined, 1–2 MHz conversion rate ADC's (for the case that Level 2 buffering is digital), and 10–11bit, 60 MHz, flash ADC's for the calorimeter Level 1 trigger system.

11 Interaction with other R&D Projects (Generic & Subsystems)

This project will depend on close interaction with other R&D efforts both in the program on Generic Detectors R&D and on Detector Subsystems R&D.

Closely related Generic Detector R&D projects are:

1. *SSC Detector Research and Development*
   Brookhaven National Laboratory (BNL)
   - Readout for Fast Calorimetry
     S. Rescia, V. Radeka, and L. Rogers
   - Wire Chambers with Interpolating Pad Readout
     B. Yu, et al.
   - Cylindrical Semiconductor Drift Chambers, Resistive Strip Detectors with Charge Division
     H. Kraner, Z. Li, and P. Rehak
   - Silicon Drift Detectors with Integrated Electronics, Sparse Write-In Readout
     P. Rehak, S. Rescia, and V. Radeka
   - Basic Properties of Detection Media
     H. Kraner and Z. Li
   - SSC Event Simulation
     F. Paige and S. Protopopescu

2. *Electronics R&D for Detectors at High Luminosity, High Energy Colliders*

   H. H. Williams, University of Pennsylvania

   V. Radeka and S. Rescia, Brookhaven National Laboratory

   W. Sansen, Katholieke Univ., Leuven

3. *A Study of Triggering Electronics Requirements for a Liquid Ionization Calorimeter*

   W. Cleland and J. Thompson, University of Pittsburgh

4. *Proposal for a Comparative Engineering Study of Cryostat Systems for Generic Hermetic Liquid Argon Calorimeters*

   M. Marx, et al., SUNY, Stony Brook

5. *SSC Detector R&D Proposal*

   Lawrence Berkeley Laboratory (LBL)

   •Semiconductor Detector and Integrated Electronics Development

   L. Bosisio, D. Nygren, and H. Spieler

   •Study of Fiber Optics for Application to SSC Detector Systems

   A. Clark, et al.

   •Fast Hermetic Calorimetry Using Warm Liquids

   C. Klopfenstein et al.

6. *Proposal to Investigate Purity in Warm Liquid Ionization Media*

   R. J. Hollebeek, University of Pennsylvania

7. *Proposal to Study Readout and Triggering Architecture for SSC Calorimeters*

   F. Sciulli, et al., Columbia University

Results from these studies will be essential to define the requirements and specifications on electronic readout circuits and to determine some basic limits (noise, speed, power and radiation resistance).

We expect that a number of proposals for Detector Subsystems R&D presently in preparation will be closely related to readout electronics development in this project. The most important ones known to us at the writing of this proposal are:

1. Research and Development of a Liquid Argon Calorimeter for the SSC

   H. A. Gordon, G. S. Abrams and collaborators, BNL, LBL and $\approx$ 10 other institutions.

2. Research and Development of a Warm Liquid Calorimeter for the SSC
   M. Pripstein, et al., LBL and collaborating institutions.
3. SSC Detector Subsystem Proposal for Silicon Calorimetry
   J. Russ, et al., Carnegie Mellon University and collaborating institutions.
4. Subsystem Proposal on Scintillator Calorimetry
   .....
5. Subsystem Proposal on Triggering and Data Acquisition
6. Subsystem Proposal on Transition Radiation Detectors
   S. Whitaker, et al., Boston Univ. and collaborating institutions.

Close interaction will be maintained with these projects. Some members of our collaboration will participate either directly or on a consultative basis in these projects. Design decisions in some cases will have to be made jointly between our project and one or more of the other projects.

12 Manpower, Milestones, and Budget

12.1 Manpower

The requested support for manpower, circuit processing, subcontracts, materials , and equipment is summarized by task and by institution in Table 12.1. Here we discuss briefly the responsibilities of each institution and note the total manpower to be dedicated to each task, including that for which no support is requested. It is important to realize that one of the primary purposes of this collaborative effort is realize the benefits of numerous experts contributing ideas and solutions to various problems. Thus many people will contribute to nearly all of the tasks. Nonetheless certain individuals and institutions will have primary responsibility for particular tasks and we note that in the following discussion.

Front End Architecture and System Level Design

Design and studies of the system level architecture will be carried out by a number of individuals from several of the institutions. At the logic level, the primary contribution will be from F. Kirsten (plus possibly an additional person) at LBL, R. Van Berg at Penn,

and engineers from Rutherford and Oxford. A number of physicists will undoubtedly contribute ideas concerning the overall data flow, particularly P. Sinervo and K. Ragan at Penn who will perform simulations of the front end data collection including representation of event building at the conceptual design level; it is anticipated that a new physicist joining LBL will contribute significantly to this effort. There will be close interaction with Bill Sippach at Columbia, who (with support from the Generic R&D program) is thinking about possible architectures and with Andy Lankford at SLAC.

Calorimeter Front End

The primary responsibility for the preamplifiers, in particular for the development of radiation hard, monolithic, JFET preamplifiers, will be at BNL. As noted below this development is being funded via the Generic SSC R&D program, except for the essential item of funds for a subcontract with INTERFET which are requested in this proposal. There will be some consideration of alternative designs at LBL and particularly at Harvard where J. Oliver will evaluate whether bipolar transistors offer comparable noise performance at significantly lower power if one were unable to use transformer matching.

Approximately 2.5 full time engineers at LBL (S. Kleinfelder plus additional persons) will work on the CMOS amplifiers and analog memory for readout of the calorimeters. Some input will also be made by V. Budihartono at Penn (a student supported by Generic R&D) who has been working on operational amplifiers in short channel CMOS. We will consider letting a small subcontract with industry for parallel design efforts in high speed operational amplifiers in very short channel processes (less than 1 micron).

The design, prototyping, and testing of the fast bipolar summing and shaping amplifiers will be undertaken by BNL (L. Rogers as 0.5 FTE plus 0.5 FTE from new positions). V. Radeka and S. Rescia will participate significantly in the conceptual design. Studies of the calibration and gain control will also be undertaken at BNL (1 FTE).

Prior to detailed design of the individual circuits, the desired characteristic s for the calorimeter system, in terms of shaping time, dynamic range, relevant trigger sums, etc. must be specified. This requires rather detailed simulation of events, both signal and background, with careful attention paid to accurate representation of thermal noise and pileup. J. Siegrist and M. Levy at LBL will contribute significantly to this work, with

help from other physicists at Penn, LBL, Harvard, and Oxford. Close interaction will be maintained with W. Cleland et al. at Pittsburgh where a study of precisely these issues is being undertaken with support from the Generic R&D program. We will also pay close attention to similar studies that may be carried out by other physicists in the community.

Readout of Proportional Chambers with Cathode Pads

The design of the readout circuitry for cathode pads will be executed by Arup Bhattacharya (0.75 FTE) and an additional engineer (0.25 FTE) at BNL. It is anticipated that this circuit will be implemented in CMOS since the low occupancy allows the use of relatively long shaping times (> 50 nsec) and the detector capacitance is small (2–4 pF). This circuit will require the use of a radiation hard CMOS process; effort concerning identification of a suitable process and radiation tests of the circuitry is discussed below. A number of the ideas developed for the drift time measurement system for wire chambers are likely to be relevant to this project and personnel from Penn will contribute suggestions for the overall architectural design. Personnel from Rutherford Lab are also interested in pad chamber readout and are likely to contribute ideas.

Drift Chamber Electronics

The development of a complete radiation hard system for drift time measurement will be carried out primarily at the University of Pennsylvania; a new full time engineer will be required for this task which requires advanced radiation hard circuits in two different technologies, bipolar and CMOS. This system will include the first implementation of the full Level 1 storage, Level 2 storage, and readout control and therefore involves extensive digital and analog design. The initial development of non radiation hard versions of the preamplifier, shaping amplifier and discriminator is supported by existing HEP funds under redirection of effort (0.3 FTE for F. M. Newcomer) and by Generic R&D (S. Tedja, EE student plus 0.75 month for J. Van der Spiegel, EE faculty). The initial development of a non rad hard TVC plus Level 1 storage and A/D is supported by redirection of effort (0.25 FTE for R. Van Berg) and Generic R&D (V. Budihartono, EE student at Pennsylvania, W. Eykmans, EE student at Catholic University of Leuven, and 0.75 month for J. Van der Spiegel). Development of the full rad hard system requires re-evaluation of the design of each of the pieces, both analog and digital, a completely new layout,

and considerable amount of new digital design for implementation of the Level 2 storage and readout control. Effort required for the evaluation of rad hard CMOS and bipolar processes is discussed below.

Silicon Strip Readout

Design of a complete system for readout of silicon strips will be carried out at Rutherford Laboratory by P. Seller and M. French. It should be noted that P. Seller designed the silicon strip readout for one of the LEP experiments. Emphasis will be on analog readout of the strips and on very low power, of order 1 mW per channel for the entire system. A recent preamplifier design by P. Jarron achieves nearly the desired performance- 1000 electrons noise, shaping time of 20 nsec, detector capacitance 5 pF- with only 1 mW power consumption. The low occupancy of a silicon strip system should allow longer shaping times (e.g. approximately 50–70 nsec) and hence still lower power. With signal to noise of 10:1, the time resolution should still be adequate to uniquely identify signals with a given bunch crossing. To accomplish very low power for the Level 1 and Level 2 buffering it will be necessary to use techniques (e.g. not moving charge until readout) developed for the drift chamber system; thus there will be close collaboration between Rutherford Lab and the University of Pennsylvania.

For shaping times in the vicinity of 40–70 nsec, it is not clear whether CMOS or bipolar will be superior for the preamplifier. A student from Pennsylvania will consider BiCMOS designs to see whether they offer superior performance to all CMOS. This will include comparisons of bipolar versus CMOS for very low power comparators and for the amplifiers required to drive the analog memory.

Common Electronics Issues

Circuits

Much of the interaction between the various participants has already been referred to above. Briefly summarizing, we note that S. Kleinfelder, V. Radeka, S. Rescia, M. Newcomer, S. Tedja, and P. Seller all have considerable experience in the design of charge preamplifiers. Students at the University of Leuven have performed a careful analysis of fast comparators and high speed receivers (in CMOS), optimizing them for minimum power (given the desired performance and evaluating the sensitivity to process variation).

S. Kleinfelder and personnel at Rutherford have some experience with analog memories, and V. Budihartono and students at Leuven have experience with CMOS operational amplifiers. (These students at Leuven are not working on any of the projects on this proposal, but are available for consultation). V. Budihartono will continue to work on limited dynamic range rad hard operational amplifiers. A new engineer at LBL will concentrate on the large dynamic range, non rad hard amplifiers required for the calorimeter system).

Evaluation of Radiation Hard Processes and Circuits

Extensive effort will be required for the evaluation of the radiation resistance of devices and circuits for JFET, CMOS, bipolar, and BiCMOS processes. At BNL, 1 FTE will be required for the testing and evaluation of JFETs, low noise transistors in all of the technologies, and for the specific subcircuits related to the pad chamber readout. At Penn 1 FTE (either a PhD or a Master's in EE) plus 1 student will be dedicated to the systematic evaluation of bipolar, CMOS, and BiCMOS processes. It should be noted that particularly for the rad hard CMOS processes very extensive investigation will be required to evaluate the suitability of these processes for analog design as they are invariably intended primarily for digital. This includes evaluation of the basic transistors (including spice model parametrization, leakage currents, threshold matching, noise, etc.) and characterization of capacitors for several processes. It will also be necessary to determine the stability of these parameters from run to run.

Level 1 Triggers

As alluded to briefly in the discussion above on parameters of the calorimeter system, extensive studies will be carried out on the Level 1 calorimeter trigger–which sums, ratios, etc of the energy deposition in the electromagnetic and hadronic calorimeter sections will yield the simplest, yet most effective trigger. J. Siegrist, M. Levy, P. Sinervo and other physicists at the institutions will contribute significantly to this work. We will also interact closely with W. Cleland et al at Pittsburgh and with M. Campbell et al at Michigan and with physicists at the University of Chicago who are interested in carrying out similar studies.

Data Acquisition Simulation

The simulation of the front end data acquisition system will be done primarily by P. Sinervo and K. Ragan at the University of Pennsylvania with probable participation from LBL. We will also collaborate closely with Andy Lankford (SLAC) and others who are interested in similar studies.

Interaction between Generic R&D and Subsystem R&D at BNL

Support for 4 engineers is requested in this subsystem proposal. From the existing staff Arup Bhattacharya will participate as 0.75 FTE and Lee Rogers as 0.5 FTE. The remaining 2.75 FTE will have to come from new positions. This is appropriate and necessary to strengthen the capabilities for monolithic circuit design for the SSC program. These positions are needed for technical work, such as monolithic circuit design, layout, simulation, electrical testing, and radiation effects testing.

The conceptual design, design studies and research into new components and circuits will be conducted mostly in the generic R&D program. The overall effort will be guided by V. Radeka (0.5 FTE) and S. Rescia (0.8 FTE). Others participating in this part of the program concerned with electronics are D. Stephani (0.5 FTE) and Z. Li (0.25 FTE). The total BNL generic R&D program involves a scientific and engineering effort of 11.2 FTE, partially funded at a level of 600K$. Readout Methods in Fast Calorimetry and wire chambers with Interpolating Pad Readout represent about one third of this total effort. A strong and well equipped support infrastructure of BNL is indispensable for both the generic and the subsystems R&D programs, and it will make a substantial contribution to both programs.

12.2 Milestones

We list a number of the important milestones. The times shown are the elapsed time from the start of the program (i.e., from the time of initial funding).

1. General Architectural Design of the Front-End System

Protocols for synchronizing and controlling the data collection functions of front-end ICs	6 months–1 yr
Protocols for collecting digital data from front-end ICs	1–2 yrs

2. Calorimetry: Preamplifier, Triggering, and Calibration

2.1 JFET and preamplifier development

Tests of prototype JFETS for operation in liquid argon	1 yr
Test prototype circuits of dielectrically isolated JFET monolithic preamplifier for operation in liquid Argon;	1 yr
improved design prototypes	2 yrs

2.2 Fast summing amplifiers and shapers

Summing amplifiers, first prototypes	1 yr
Improved design prototypes	2 yrs
Shaping amplifiers	2 yrs

2.3 Calibration system and gain control

Charge injection and pulse distribution circuits	1 yr
Pulser control and gain control circuits	2 yrs

3. Calorimetry: Data Storage and Readout

Definition of performance requirements (dynamic range, linearity, speed, etc.) as dictated by liquid calorimetry	6 months
Studies of IC circuit technologies for analog data storage and processing	6–9 months
Specifications for data storage/processing electronics	6–9 months
Integrated circuit implementations (design, prototype, and test)	
Initial prototypes of subcircuits	12–15 months
Improved integrated system	18–24 months

4. Interpolating Pad Chamber Readout

Prototypes of preamplifier, shaper and multiplexing circuits	1 yr
Prototypes of Storage and Sparsing circuits	3 yrs

5. Drift Time Measurement System

Studies of the architecture for Interaction with Level 2 trigger and for readout; design of individual digital subcircuits; studies of digital cells available in rad hard processes; reevaluation of analog subcircuits based on preliminary information on behavior of devices under radiation.	6 months
Implementation of digital logic appropriate to chosen rad hard process; implementation of refined analog circuits based on device characterization; production of nearly complete system (several channels per chip).	12 months
Measurements of first chip; radiation tests; characterization of performance degradation. Refinement of digital and analog designs; manufacture of refined circuit; possible implementation in a second rad hard process.	18 months
Measurement of second version of complete chip. Complete characterization as function of radiation. Inclusion of refinements in overall architecture. Production of "final" version for R&D purposes.	24 months

6. Silicon Strip Readout

Optimization of shaping time for minimum power, subject to 5 nsec time resolution, adequate S/N. Study of architecture for Level 1–Level 2 storage which provides minimum power.	6 months
Optimization of designs for rad hard process; Fabrication of preamplifier and Level 1 storage.	12 months
Evaluation of radiation resistance of prototype amplifier and analog storage. Detailed design and layout of Level 2 storage. Refinement of analog designs for improved radiation resistance. Fabrication of second chip.	18 months
Evaluation of 2nd chip for analog performance, radiation hardness; refinements to Level 2 storage, inclusion of digital logic for interaction with trigger system and readout.	24 months

7. Radiation Resistance Testing of Devices and Circuits
   In 2, 4, 5, 6 will be completed in 6 months after the electrical tests on prototypes have been done.

12.3 Budget

The table on the following pages summarizes the required resources for the program outlined.

Budget for Front End Subsystem - Per Year

	Manpower Eng	Tech	Stud/ Facul	Cost	Materials & Purchases Sub.	Proc. Suppl.	Equip	Travel	Instit.
1. Front End Electronics for Calorimetry									
1.1 JFET and preamplifier Development (sub-contracts with industry only)					75				BNL
1.2 Fast summing amplifiers and shapers	1			125		25			BNL
1.3 Calibration system and gain control	1			125		25			BNL
1.4 Development of Amplifiers for Readout Branch;	1			140					LBL
		0.25		25					LBL
Subcontract with Industry					50				
1.5 Development of 60 MHz, Large Dynamic Range, Analog Memory	1.5			210					LBL
		0.25		25					LBL
1.6 Alternative Preampl. Designs	0.5			60					Harvard
2. Interpolating Pad Chamber Readout	1			125		25			BNL
3. Drift Time Readout									
3.1 Rad Hard TVCAMU incl Level 2 & Readout	1			125		10			Penn
4. Silicon Strip Readout									
4.1 CMOS Analog Readout	1			100		10			Rutherfo
4.2 BiCMOS Analog Readout			1	40					Penn
5. Radiation Hard Evaluation, Testing, and Development									
5.1 Testing of Devices and Circuits in 1.1 & 2	1			125					BNL
5.2 Systematic Test of Devices for CMOS & Bipolar;	1			80					Penn
Subcircuits for TVC			1	40					Penn
5.3 Subcontract w Bipolarics for Dev. of Rad Hard Bipolar					50				
6.0 General Architectural	0.5			70					LBL

Budget for Front End Subsy

Studies

7. Equipment and Software

7.1 IC Design Workstation (LBL) (hardware and software)	0	LBL
7.2 IC Design Software (Penn)	0	Penn
7.4 Verilog Simulator for Front End Daq Simulation	7	Penn
7.3 Test Equipment (LBL)	0	LBL
7.4 Test Equipment (Penn)	0	Penn
7.5 Workstation: IC Design & Daq. Simulation (Penn)	5	Penn
7.6 Misc. Equip.(Harvard)	0	Harvard

8. Processing

8.1 Bipolar for calorimeter summing and shaping amps, Drift chamber preamps, etc.

8.2 Short channel, double poly, analog CMOS for calorimeter readout and other applications (non-rad hard)

8.3 Rad Hard CMOS for Wire chamber drift time readout, pad chamber readout, silicon strip readout

9. Travel

Penn	10	Penn
LBL	10	LBL
BNL	10	BNL
RAL/Oxford	5	RAL/Oxf
Harvard	5	Harvard

Subtotals	$1,415	$175	$3	$40
	Manpowe	Subcont	Proc	Trav.

Total Budget $2,367

Notes:

(1) The column labelled Fac/Student includes the graduate student stipend, tuition, and 0.5

month faculty salary for supervision.

(2) All amounts include overhead at the relevant institution except for the Subcontract, Processing, and Equipment charges which are assumed to be overhead free.

(3) The budget is per year for two years. Successful conclusion of some of the projects may require funding for a third year.