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STUDY OF ACQUISITION ELECTRONICS WITH A HIGH DYNAMIC RANGE FOR A BEAM LOSS MEASUREMENT SYSTEM

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To dad and mom, for their love and support throughout these years.

"Fundamentally, all writing is about the same thing; it's about dying, about the brief flicker of time we have here, and the frustration that it creates."
Mordecai Richler

"Try not to be so negative all the time. Why don't you offer a little... constructive criticism?"
the Blues Brothers, while racing in a parking lot chased by the cops.

Sommario

Le particelle accelerate nella catena di acceleratori al CERN raggiungono energie elevate, la più elevata, al momento di collisione nel LHC, è pari a 7 GeV.

Durante l'azionamento delle macchine, inevitabilmente un certo numero di particelle sono perse dal fascio, depositando energia nelle parti che compongono la macchina e generando una cascata di particelle secondarie nella collisione con la struttura.

Il processo di generazione della cascata, nell'interazione con la struttura dell'acceleratore, attiva il materiale, costituendo un fattore di rischio per i lavoratori nell'acceleratore.

A seconda dell'entità delle perdite è anche possibile che si determini un danneggiamento fisico dei componenti dell'acceleratore. Nel Large Hadron Collider, i magneti superconduttori che mantengono le particelle nell'orbita circolare e forniscono la necessaria messa a fuoco al fascio sono mantenuti ad una temperatura di funzionamento pari a 1.9 K attraverso un sistema criogenico facente uso di elio superliquido. Un innalzamento di temperatura potrebbe potenzialmente interrompere il fenomeno superconduttivo, provocando un innalzamento improvviso della resistivitá del materiale e la dissipazione immediata di tutta l'energia immagazzinata nel magnete, danneggiandolo irrevocabilmente. La perdita del fascio é potenzialmente distruttiva anche negli acceleratori minori, nel SPS é in grado di perforare la camera a vuoto che lo contiene.

Il sistema di monitoraggio delle perdite del fascio è stato sviluppato per proteggere affidabilmente le macchine che compongono la catena di acceleratori del CERN, minimizzare l'attivazione dei materiali e fornire informazioni sullo stato del fascio agli operatori del sincrotrone: il sistema fornisce misure riguardo a restrizioni dell'apertura focale, distorsione dell'orbita, oscillazione del fascio e diffusione delle particelle. Tali informazioni sono utilizzate per regolare i parametri della macchina e massimizzare l'efficienza di trasmissione delle particelle dalla sorgente al punto di interazione.

Per questo motivo, due tipi di rivelatori sono distribuiti lungo gli acceleratori, nelle posizioni in cui si attendono le perdite più significative: il tipo di sensore principale è la camera di ionizzazione, sebbene dove si attendano dosi estremamente elevate, tali da saturarne la risposta, vengono utilizzati monitor di emissione secondaria. Entrambi i rivelatori sono sensibili alle cascate di particelle secondarie dovute alle interazioni ad alta energia e sono caratterizzati da una eccellente linearità e accuratezza rispetto all'energia persa dalle particelle nell'attraversamento, una risposta rapida e una buona resistenza alle radiazioni ionizzanti.

Laddove è richiesta una protezione pronta della macchina, per ogni posizione dei rivelatori, la frazione della cascata di particelle che interagisce con il sensore è ricondotta all'energia deposta nel magnete attraverso simulazioni ed è definito un massimo valore permesso, tale da non causare danni.

Il segnale proveniente dal rivelatore è letto dall'elettronica di misura e, dove necessario, il valore acquisito è confrontato con la soglia associata alla posizione considerata lungo l'anello. A causa della varietà delle dimensioni degli acceleratori, il segnale può essere acquisito e convertito in digitale nel tunnel dell'acceleratore e inviato all'elettronica di superficie per essere processato – come avviene nell'LHC – o l'intera acquisizione e processamento può essere effettuata in superficie in una zona protetta ricavata ad hoc. Nel primo caso, è necessario che l'elettronica sia in grado di tollerare l'esposizione alle radiazioni.

Quando è rilevato che una soglia energetica è stata superata, l'abilitazione del fascio è interrotta e le particelle sono dirette verso una linea di dump. Nelle macchine che utilizzano magneti caldi – ad esempio PS Booster – quando si verificano delle perdite eccessive, i parametri della macchina sono regolati, migliorando così la qualità del fascio.

In questo lavoro, è stato realizzato il progetto di un convertitore digitale per il segnale di corrente proveniente da camere di ionizzazione, basato su un principio di conversione corrente-frequenza. Il progetto si rivolge agli acceleratori Proton Synchrotron, PS Booster e al futuro LINAC4, dove le perdite sono elevate rispetto ad altri casi simili, con un massimo pari a 100 mA. La minima corrente che si vuole rilevare vale 1 nA.

Il sistema permette l'acquisizione integrale di segnali di ambo le polarità senza richiedere alcuna configurazione e fornisce un numero digitale avente un LSB pari ad una carica elementare, corredato da un conteggio frazionario tramite un convertitore analogico digitale, per incrementare la risoluzione.

Dopo una introduzione sul CERN, la prima parte fornisce una descrizione del sistema di misura delle perdite del fascio e dei sensori utilizzati. La teoria alla base del loro funzionamento è rivista e corredata di misure sperimentali.

Successivamente, è effettuato un confronto tra le possibili scelte che possono essere fatte per realizzare il dispositivo.

Sono innazitutto considerate le tecniche presenti in letteratura che permettono l'acquisizione del segnale per accoppiamento in continua, con particolare attenzione a quelle che offrono un range dinamico elevato, tra cui i convertitori corrente-frequenza. Nel capitolo successivo, è rivista la teoria della misura di carica associata ad impulsi di corrente rapidi e ripetitivi, tali sono quelli generati dai singoli gruppi di particelle che riempiono gli acceleratori. Per ottenere un range dinamico elevato, è data particolare attenzione alla minimizzazione della carica di rumore equivalente (ENC), basata sulla teoria del filtraggio ottimo.

Tra le due categorie, è stata scelta la prima, per le seguenti ragioni: il segnale di uscita dalla camera di ionizzazione è una rapida sequenza di impulsi, spaziati di 500 ns caratterizzati da una lunga coda, dovuta alla lenta deriva degli ioni nel gas che riempie il rivelatore. La carica di questi impulsi vuole essere misurata integralmente ma la soppressione della coda viene ad essere necessaria per impedire la sovrapposizione dei segnali in ingresso al convertitore analogico digitale alla fine della catena di filtraggio. Inoltre, il sistema non si presta facilmente a misure di correnti di ambo le polarità, richieste nelle specifiche.

Diverse architetture circuitali sono considerate e modifiche sono proposte ove necessarie. Tra i circuiti analizzati sono presenti integratori a bilancio di carica, stadi a due integratori operanti in parallelo e integratori con condensatori commutabili, in versioni sincrone e asincrone.

È stato progettato un sistema, contenente un FPGA per il processamento dei dati e la loro trasmissione su bus VME64. È stato scritto il codice VHDL necessario al funzionamento, incluso il processamento dei dati acquisiti e la loro organizzazione in somme parziali su finestre temporali mobili, la loro trasmissione secondo il corretto protocollo sul bus e diverse funzionalità secondarie che forniscono informazioni sullo stato del sistema. Un primo prototipo è stato inviato per essere realizzato. A causa di alcuni ritardi nella realizzazione della scheda stampata, al momento della scrittura di questa tesi non sono ancora disponibili dati sperimentali.

Abstract

The particles accelerated in CERN accelerator chain reach high energies, topped by the particle energy at collision in the LHC, 7 GeV.

During the operation, an amount of particles is inevitably lost from the beam. Depending on the extent of the losses, physical damage to machine components may be caused and the shower of secondary emission particles deposits energy in the surrounding equipment constituting the accelerator. The hadronic cascade also activates their materials, representing a hazard to the workers at CERN.

In the LHC, the superconducting magnets that constitute the synchrotron lattice are kept at an operating temperature of 1.9 K through a cryogenic facility employing superliquid helium, the increase in their temperature potentially initiates a quench. In the SPS, the damage due to a lost beam is also visible.

The Beam Loss Monitoring (BLM) system has been developed to reliably protect the machines composing CERN's accelerator chain and additionally provide information about the beam status: the system provides observations about local aperture restrictions, orbit distortion, beam oscillations and particle diffusion, allowing the operators to tune the machines, measure and maximize the efficiency of the chain.

To achieve this, two types of particles detectors are distributed along the machines in the positions where the most intense losses are expected, typically where aperture limitations are present – for example where the collimators are located. The main type of detector in use is the ionization chamber, albeit where a very high dose rate is expected Secondary Emission Monitor (SEM) are employed instead. Both types of detectors are sensitive to the hardronic showers initiated by high energy particles and they are characterized by high linearity and accuracy with respect to the energy lost by the particles, a fast responses and good radiation tolerance.

Where timely machine protection is in place, for every detector location the fraction of particles from the hardronic showers has been linked to the energy distribution within the coil through simulation-based analysis and maximum allowable energy value has been established.

The signal from the detector is acquired by the front-end electronics and, where applicable, the measurement is compared with the threshold relevant for the considered ring location. As the dimensions of the accelerators varies greatly, the signal might be acquired, digitized in the accelerator tunnel and then sent to the surface electronics to be processed – as it happens in the LHC – or the complete processing may occur in a shielded facility closely located. In the former case, radiation tolerant electronics is required.

In the LHC, when a threshold is exceeded, the beam permit signal is revoked and the circulating particles are directed towards the dump line. In machines employing warm magnets – such as the PS Booster – the beam parameters are tuned before the next injection, to increase the quality of the beam.

A discrete components design of a current digitizer based on the current-to-frequency converter (CFC) principle has been studied in this work. The design targets at rather high input current compared to similar acquisition systems, with a maximum equal to 100 mA and a minimum of 1 nA, as required by the ionization chamber that will be employed in the Proton Synchrotron and Booster accelerators as well as in the LINAC 4. It allows the integral acquisition of currents of both polarities without requiring any configuration and provides a digital number having an LSB equal to a reference charge complemented with an additional fractional count through an ADC, to increase the resolution.

Several architectural choices we considered for the front-end circuit, including charge balance integrators, dual-integrator input stages, integrators with switchable-capacitor, in both synchronous and asynchronous versions.

The signal is processed by an FPGA and transmitted over a VME64x bus.

Acknowledgements

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Many thanks to Christos Zamantzas, for helping me out many times, sometimes they were small but important things and for sharing with me his insight in digital design. And for being a friend.

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Outside the time spent in the lab or in front of the PC, I was very luck to meet some good friends, Daniel, Ling and Lourdes. If this year has been so pleasant, they're surely responsible.

Abbreviations

ADC Analog Digital Converter

BLM Beam Loss Monitoring

BJT Bipolar Junction Transistor

CERN European Organisation for Nuclear Research

CFC Current-to-Frequency Converter

DAC Digital to Analog Converter

DPDT Double Pole Double Throw

DR Dynamic Range

ENC Equivalent Noise Charge

FCC Frequency-to-Current Converter

FF Flip-Flop register

FPGA Field Programmable Gate Array

GBW Gain Bandwidth Product

IC Integrated Circuit

LEIR Low Energy Ion Ring

LHC Large Hadron Collider

LINAC Linear Accelerator

LSB Least Significant Bit

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

OA Operational Amplifier

PS or CPS (CERN) Proton Synchrotron

SNR Signal to Noise Ratio

SPDT Single Pole Double Throw

SPS Super Proton Synchrotron (CERN)

SPST Single pole Single Throw

VFC Voltage-to-Frequency Converter

VHDL VHSIC Hardware Description Language

Contents

Introduction

This work was carried out at CERN during an one year internship in the BE-BI-BL section.

The main objectives of this work are summarized as follows:

- Evaluation of the different architectures available at the state of the art to measure the current signal
- Design, review and simulation, where applicable, of selected circuits conforming to the specifications.
- Design of the digital electronics required for processing and data transmission.
- Realization of a prototype printed circuit board (PCB).
- Review of the results and future developments.

The first chapter introduces CERN, its accelerator complex and the Beam Loss Monitoring system.

The second chapter is dedicated to the Beam Loss Monitoring (BLM) system, in particular to the particle detectors, their outcoming signal and the electrical circuit.

Chapter 3 reviews the possible state-of-the-art design choiches for the measurement of currents extending to DC over a wide dynamic range.

In Chapter 4, the techniques for fast measurement of the charge of the single pulses due to each bunch are described, with focus on minimizing the noise of the measurement, thereby increasing the dynamic range.

The first part of Chapter 5 describes the selected circuits, deals with the modifications to their architectures introduced in this work, describes the expected results front-end analog part of the acquisition board. The second part of the chapter is dedicated to the digital circuits: the section covers the signal acquisition and its processing, the choice of the FPGA and the VHDL code written.

Possibilities for further developments are part of the topic of the Conclusions.

Chapter 1

CERN - European Organization for Nuclear Research

CERN, the European Organization for Nuclear Research, is the world's largest particle physics laboratory. The acronym originates from the initial French name "Conseil Européen pour la Recherche Nucléaire", or European Council for Nuclear Research, a provisional body founded in 1952 with the mandate of establishing a world-class fundamental physics research organization in Europe.

When the laboratory officially was founded in 1954, the organization was given the name European Organization for Nuclear Research, although the name CERN was retained. CERN was one of Europe's first joint ventures and it includes presently 20 member states.

The research center is located across the Franco-Swiss border near Geneva, besides the Jura mountains.

CERN's main function is to provide to scientists the particle accelerators, detectors and other infrastructure needed for high-energy physics research. Even advancements in other fields are due to the work of the scientists working at the laboratory, the most popular being the World Wide Web. Numerous experiments focused on different aspects have been constructed at CERN and the access is provided to universities and research group spread around the world. A large computer center provides the powerful data processing facilities for experimental data analysis, the data storage and a wide area networking hub allows the access.

The key events of the history of CERN from its first conception in 1954, to the first beam in the LHC in 2008 can be found in appendix A.

1.1 CERN experiments

The bleeding edge research is currently carried out in the Large Hadron Collider, whose operation is scheduled to restart in October 2009. The LHC has four main experiments, each is constituted by an assembly of detectors centered around a collision point, tracking the trajectories and measuring the energies of the generated particles at the four beam crossings in the machine. These detectors are specifically targeted at searching for the Higgs boson and evidence of supersymmetry.

The experiments are ATLAS, A Toroidal LHC ApparatuS, CMS, the Compact Muon Solenoid, ALICE, A Large Ion Collider Experiment and LHCb, which stands for LHC beauty.

The ATLAS detector is 44 meters long and 25 meters in diameter, weighing about 7 thousand tonnes. It employs silicon pixels and strips, and a straw-tube based transition radiation detector inside a superconducting solenoid with a SI2T magnetic field. The region surrounding the inner core, closest to the interaction point, is constituted by a electromagnetic calorimeter enclosed by ironscintillator and Cu/W-LAr hadronic calorimeters. The outer shell is the ATLAS muon system, composed of muon drift tubes, thin gap chambers and resistive plate chambers embedded in a large array of 8 air-core toroid magnets.

CMS is a general-purpose detector, capable of studying many aspects of proton collisions. It contains subsystems which are designed to measure the energy and momentum of photons, electrons, muons, and other particles produced in collision. It is formed by five layers, the innermost being a silicon-based tracker, itself composed by silicon pixels and microstrips. Surrounding it is a scintillating crystal electromagnetic calorimeter, followed by a sampling calorimeter for hadrons. The tracker and the calorimetry are fitted inside a superconducting solenoid which generates a magnetic field of 4 T. Outside the magnet is the muon system, which is composed of drift tubes, cathode strip chambers and resistive plate chambers inserted between iron layers of the flux return. [43]

1.2 The CERN Accelerator Complex

The protons collided in the experiments described are accelerated through a chain of five accelerators:

LINAC2 → Booster → PS → SPS → LHC

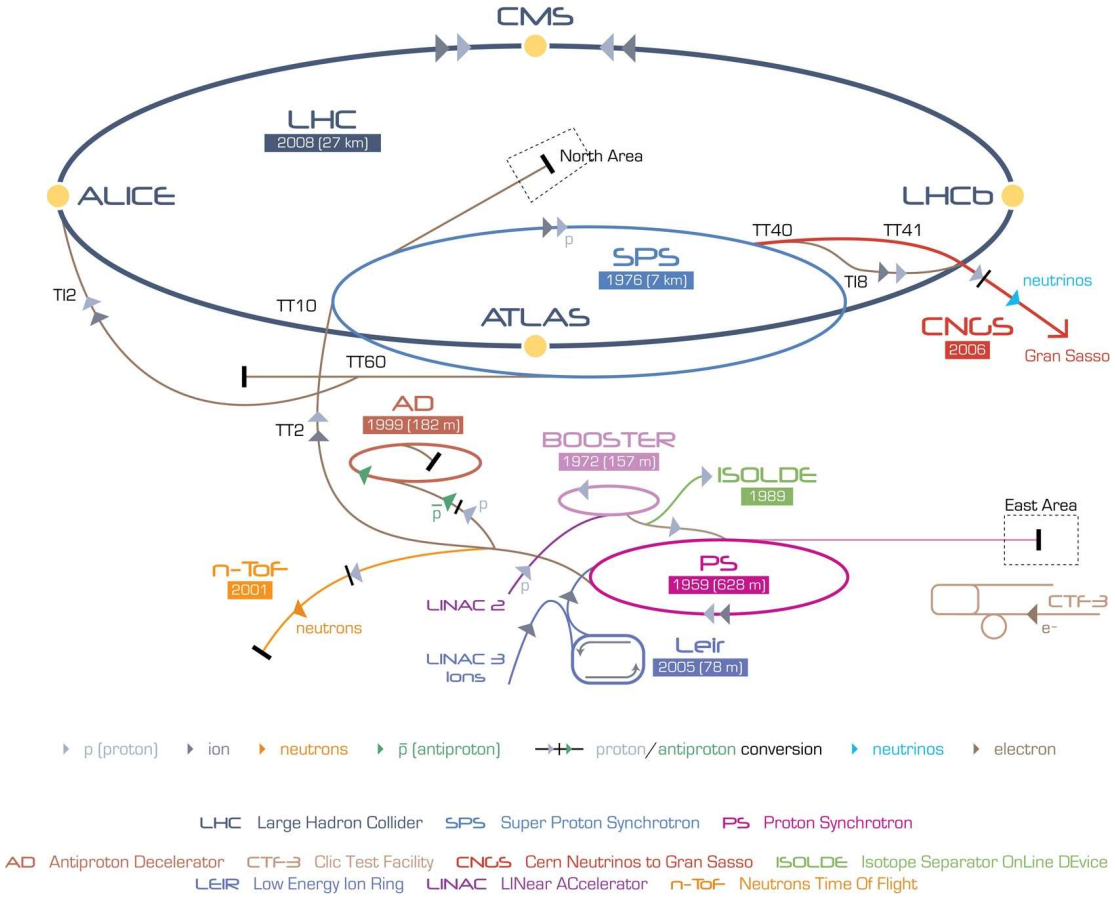


Figure 1.1: CERN accelerator complex

On the other hand, the path for ions is,

LINAC3 → LEIR → PS → SPS → LHC

This complex has been enhanced and upgraded over many years, the Proton Synchrotron (PS) was one of the first accelerators commissioned at CERN, and almost fifty years later is still working with very high efficiency. In PS, the protons are accelerated an energy equal to 28 GeV, from here they are passed to the SPS where they are accelerated to 450 GeV, finally they are transferred to LHC, where acceleration will bring protons to an energy of 7 TeV, determining a collision energy of 14 TeV.

CERN accelerator complex is shown in fig. 1.1, where other experiments are also visible. One of the most notable is the CERN Neutrinos to Gran Sasso (CNGS), where a beam consisting of only muon-type neutrinos from the SPS accelerator is sent to the Gran Sasso National Laboratory (LNGS) of the INFN in Italy. Since neutrinos interact very rarely with matter, the beam is received at a distance of 730 km. Other experiments are the neutron time-of-flight facility (n_TOF), a pulsed neutron source operative since 2001, ISOLDE, a line dedicated to the production of several different radioactive ion beams, the CLIC Test Facility (CTF3) a linear electron-positron accelerator aimed at demonstrating the feasibility of the proposed Compact Linear Collider (CLIC) study and the CERN Antiproton Decelerator (AD).

1.2.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is the latest accelerator built at CERN, first operational in September, 2008 and scheduled for restart in October, 2009. [21]

Characterized by a circumference length of 27 km, it is divided in eight sectors, or octant, each 3.3 km in length. The particles in the machine are concentrated into bunches, spaced by 25 ns and 1.12 ns long. Each ring hosts an effective number of 2808 bunches with an intensity of 1.1×10^{11} per bunch of protons. The revolution time is 88.9 μs corresponding to a frequency of 11.246 kHz.

The particles are kept in a circular orbit by cooled magnets, providing a magnetic field of 8.3 T. The magnets are made from superconducting NbTi, supporting a current of about 12 kA and storing, during the operation, a total amount of energy of about 10 GJ. Each sector is served by a cryoplant, in which is housed a helium refrigerator, providing superfluid helium at 4.5 K or 1.9 K.

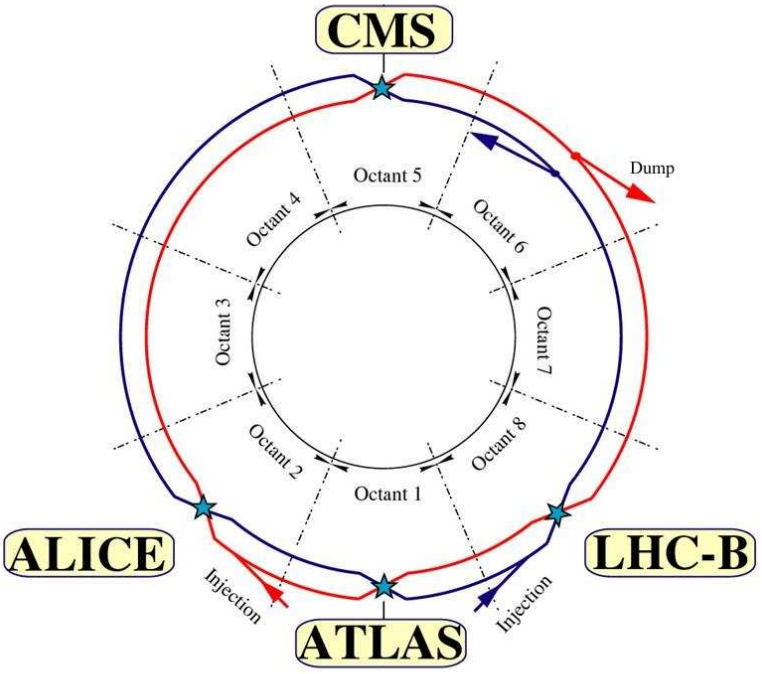


Figure 1.2: Structure of the LHC, with experiment locations in evidence

Beam Parameter	Value
Proton Energy at Injection	450 GeV
Proton Energy at Collision	7 TeV
Protons per Bunch	1.15×10^{11}
Number of Bunches in LHC	2808
Protons in LHC	3.23×10^{14}
Number of Bunches in SPS extraction	216 or 288
Protons at SPS extraction	2.48×10^{13} or 3.31×10^{13}
Number of Bunches at PS extraction	72
Protons at PS extraction	8.27 1012

Table 1.1: Beam Parameters of the LHC. [21]

The luminosity $\mathcal{L}$ of a storage ring determines the secondary particle rate and therefore the discovery potential. It is a measurement of the number of collisions that can be produced in a detector per cm^2 and per second and it is a parameter optimized in the design of a storage ring.

$$\mathcal{L} \approx \frac{N^2 f}{4\pi\sigma_x\sigma_y} \tag{1.1}$$

N are the number of particles per bunch of beam, supposed to be equal for both beams

f is the rate of bunches with protons [Hz]

σ_x and σ_y are the standard deviations that characterize the Gaussian transverse beam profile [cm]

The luminosity of the LHC will be approximatively $1 \times 10^{34}\ /cm^2/s$, which multiplied by the interaction cross section determines the average rate of collisions per seconds.

The other main parameters of the machine are listed in tab. 1.1. Its performances will surpass comparable machines in energy by a factor 7, in luminosity by a factor of 100 and in beam intensity by a factor of 23.

1.2.2 The Super Proton Synchrotron

The SPS is a circular proton accelerator operational since 1976, with a circumference of 7 km. At the end of the 70's, it was used also as a proton - antiproton collider, revealing the W and

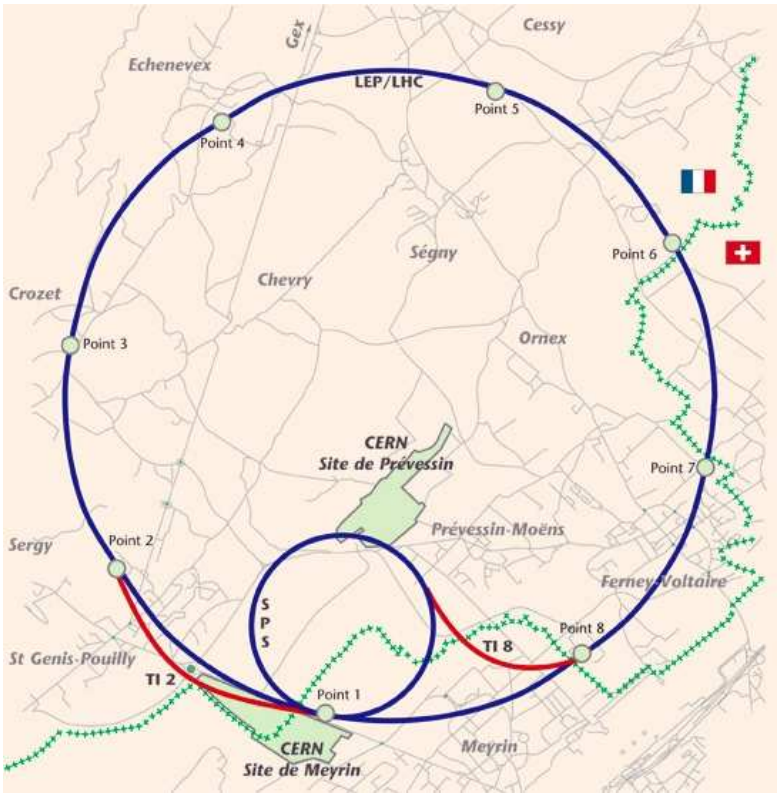


Figure 1.3: The SPS and the extraction lines to the LHC

Z bosons, for whose discovery the Nobel Prize was awarded to Simon van der Meer and Carlo Rubbia. SPS is currently in use as a proton or heavy ion accelerator, with a maximum energy of 450 GeV. Two transfer lines, TI2 and TI8, have been added to the machine, permit the injection of the beam in the LHC. The SPS, the transfer lines and their connection to the LHC are shown in fig. 1.3.

1.2.3 The Proton Synchrotron and the Proton Synchrotron Booster

Figure 1.4: A picture of the PSB tunnel, showing the four ring circular accelerator.

The CERN Proton Synchrotron (PS or CPS) is a circular accelerator with a circumference of 628.3 m. It is currently the oldest machine in operation at CERN (built in 1950), due to its extreme versatility: it is capable of accelerating protons, antiprotons, electrons, positrons and various species of ions. Over the years, major upgrades have improved its performances by more than a factor of 1000 since its initial operation in 1959.

The protons are injected in PS from the Proton Synchrotron Booster (PSB), the smallest circular proton accelerator in the CERN accelerator complex, built in 1972 and measuring 160 meters. It receives protons at an energy of 50 MeV from the linear accelerator Linac2 and accelerates them up to 1.38 GeV, when they are injected into the Proton Synchrotron.

Chapter 2

The Beam Loss Monitoring System

2.1 The Beam Loss Monitors

The ionization chamber is the main Beam Loss Monitor (BLM) currently in use in CERN accelerator complex. As it will be explained more in detail in the next sections, the ionization chamber provide a charge on the electrodes proportional to the amount of particles that traversed the active volume. The incoming particles ionize the nitrogen gas within the chamber, freeing electrons from the gas molecules. The positively charged ions and electrons are separated through an applied electric field and collected at the electrodes.

This chapter introduces the principles of the operation of ionization chambers and gives a basic introduction to energy loss of charged particles in matter [19, 45].

2.2 Principles of operation of ionization chambers

When energetic particles pass through matter a certain amount of their energy is lost in the interaction. The amount of lost energy and the different processes responsible for its transfer depend on the characteristics of the particle, such as charge and mass, energy and the material.

Several types of interaction that may occur, here the principal ones are summarized by particle type. [45]

Electrons lose energy mainly by ionization at low energies and by bremsstrahlung at high energies. Particles without charge as photons and neutrons do not directly ionize the gas, but generate secondary charges by a combination of other processes. Photons may lose their energy in the interaction with an atom and liberate an electron through the photoelectric effect. Other phenomena in which photons are of primary importance are Compton scattering and the pair creation process. If we consider neutrons, different interactions as elastic or inelastic nuclear collisions become important, depending on the energy of the particle.

2.2.1 Energy loss by heavy charged particles

Particles with a mass greater than the mass of the electrons are briefly considered in this section.

Several different interactions are responsible for the transfer of energy form the heavy particle to the molecule. The ionization event is possible if the transferred energy is greater than the binding energy of an electron in the outer shell of the atom. If this condition is not verified, the effect is an increased temperature of the gas, until the energy is transferred elsewhere and the gas returns at rest.

For particles of energies of the order of 0.1 to 100 GeV, the Bethe-Bloch equation (eq. 2.1) gives the average energy lost by a charged particle (dE) as it travels a length equal to dx [16]. The quantity dE/dx is also referred to as stopping power of the material.

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln(\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2}) - \beta^2 - \frac{\delta}{2}\right] \tag{2.1}$$

$\gamma = (1-\beta^2)^{-1/2}$

Z is the atomic number of the gas

A is the atomic mass of the medium

z is the charge of the heavy charged particle

β is the velocity of the particle normalized to the speed of light c

δ is a density effect correction

K is defined as $4\pi N_A r_e^2 m_e c^2$

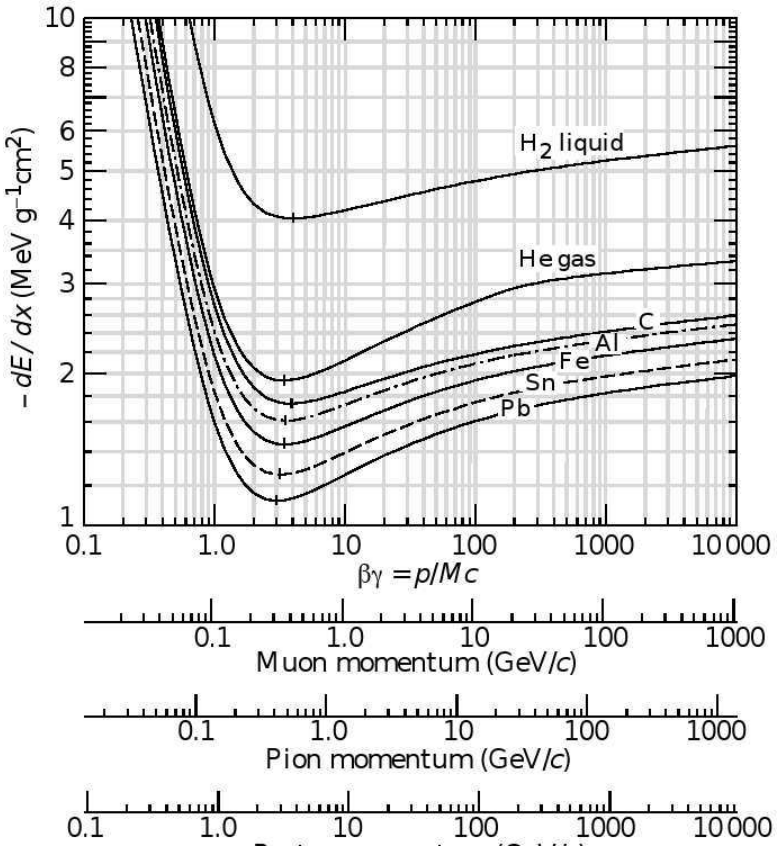


Figure 2.1: Stopping power of different materials, from [57, 45]

N_A is Avogadro's number

r_e is the classical electron radius

$T_{max} = 2m_e c^2 \beta^2 \gamma^2$ is the maximum transferable energy in a single collision of an electron

The mean energy loss rate in different materials for muons, pions and protons depending on their kinetic energy is shown in fig. 2.1.

2.2.2 Energy per ionization event, mobility of the charge carriers and region of operation of the detector

Nitrogen gas (N_2) was chosen for the BLM monitors. The first ionization potential of the electron is at about 15.5 eV, this corresponds to the minimum energy that a charged particle or a photon must have in order ot be detected, for lower energies, a single particle interaction can't free an electron.

Since other processes, in addition to ionization events, contribute to the energy loss of the particle, the average energy required per creation of ion-electron pair is greater than the ionization energy. Its value is called the W-factor and it is in the range 25 eV-35 eV depending on the type of the incoming particle and gas. The average number of elctron-ion pairs created is propotional to the energy lost by the particle and inversely proportional to the W-factor. [45]

The simulated LHC BLM detector response function for different particle types is shown in fig. 2.2. The impact angle of the particles relative to the detector axis is 60°, the detector structure is described in sect. 2.3.

The drift velocity of a charged particle in the pressurized gas where a uniform electric field E is present can be described by the law:

$$v = \mu \frac{E}{P} \tag{2.2}$$

μ is a constant called mobility, associated with the considered carrier [$\mathrm{m\,Pa^{-1}\,V^{-1}}$]

E is the electric field [$\mathrm{V\,m^{-1}}$]

P is the pressure of the gas [Pa]

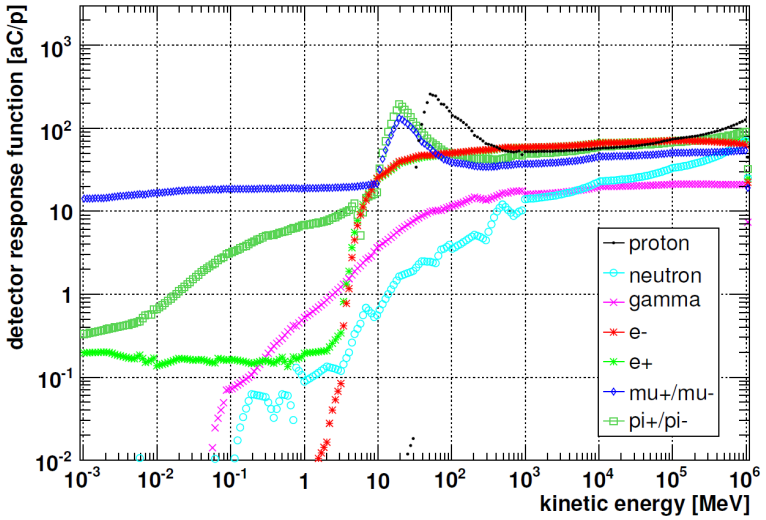


Figure 2.2: Collected charge for different particles at different energies. From [45].

Ions have much lower mobility – a factor 1×10^3 or more – than electrons and therefore drift at a lower velocity and are collected at the electrodes after a longer time.

Two main observations led to the choice of N_2 as filling gas for the ionization chamber: it is, between the possible choices, the gas with the highest ion mobility and it is a gas common in the air, therefore a ionization chamber with leakage would still provide an output signal. [45]

Another important observation concerns the operating mode of the ionization chamber as the applied voltage is varied. The gain of the ionization chamber is defined as the proportionality factor between the initially ionized charge and the charge overall collected.

A plot of the gain is shown in fig. 2.3, it is possible to distinguish several operating conditions, the three most important will be mentioned here.

At low voltages, the induced field in the ionization chamber is low, producing a slow drift of the carriers which will have greater chances of recombining before reaching the electrodes. The zone labeled “ionization chamber” is the region of standard operation, here the gain is constant and approximatively equal to one. In this region, a fixed ratio of the ionized charge is collected, independently of the applied field and therefore the gain has a very low dependence on the fluctuations of the supply. Increasing further the applied potential, multiplication effects begin to appear. The carriers can gain enough energy to collide and ionize other molecules. The collected charge will again be proportional to the initial ionized charge, but through a multiplication factor, greater than one, that depends on the applied voltage. In fig. 2.3, this

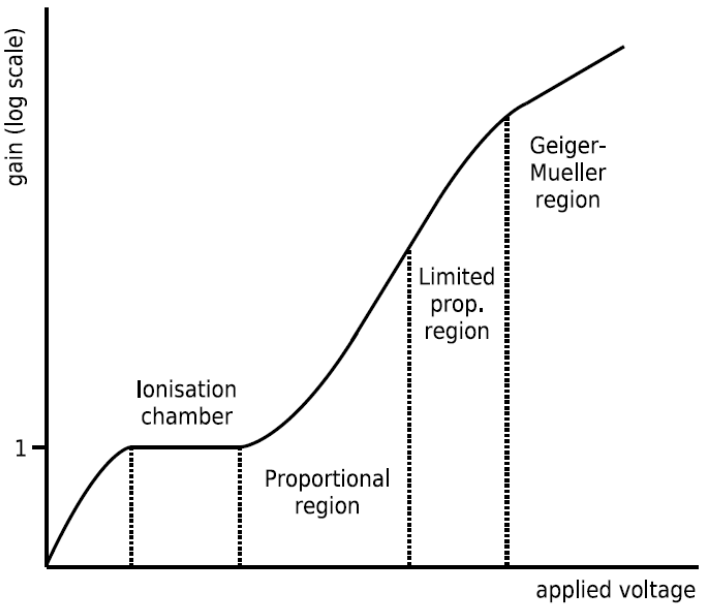


Figure 2.3: Gain of a ionization chamber with applied voltage, from [45].

region is labeled “proportional region"". In the next zones, other non-linear effects will modify the gain. To preserve the linearity of the detector, the operating point of the ionization chamber is kept out of these regions.

2.2.3 Ramo’s theorem

The current induced on the electrodes by a charge generated in the medium can be derived with the Ramo-Shockley theorem.[37, 41, 44]

Consider a structure delimited by an arbitrary number of electrodes and assume that all the conductors are at ground potential. A charge q is situated in the region. If the potential of the electrostatic field between the conductors is V, then we can write

$$\nabla^2 V = 0 \tag{2.3}$$

A small equipotential sphere can be chosen to surround the charge q. Let V_q be the potential on its surface S_s. Applying Gauss’ Law,

$$\int_{S_s} \frac{\partial V}{\partial n} ds = 4\pi q \tag{2.4}$$

If the charge is removed and a conductor is biased at 1 V, calling the potential in this situation V_1, it is still true that $\nabla^2 V_1 = 0$, again in the region between the electrodes.

From Green's theorem,

$$\int_{Volume} (V_1 \nabla^2 V - V \nabla^2 V_1) dv = - \int_{S_{boundary}} \left[V_1 \frac{\partial V}{\partial n} - V_1 \frac{\partial V}{\partial n} \right] dS \tag{2.5}$$

If the volume in eq. 2.5 is chosen to be delimited by the surfaces of the electrodes (the surface of the biased electrode is called S_1 in the following) and the surface of the sphere (S_s), the left-hand side integral is null and the right hand integral can be split in three components:

- The integral over the grounded conductors, which is null, since V and V_1 are both zero.
- The integral over the surface of the biased electrode. Here $V = 0$ V and $V_1 = 1$ V and the integral reduces to $- \int_{S_1} \frac{\partial V}{\partial n} ds$.
- The integral over the surface of the sphere, which can be written as the sum $-V_{q1} \int_{S_s} \frac{\partial V}{\partial n} dS$ and $V_q \int_{S_s} \frac{\partial V_1}{\partial n} dS$, the latter integral corresponds to Gauss' Law in the second situation, when there is no charge between the conductors and it is therefore null.

Eq. 2.5 can be rewritten as:

$$0 = - \int_{S_1} \frac{\partial V}{\partial n} ds - V_{q1} \int_{S_s} \frac{\partial V}{\partial n} ds = 4\pi Q_i - 4\pi q V_{q1} \tag{2.6}$$

Where Q_i is the charge induced on the biased electrode.

$$Q_i = q V_{q1} \tag{2.7}$$

Differentiating Q_i with respect to time, if the charge is moving in a direction x, we get the induced current:

$$i_i = \frac{dQ_i}{dt} = q \frac{dV_{q1}}{dt} = q \frac{\partial V_{q1}}{\partial x} \frac{\partial x}{\partial t} = q \frac{\partial \Phi}{\partial x} v_x \tag{2.8}$$

Where Φ is a weighting potential associated with the considered electrode that describes the coupling of the potential to the considered conductor. It is calculated biasing the electrode under study to 1 V while all the others are connected to ground. The electric field in a given

geometry determines the trajectory of the particles and it coincides with the weighting field, obtained from the weighting potential, only in presence of two electrodes.

From the Ramo-Shockley Theorem, the following conclusions can be drawn:

- A charge q moving from position p_1 to position p_2 along any path induces a net charge on the electrode n given by:

$$Q_n = q\left(\Phi_n(p_2) - \Phi_n(p_1)\right) \tag{2.9}$$

- The instantaneous current can be written in terms of weighting field as $i_i = -q\vec{v} \cdot \nabla\Phi_n$. The electric field s responsible of the trajectory of the particle, while the weighting field is responsible of the induced current.

2.2.4 Parallel plate capacitor

A plane capacitor with gas insulator is a basic structure for a ionization chamber. In this section, the signal induced on the electrodes by a plane layer of charge Q emitted from the anode and moving towards the cathode is derived, with and without Ramo's theorem and the results are compared. If, at a time $\bar{t}$, the layer of charge is located at the coordinate $\bar{x}$, the electric field in the device is as shown in fig. 2.4.

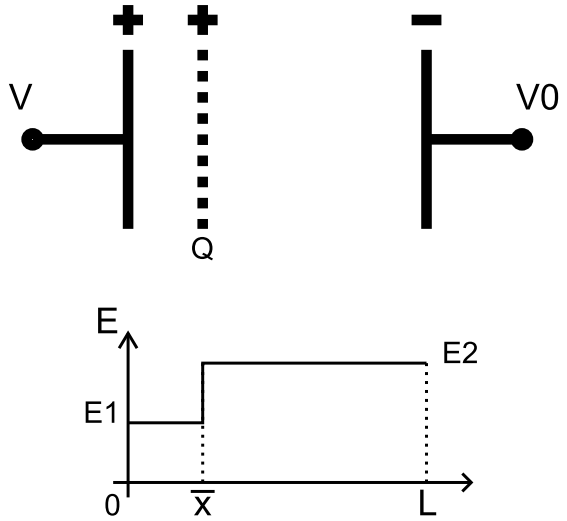


Figure 2.4: Electric field in a plane capacitor

The difference $E_2 - E_1$ can be evaluated applying Gauss' Law:

$$\epsilon(E_2 - E_1) = Q/A \tag{2.10}$$

Where A is the area of the plates of the capacitor.

The anode voltage is given by,

$$V = \int_0^L E(x)dx + V_0 = E_1\bar{x} + E_2(L - \bar{x}) + V_0 \tag{2.11}$$

Where L is the distance between the parallel plates and V_0 is the cathode voltage.

Substituting 2.10 in 2.11, we get:

$$V = E_2 L - \frac{Q\bar{x}}{\epsilon A} + V_0 \tag{2.12}$$

The charge on the anode is equal to:

$$Q_a = -\epsilon A E_2 = -\frac{\epsilon A}{L}\left(V - V_0 + \frac{Q\bar{x}}{\epsilon A}\right) \tag{2.13}$$

The current flowing in the capacitor is the derivative in time of the charge on the anode, Q_a.

$$I = -\frac{dQ_a}{dt} = \frac{\epsilon A}{L}\left(\frac{dV}{dt} + \frac{Q}{\epsilon A}\frac{d\bar{x}}{dt}\right) = C\frac{dV}{dt} + \frac{Qv}{L} \tag{2.14}$$

The two components are the current due to the capacitive coupling of the voltage applied on one electrode to the other and the current induced by the moving charges. Setting $dV/dt = 0$, integrating at both sides eq. 2.14, we get:

$$\int_0^T Idt = \int_0^L \frac{Q}{L}dx = Q \tag{2.15}$$

The integral of the induced current is equal to Q. It can be shown that if two layers of charge of the same absolute value Q and opposite sign are generated in an arbitrary position within the chamber, each of them will induce a current signal and the integral of their sum will again evaluate to Q.

The result in eq. 2.14 can be confronted with the one provided by Ramo's Theorem.

The weighting field is found setting the anode voltage to 1 V,

$$\Phi = \frac{1\,\mathrm{V}}{L} \tag{2.16}$$

And therefore, from eq. 2.8, the current is $I = Qv/L$. If the voltage applied to the anode is constant, eq. 2.14 gives the same result.

2.3 BLM ionization chambers

The ionization chamber in use in the BLM system are parallel plate chambers, more complex than the simple parallel plates capacitor considered previously.

The main parameters that affect the operation of this type detectors are the the choice of the gas that fills it, its pressure, as the determine the sensitivity and mobility of the carriers, and the bias voltage, which determines the operating region. The BLM ionization chambers are filled with nitrogen at a pressure of 100mbar and the bias voltage applied to the detector 1.5 kV is applied to the electrodes.

Two sensors having a very similar structure are in use: both of them have a circular section, electrodes of the same shape, orthogonal to the main axis of the chamber, with a thickness of 0.5 mm, equally spaced by 5.75 mm. Alternatively, one plate is connected to the output connector and the next to the high voltage input. The smaller ionization chamber, in use mainly in the SPS contains a total of 31 electrodes, while the bigger ionization chamber, in use mainly in the LHC but planned to be used in other accelerators as well, has a total of 61. They are hold in place by six stainless steel rods traversing longitudinally the whole structure and secured to the top and bottom plates by insulating ceramic bindings. [17, 45]

The two ionization detectors are enclosed in a stainless steel tube, with a wall thickness of 2 mm, and of a diameter equal to 75 mm, in the case of the LHC BLM (fig. 2.5), while the other (fig. 2.6) is wider and has a diameter of 93 mm.

Two cover plates are present: the bottom one, made of stainless steel as well and 4 mm (SPS BLM) or 5 mm thick; the top cover holds the connectors for the high voltage supply and the

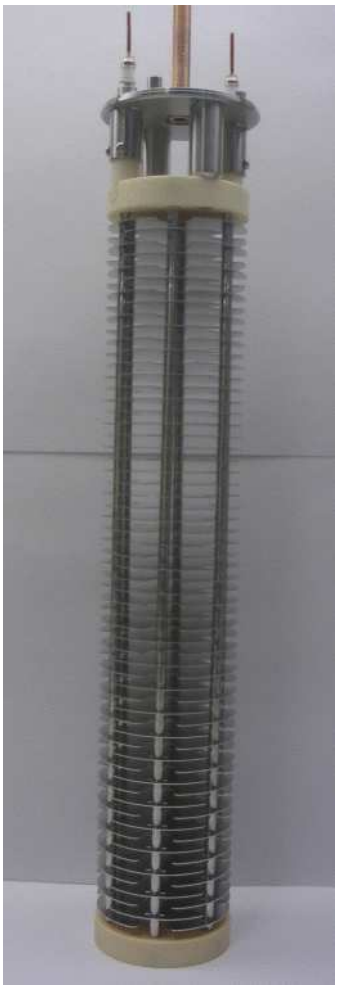


Figure 2.5: BLM ionization chamber introduced for the LHC. Metallic enclosure removed.

Figure 2.6: BLM ionization chamber developed for SPS. Metallic enclosure removed.

output signal. Under it, a RC filter is located. The purpose of the low pass filter is to reject any picked up interference or residual ripple on the high voltage, to avoid an unintended modulation of the gain of the detector. The values of the componets are $R = 1\,\mathrm{M\Omega}$, $C = 0.5\,\mu\mathrm{F}$, threfore the time constant of the filter is $\tau = 0.5\,\mathrm{s}$.

The mechanical drawing of the LHC and SPS ionization chambers can be found in the appendix C and D.

The capacitance of the LHC monitor has been measured and is equal to 350 pF.

Another type of detector that has a limited use as a beam loss detector is the Secondary Emission Monitors (SEM), employed in the locations where an higher intensity of particle flux is expected and shown in fig. 2.7. Its design is similar to the ionization chambers, but the principle of operation is different. Three titanium electrodes are enclosed in a stainless steel tube kept under vacuum. The incident particles free electrons colliding with the electrodes, through a physical process known as secondary emission those particles are accelerated and collected on the electrode of the opposite polarity and as in the previous case, the induced signal is measured.

Figure 2.7: Secondary emission monitor. Metallic enclosure removed.

2.4 Specifications

The electronics studied in this will replace the existing electronics in two accelerators, the PS and the PSB. Additionally, it will be employed in the replacement of LINAC 2, the LINAC 4, as soon as its construction is completed, expected in 2011. [35]

The specifications for the design are reported in tab. 2.1. From them, the specifications for the front-end listed in tab. 2.2 were derived.

From the reported specifications, the following observations can be made: the number of lost particles from the beam has to be measured on different fixed windows. Those values, stored in a local memory over several windows, constitute the post mortem buffer and should be supplied when requested. The post mortem buffer is useful in case the machine cannot be operated because as soon as it is started one or more of the maximum particle loss thresholds are exceeded. In this situation, the buffer provides detailed information about the last seconds of operation of the machine, allowing the debugging of its settings.

Moreover, the highest instantaneous loss corresponds to 100 mA and the front-end electronics should be able to acquire this current without saturating.

A last observation regards the synchronization: the beginning of the measurement has to be synchronized with the beginning of the cycle or pulse, if the accelerator is linear.

	PS	PSB	LINAC 4
Time resolution	2 µs	500 ns	2 µs
Largest loss	Loss of 4×10^{13} protons at 26 GeV	Loss of 4×10^{13} protons at 26 GeV	1.4×10^{9} H^- ions
Integration windows	1 ms and 1.2 s	1 ms and 1.2 s	2 µs and 400 µs
Max window	5 basic periods, or 6 s	1 basic period, or 1.2 s	400 µs
Post mortem	Not strictly necessary	Not strictly necessary	Yes
Post mortem buffer length	6000, maximum and minimum windows	1200, maximum and minimum windows	42000
Logging frequency	Once per cycle	Once per cycle	2 Hz
Synchronization	Start of cycle and revolution frequency	Start of cycle and revolution frequency	Start of pulse

Table 2.1: Specifications for the electronics

Parameter	Value
Maximum input current	100 mA
Minimum detected input current	1 nA
Signal to noise ratio	1×10^3 or greater
Maximum linearity error	20

Table 2.2: Specifications for the electronics

Chapter 3

Circuit architectures for DC current measurements

3.1 High dynamic range and bandwidth

There are several possible circuit architectures regarding the measurement of a current. The most immediate method to implement a current-to-voltage converter is through a transimpedance amplifier with resistive feedback, as shown in fig. 3.1. The input current I_{in} is supposed to be of a single polarity, ie positive.

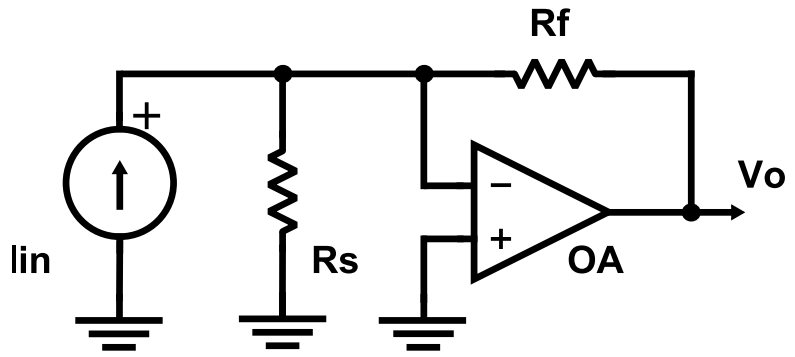


Figure 3.1: Transimpedance amplifier.

If we consider all components as ideal, in particular if we assume that the current source has no output capacitance, that the amplifier has a transfer function $A(s)$ and that the input and output

resistance of the amplifier are, respectively, infinite and null, then the circuit may be studied with the linear network theory, as follows.

Under the stated hypothesis, the circuit has a shunt-shunt feedback. The forward gain is $A_f(s) = -(R_s \mathbin{/\!/} R_f)A(s)$[1] and the feedback transfer function is $\beta(s) = -R_s/(R_f + R_s)$. The loop gain is hence:

$$G_{loop}(s) = A(s)\beta(s) = -A(s)R_s/(R_f + R_s) \tag{3.1}$$

The corresponding linear input-output characteristic is,[2]

$$\frac{V_o(s)}{I_{in}(s)} = \frac{A_f(s)}{1 - G_{loop}(s)} = -\frac{R_s R_f A(s)}{(1 + A(s))R_s + R_f} \tag{3.3}$$

In the following text, the closed-loop transfer function will be referred to as $G(s)$.

From eq. 3.3, it is easily shown that for all angular frequencies for which $|A(s)|_{s=j\omega} \gg -1/\beta$, the input-output characteristic reduces to $V_o = -R_f I_{in}$.

The approximation is reasonable until a decade before the loop gain angular frequency, which is defined as the angular frequency ω_p where:

$$|G_{loop}(s)|_{s=j\omega_p} = 1 \tag{3.4}$$

Or, equivalently:

$$|A(s)|_{s=j\omega_p} = -1/\beta \tag{3.5}$$

[1]The operator $\mathbin{/\!/}$ is here defined as: $a \mathbin{/\!/} b = ab/(a + b)$.

[2]The output resistance of a current source may be of the same order of magnitude of resistance R_d at input of the operational amplifier. In this case, the approximation $R_d \approx +\infty$ no longer holds. To take it in account, it is possible to substitute $R_s \mathbin{/\!/} R_d$ to R_s in eq. 3.3. A more general equation that considers both the finite input resistance and the reactive part of the elements composing the circuit is the following, written in the standard form:

$$\frac{V_o(s)}{I_{in}(s)} = -\frac{Z_f(s)}{1 + \frac{Z_s(s) \mathbin{/\!/} Z_d(s) + Z_f(s)}{A(s)(Z_s(s) \mathbin{/\!/} Z_d(s))}} \tag{3.2}$$

If the operational amplifier is internally compensated and its gain bandwidth product (GBW) is known, neglecting the effect of the other singularities, the loop gain angular frequency is equal to:

$$\omega_p = GBW \frac{R_s}{R_s + R_f} \approx GBW \tag{3.6}$$

if the value of the output resistance of the current source is much greater than the value of the feedback resistance, R_f.

Therefore, under the stated hypothesis, the circuit bandwidth doesn't depend on the gain. Furthermore, in the present discussion, we will assume that the bandwidth of the circuit may be selected independently from the gain of the amplifier.

The circuit is redrawn in fig. 3.2 along with its noise sources: the Johnson-Nyquist noise of R_f, i_{n,R_f}, the equivalent inverting current noise and voltage noise of the operational amplifier, $v_{n,OA}$ and $i_{n,OA}$ respectively and the input signal noise $i_{n,in}$. R_s is the equivalent output resistance of the source and may be dynamic. If this is the case, it doesn't have a thermal noise associated to it. In the present discussion, its noise is included in $i_{n,in}$. Other types of noises, such as flicker or burst noise, are not considered here.

The output noise is given by:

$$V_{o,n}(s) = -\frac{A(s)}{(1 + A(s))R_s + R_f} \left[R_s R_f \left(i_{n,in} + i_{n,OA} + i_{n,R_f} \right) + \left(R_s + R_f \right) v_{n,OA} \right] \tag{3.7}$$

Within the circuit bandwidth, where $|G_{loop}(s)|_{s=j\omega} \gg 1$, the previous expression reduces to:

$$V_{o,n}(s) = -R_f \left(i_{n,in} + i_{n,OA} + i_{n,R_f} \right) + \left(1 + \frac{R_f}{R_s} \right) v_{n,OA} \tag{3.8}$$

The amplifier shall be chosen so that it doesn't increase the magnitude of the overall output noise. For low minimum current applications, the op-amp must have low noise characteristics.

The maximum input current is determined by the amplifier saturation voltage, which are here supposed to be symmetric (ie $V_{o,MAX} = -V_{o,MIN}$).

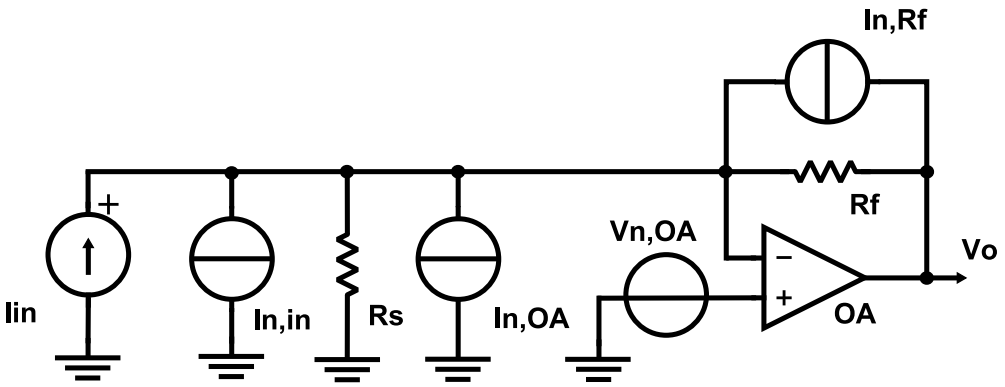


Figure 3.2: Transimpedance amplifier: noise sources.

Then:

$$I_{in,MAX} = \frac{V_{o,MAX}}{R_f} \tag{3.9}$$

Supposing that the output noise is due to the feedback resistor noise, the output voltage noise and its root mean square value are:

$$V_{o,n}(s) = -R_f \, i_{n,R_f} \tag{3.10}$$

$$V_{o,n,rms} = R_f \, i_{n,R_f,rms} = \sqrt{4kTR_fB} \tag{3.11}$$

Where:

k is the Boltzmann's constant, equal to $1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}}$.

T is the temperature in Kelvin degrees.

B is the equivalent single-sided noise bandwidth of the circuit [Hz], defined as,

$$B = \int_0^{+\infty} \left[\frac{G(s)}{G(0)}\right]_{s=j\omega} \frac{d\omega}{2\pi} \tag{3.12}$$

The dynamic range is:

$$DR = \frac{I_{in,MAX}}{I_{in,MIN}} \tag{3.13}$$

Supposing the the minimum detectable amplitude of V_o corresponds to a SNR equal to 1, we have:

$$I_{in,MIN} = \frac{V_{o,n,rms}}{R_f} \tag{3.14}$$

And substituting, the DR can be expressed as:

$$DR = \frac{I_{in,MAX}}{V_{o,n,rms}/R_f} = \frac{V_{o,MAX}}{R_f} / \sqrt{\frac{4kTB}{R_f}} = \frac{V_{o,MAX}}{\sqrt{4kTR_fB}} \tag{3.15}$$

From which we get:

$$DR\,B = \frac{V_{o,MAX}\,I_{in,MIN}}{4kT} \tag{3.16}$$

Hence the dynamic range is inversely proportional to the circuit bandwidth, if we keep the minimum detectable current constant. [28]

This can be intuitively explained with the following argument: if we increase the circuit bandwidth, R_f has to be increased of the same factor to keep the minimum detectable current i_{n,R_f} constant. The amplifier will therefore saturate for a input current I_{in} which is a factor $1/R_f$ lower. Hence, the dynamic range is reduced of the same factor, giving a constant $DR\,B$ product.

For example, if $|I_{in,MAX}| = 100\,\text{mA}$, $T = 300\,\text{K}$ and $V_{o,MAX} = 10\,\text{V}$, requiring a dynamic range of 9 decades leads to a bandwidth of approximatively 60 Hz and $R_f = 100\,\Omega$.

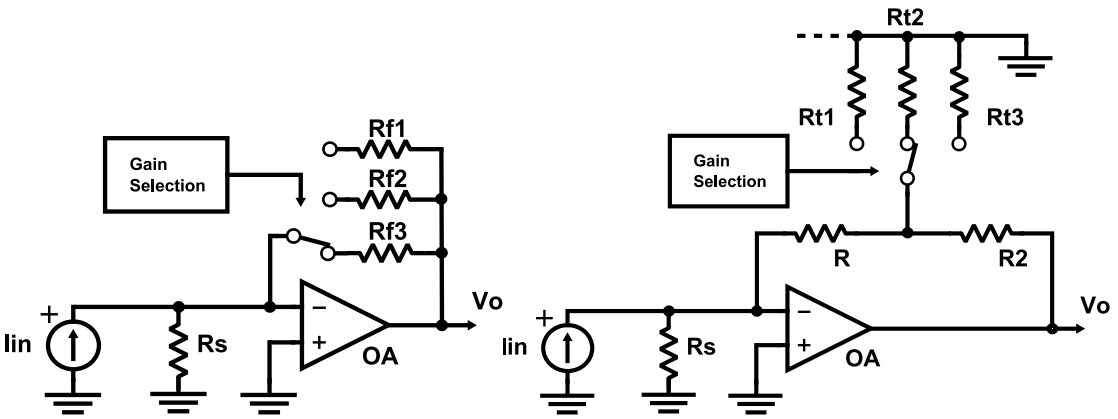
The maximum output voltage $V_{o,MAX}$ may be increased changing the value of the supplies, on the other hand, this would increase the power dissipation of the circuit.

A different type of circuit is necessary for wideband high dynamic range measurements.

The possibilities to overcome the problem may be: taking into account the shape of the input signal to filter effectively the noise, thus reducing the minimum detectable signal, as described in chap. 4, using amplifiers with a compressive input-output characteristic (sect. 3.2, 3.3, 3.4, 3.5), multiple linear amplifiers selecting the desidered output (sect. 3.6) and converting the signal to a variable that is not affected by the limits the same limits of a voltage level (sect. 3.8).

3.2 Transimpedance amplifier with switched gain

A direct extension of the circuit that has been previously considered can be obtained switching the feedback resistor according to the level of the input signal, as schematically illustrated in fig. 3.3a.



(a) Switched feedback resistor (b) Switched T-network

Figure 3.3: Transimpedance amplifiers with switchable gain: simplified schematic.

Once a feedback resistor is connected, the circuit is the same as the one considered in sect. 3.1. The stability of this configuration may be compromised by the stray capacitance due to the signal source and the input of the operational amplifier. [2]

The amplifer is therefore reviewed and greater emphasis is given to the stability issues. The circuit is shown in fig. 3.4.

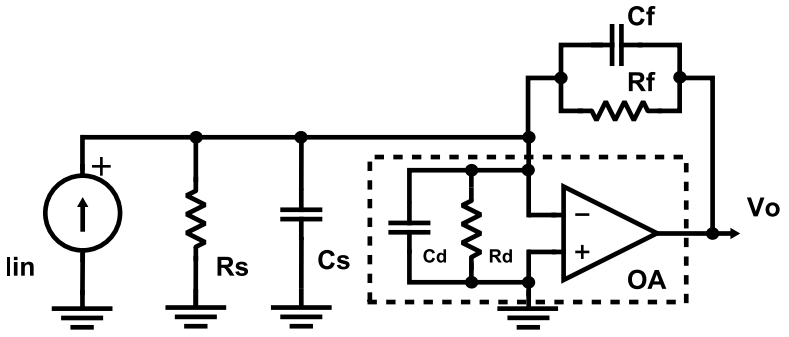


Figure 3.4: Transimpedance amplifier with stray capacitances

The feedback transfer ratio is equal to:

$$\beta = -\frac{R_d \,/\!/\, R_f \,/\!/\, R_s}{R_f} \frac{1 + sC_fR_f}{1 + s(C_d + C_f + C_s)(R_d \,/\!/\, R_f \,/\!/\, R_s)} \tag{3.17}$$

The expressions for its characterstic values are as follows:

$$\beta(0) = -\frac{R_d \,/\!/\, R_f \,/\!/\, R_s}{R_f} \tag{3.18}$$

$$\omega_z = \frac{1}{C_fR_f} \tag{3.19}$$

$$\omega_p = \frac{1}{(C_d + C_f + C_s)(R_d \,/\!/\, R_f \,/\!/\, R_s)} \tag{3.20}$$

$$\lim_{\omega \to +\infty} \beta(s)|_{s=j\omega} = \frac{C_f}{C_d + C_f + C_s} \tag{3.21}$$

As C_s depends on the source and its connecting cables, it is not known exactly, C_f may be specified to ensure stability of the system, which shall be verified for every resistor composing the $\{R_{fn}\}$ set. While increasing C_f is straightforward, decreasing it under the limit provided by the stray capacitance of the feedback resistor R_f requires special layout techniques. For example, replacing R_f with two resistors of half its value connected in series, assuming that the stray capacitance doesn't change, reduces the overall capacitance seen between input and output node of a factor two.

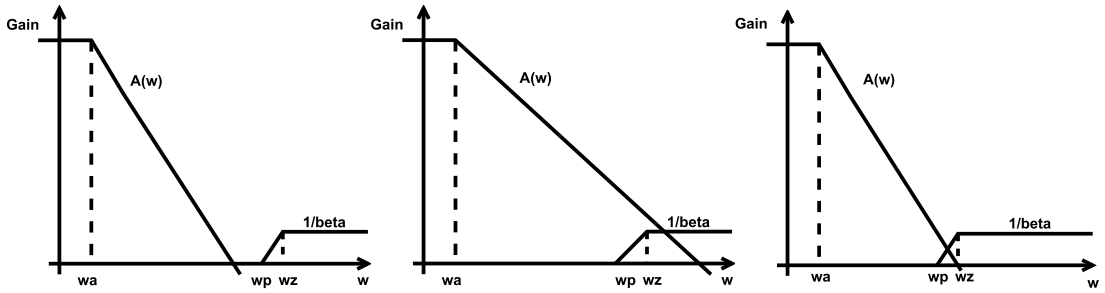
The phase margin is equalt to 45° for:

$$C_f = \frac{1 + \sqrt{1 + 4(C_d + C_s)GBWR_f}}{2GBWR_f} \tag{3.22}$$

The last result may be simplified to:

$$C_f = \sqrt{\frac{C_d + C_s}{GBWR_f}}, \quad for \quad 4(C_d + C_s)GBWR_f \gg 1 \tag{3.23}$$

The result corresponds to the bode plot in fig. 3.5b, a case in which $GBW > \omega_p, \omega_z$ is shown in fig. 3.5a, while fig. 3.5c depicts an unstable configuration.



(a) Stable, 1 of 2. (b) Stable, 2 of 2. (c) Unstable.

Figure 3.5: Noise gain for the transimpedance amplifier

A stable configuration has a transimpedance gain equal to:

$$\frac{V_o(s)}{I_{in}(s)} = Z_T(s) = -R_f \frac{A_0\omega_a\omega_x}{s^2 + (\omega_p + \omega_a + \omega_a\frac{\omega_x}{\omega_z}A_0)s + \omega_a\omega_p + A_0\omega_a\omega_x} \tag{3.24}$$

A_0 is the low frequency gain of the operational amplifier.

ω_{pa} is the angular frequency of the first pole of the transfer function of the operational amplifier [rad s^{-1}]. Hence $GBW = A_0\omega_a$

ω_x is equal to $1/C_f(R_d \mathbin{/\!/} R_f \mathbin{/\!/} R_s)$, [rad s^{-1}]

Comparing eq. 3.24 to the canonical form for a second order system (3.25), we find:

$$T(s) = \frac{T_0}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3.25}$$

ω_n natural frequency of the system:

$$\omega_n = \sqrt{A_0\omega_a\omega_x} \tag{3.26}$$

ξ damping factor:

$$\xi = \frac{1}{2}\left(\frac{\omega_p + \omega_a}{\omega_n} + \frac{\omega_n}{\omega_z}\right) \tag{3.27}$$

If the gain is considered infinite ($A_0 \to +\infty$), then the transfer impedance $Z_T(s)$ reduces to its ideal counterpart:

$$\lim_{A_0\to+\infty} Z_T(s) = -\frac{R_f}{1 + sC_fR_f} \tag{3.28}$$

Which in turn reduces to the result found in sect. 3.1, if C_f is trascurable.

The output voltage due to DC errors is equal to:

$$V_o = (-I_{in} + I_b)R_f + V_{os}\left(1 + \frac{R_f}{R_s \,/\!/\, R_d}\right) \tag{3.29}$$

I_b is the input bias current of the operational amplifier. [A]

V_{os} is the input offset voltage of the operational amplifier. [V]

A fundamental drawback of this solution is that high value resistors are required in order to provide high gain for low currents. For example, to have a 1 V output with a 1 nA current input, a 1 GΩ resistor is required. This kind of resistors are usually made from carbon film or deposit ceramic oxide, glass-sealed to prevent their value from changing because of humidity and are bulky and expensive.[52]

This problem is overcome by the transimpedance amplifier with a T-network feedback shown in fig. 3.3b.

It can be shown that the output voltage corresponding to a DC input, including the effect of the input voltage and the input bias current, is:

$$V_o = \left(-I_{in} + I_b + \frac{V_{os}}{R_s}\right)\left[R\left(1 + \frac{R_2}{R_{tn}}\right) + R_2\right] + V_{os} \tag{3.30}$$

R_{tn} is the selected resistor among those available for setting the gain. [Ω]

As some of the current is flowing towards ground, the sensitivity is augmented avoiding the usage of high-value resistors. From eq. 3.30, the transfer is linearly dependent on a term $(1 + R_2/R_{tn})$, hence decreasing R_{tn} provides an increased transimpedance gain. On the other hand, the circuit is affected by a higher noise gain and the loop gain is decreased. The contribution of the offset voltage, bias current and root mean value of the output voltage due to the input current and voltage noises are also linearly dependent on the same factor, deteriorating the DR.

These circuit architectures require a system to select the appropriate gain. An effortless solution is setting the gain beforehand according to the expected signal from each detector. The signal level expectations may be used to preset the configuration of the interface electronics, avoiding

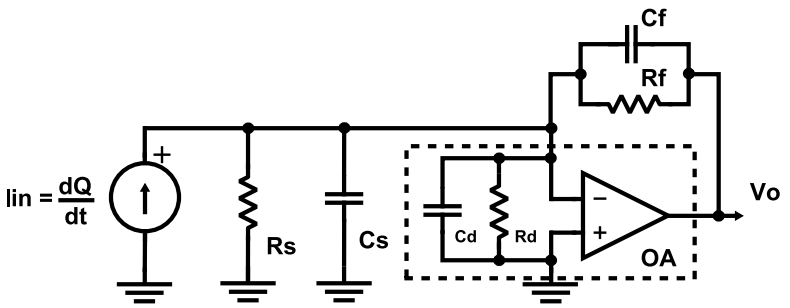


Figure 3.6: Charge amplifier

output saturation. The dynamic range of each configuration is the same as previously considered for the transimpedance amplifier, only the maximum and minimum current are scaled according to the gain.

A more elaborate switching system may be implemented, so that the gain changes with the input signal level. This leads to several more difficulties: the input signal has edges with rising times of some tens of nanoseconds, which would require an equally fast gain switching. On the other hand, rapidly switching the gain value will produce spurious spikes at the output.

The output due to voltage offset and offset current at the input is variable, as the gain is. In addition, the stability depends on the gain configuration, each of them has to be stable.

3.3 Charge amplifier

A charge amplifier[3] provides an output signal proportional to the electric charge produced by a device connected to its input. Its is intended to be used with a sensor that yields an output charge proportional to a measured physical quantity.

The schematic of a charge amplifier is the same as the one of the transimpedance amplifier shown in fig. 3.4, only in this case, the feedback capacitor is the element that provides the desidered functionality and R_f is composed by the shunt resistance of the capacitor (representing the leakage current) and any additional resistor added to ensure direct current stability.

Therefore, it is possible to analyze the stability of the circuit through the noise gain found in sect. 3.2.

[3]In this section, the charge amplifier is considered in its simpler configuration, ie with a fixed integration capacitor. About the possibility of switching the capacitor to modify the gain, the remarks concerning the switching of the feedback resistor in a transimpedance amplifier apply.

From eq. 3.24, we can derive the closed loop transfer function Being $I_{in} = Q'_{in}$, applying the Laplace Transform to both sides we get:

$$\mathcal{L}(I_{in}(t))(s) = \mathcal{L}(Q'_{in}(t))(s) = s\mathcal{L}(Q_{in}(t))(s) = sQ_{in}(s) \tag{3.31}$$

Substituting in 3.24, we get:

$$\frac{V_o(s)}{Q_{in}(s)} = -\frac{1}{C_f}\frac{sA_0\omega_a\frac{\omega_x}{\omega_z}}{s^2 + (\omega_p + \omega_a + \omega_a\frac{\omega_x}{\omega_z}A_0)s + \omega_a\omega_p + A_0\omega_a\omega_x} \tag{3.32}$$

All the parameters are the same as those introduced in sect. 3.2.

The transfer function has two poles and a zero. If the two poles are distant from each other enough, the following approximation can be used to estimate their position: at low frequency eq. 3.32 simplifies to:

$$\frac{V_o(s)}{Q_{in}(s)} = -\frac{1}{C_f}\frac{sR_fC_f}{sC_fR_f + 1} \tag{3.33}$$

While at higher frequencies,

$$\frac{V_o(s)}{Q_{in}(s)} = -\frac{1}{C_f}\frac{A_0\omega_a\frac{\omega_x}{\omega_z}}{s + (\omega_p + \omega_a + \omega_a\frac{\omega_x}{\omega_z}A_0)} \tag{3.34}$$

Therefore, the positions of the poles are approximatevely:

$$\omega_l \approx \frac{1}{C_fR_f} \tag{3.35}$$

$$\omega_h \approx \frac{GBW\omega_p}{\omega_z} \approx GBW\frac{C_f}{C_f + C_s + C_d} \tag{3.36}$$

The gain between the two poles can be estimated as $-1/C_f$. Fig. 3.7 shows a bode plot of the transfer function, superimposed to the transfer function of the operational amplifier, $A(\omega)$.

The output due to the DC errors has the same expression as the one affecting the transimpedance amplifier (eq. 3.29).

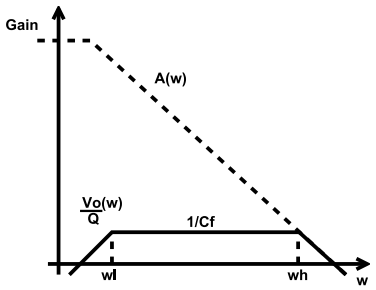


Figure 3.7: Bode plot of the transfer function of a charge amplifier.

The output drift is a characteristic parameter of the charge sensitive amplifier and it takes into account the effect of the discharge of the feedback capacitor C_f through its leakage resistor, R_f, and the effect of the input bias current of the operational amplifier, I_b on the output. It is expressed by the following relationship:

$$OD = \frac{V_o}{C_f R_f} + \frac{I_b}{R_f} \tag{3.37}$$

The feedback capacitor C_f is a key element in this design. In order to obtain a large sensitivity, C_f should be kept small, but at the same time, reducing the feedback capacitor decreases ω_h and increases ω_l, deteriorating the transfer function and potentially undermining the stability of the circuit. To prevent gain drift, C_f should be as stable as possible. Moreover, it should be chosen among those who have a low leakage. Suitable dielectrics are polypropylene and polystyrene, for example.

To improve the stability of the circuit, the signal may be connected to the inverting input of the operational amplifier through a resistor. [2] The input resistor also protects the input, limiting the maximum current flowing into the charge amplifier when a voltage source is connected to the input. It introduces a pole at an angular frequency equal to:

$$\omega_{p1} \approx \frac{1}{C_s R_x} \tag{3.38}$$

R_x is the resistor connected in series with the input.

This pole sets the high frequency limit, if $\omega_{p1} < \omega_h$.

A FET input operational amplifier should be used to reduce errors, since the input bias current of the operational amplifier is summed to the signal current.

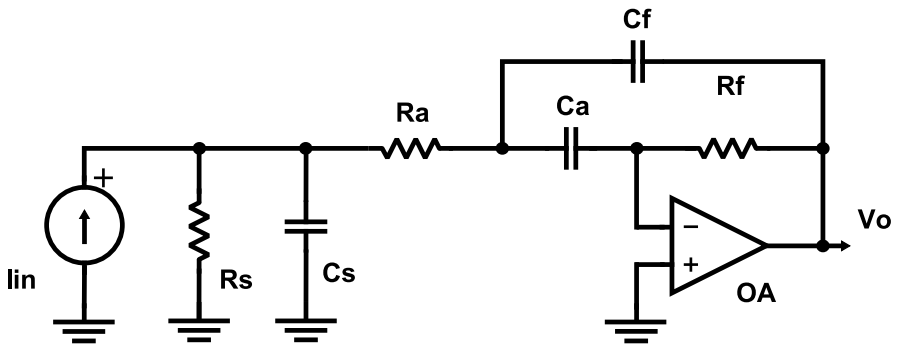


Figure 3.8: Alternative charge amplifier

A discrete resistor shunting the feedback capacitor may be omitted, but, in that case, a switch or another suitable reset mechanism should be included in the circuit to prevent saturation, as the already mentioned bias currents would drive the output voltage to one of the supply rails in absence of signal. When the feedback resistor is included, there is a trade-off between low frequency response – as R_f directly affects the position of ω_l – and DC offset voltage at the output. A high-value resistor determines a large DC error at the output, while a low-value resistor moves the lower end of the transfer function to higher frequencies.

3.3.1 Alternative implementations of a charge amplifier

An alternative charge amplifier is shown in fig. 3.8 [34]. This design has some key differences from the previous one: the feedback resistor R_f provides a DC path for the input bias current I_b without affecting the charge stored on the feedback capacitor C_f.

The transfer function is:

$$\frac{V_o(s)}{Q_{in}(s)} = -\frac{1}{C_f}\frac{sR_fC_a}{(1+sR_aC_s)\left(1+\frac{C_a}{C_f}+sR_fC_a\right)+\frac{C_s}{C_f}} \tag{3.39}$$

The location of the two poles may be approximated with the following expressions, if they are situated at a distance of at least one decade.

$$\omega_l \approx \frac{1}{\frac{C_aC_f}{C_a+C_f+C_s}R_f} \tag{3.40}$$

$$\omega_h \approx \frac{1}{R_aC_s} \tag{3.41}$$

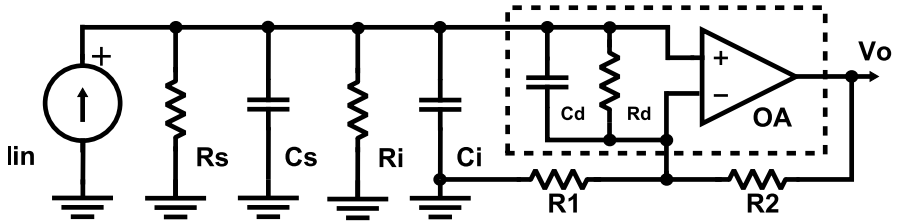


Figure 3.9: Charge amplifier without virtual ground at the input.

In the range between ω_l and ω_h, the transfer function is $1/C_f$. Therefore, the introduction of R_a and C_a allows greater freedom in the independent choice of the frequency response and sensitivity.

Being AC coupled, the input of the amplifier is protected against DC overloads.

It is also possible to integrate passively the input current on a capacitor and the resulting voltage may be successively amplified through an amplifier with an high input resistance. This setup is shown in fig. 3.9.

Ideally, all the input current flows in C_i and it is integrated. The voltage across the integrating capacitor is the amplified of a factor $G_v(s)$, given by eq. 3.42, where the input resistance and capacitance of the operational amplifier are not taken into account. To provide a path for the input bias current, R_i has been added to the circuit.

$$G_v(s) = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + s/\omega_{pa}} \tag{3.42}$$

The pole can be shown to be:

$$\omega_{pa} = GBW \frac{R_1}{R_1 + R_2} \tag{3.43}$$

On the whole, the transfer function of the charge amplifier is:

$$\frac{V_o(s)}{Q_{in}(s)} = \frac{1}{C_i + C_s} \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + s/\omega_{pa}} \frac{s(R_i + R_s)(C_i + C_s)}{1 + s(R_i + R_s)(C_i + C_s)} \tag{3.44}$$

The stability of the operational amplifier is easily ensured and this design has potentially a very wide bandwidth, depending on the choice of the operational amplifier. On the other hand, this setup is more sensitive to the characteristics of the current source and the length of the cable. As it can be seen in eq. 3.44, the effective capacitance that integrates the input signal is composed

of the capacitor C_i and the cable and source capacitance C_s. Moreover, the lower frequency pole is also set by the the current source and therefore, a different source or a different cable length directly affects the gain.

3.4 Amplifier with a nonlinear characteristic

An amplifier with a defined nonlinearity may also be employed; linear frequency independent input-output relationships arise from the use of components with a linear frequency independent characteristic at the input or in the feedback loop of an amplifier. As reactive componets produce frequency dependent relationships, nonlinear elements determine a nonlinear relationship.

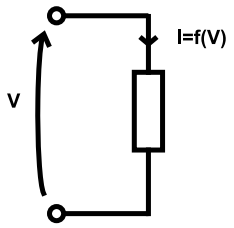


Figure 3.10: Nonlinear element.

Both compressive and expanding characteristics may be implemented – the former being suitable for our purposes – and the relationship may be an arbitrary or a well known mathematical function. Logarithmic amplifiers are considered in sect. 3.5.

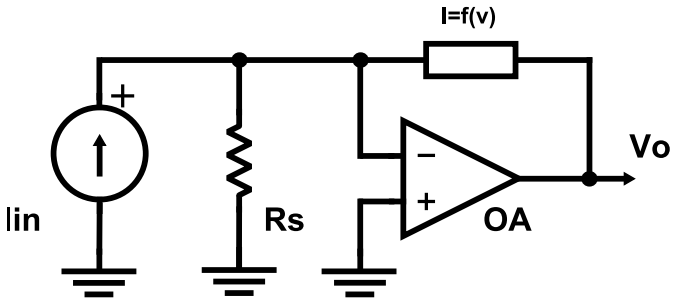


Figure 3.11: Operational amplifier with nonlinear feedback path.

A key role is played by the element providing the required nonlinearity: it is required to adhere accurately to the ideal characteristic over a wide range of currents with low temperature sensitivity. Such components may be constituted by a single nonlinear component or by a network of linear and nonlinear elements, where the nonlinear elements are used as switches.

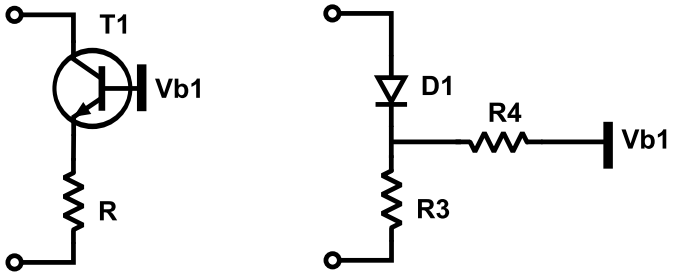


Figure 3.12: Possible building blocks for nonlinear feedback networks

Two examples of networks of the latter type are shown in figure 3.12. Referring to the right-hand figure, the external bias voltage and the resistor set the voltage required to turn on the diode. A very similar results may be achieved with a network based on a bipolar transistor, as seen in the left-hand figure.

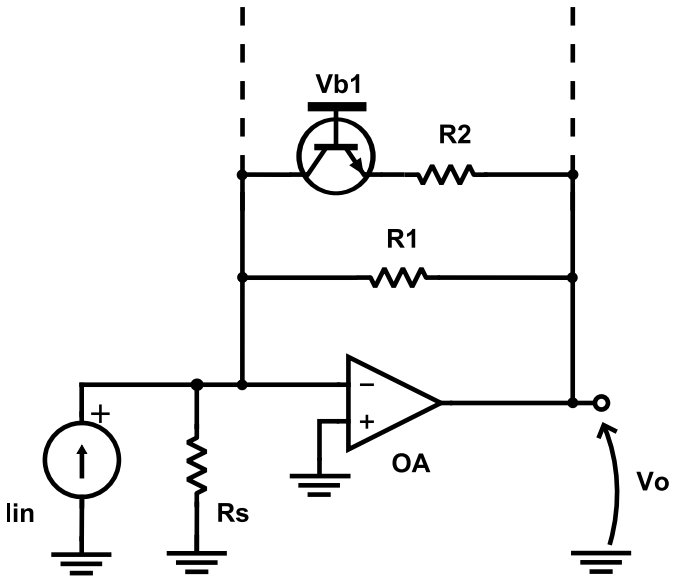


Figure 3.13: Nonlinear amplifier using the network shown in fig. 3.12

A nonlinear amplifier is depicted in fig. 3.13. The ideal characteristic shows a transconductance gain equal to R_1 until the output reaches $V_{bi} - V_{BE}$, where V_{BE} is the approximative forward bias required to turn on the diode, after that the gain is $R_1 \ /\!/ \ R2$. The same happens for the successive breakpoints.

A concept circuit has been simulated with SPICE, using the THS4631 operational amplifier and 2N3716 bipolar junction transistor. The approximate gain vales, the the threshold currents and the bias voltages are shown in tab. 3.1. The results are shown in fig. 3.15 and 3.14.

Threshold current	Resistor value	Gain	Bias voltage
None	20 MΩ	20×10^6 V A^{-1}	None
100 nA	200 kΩ	200×10^3 V A^{-1}	−1.8 V
10 µA	2 kΩ	2×10^3 V A^{-1}	−4.7 V
1 mA	20 Ω	20 V A^{-1}	−6.7 V

Table 3.1: Thresholds, gains and bias voltages for the simulated nonlinear amplifier, simplified schematic in fig. 3.13.

As expected, the simulations show that output and breakpoint voltages are dependent on the temperature.[4]

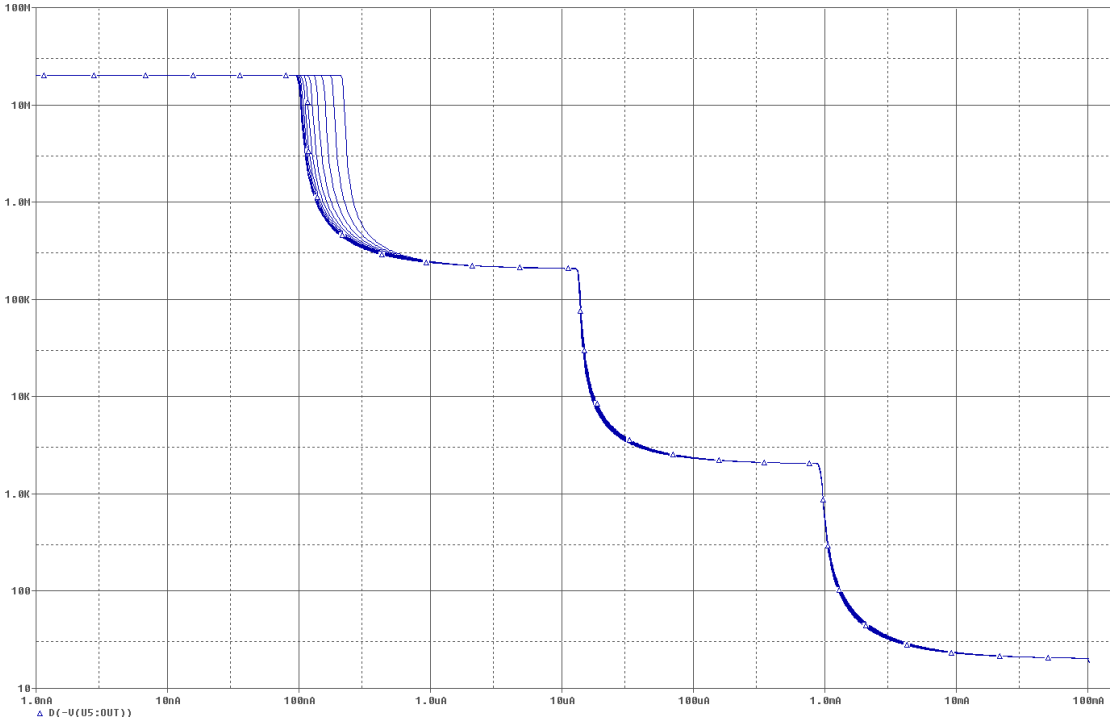


Figure 3.14: Transimpedance gain versus input current for temperatures from 0 °C to 70 °C, step 5 °C, lower temperatures correspond to lower thresholds.

The circuit is nonlinear, the stability has to be verified for all operating points.

Another important issue that has to be taken into account is the fact that the thresholds on each board have to be as accurate as possible in order to be able to compare different outputs from different boards.

[4]For a silicon diode, with a constant current applied, the voltage across a silicon diode will decrease by approximately 2 mV °C^{-1} over the normal operating range (0 °C - 70 °C).

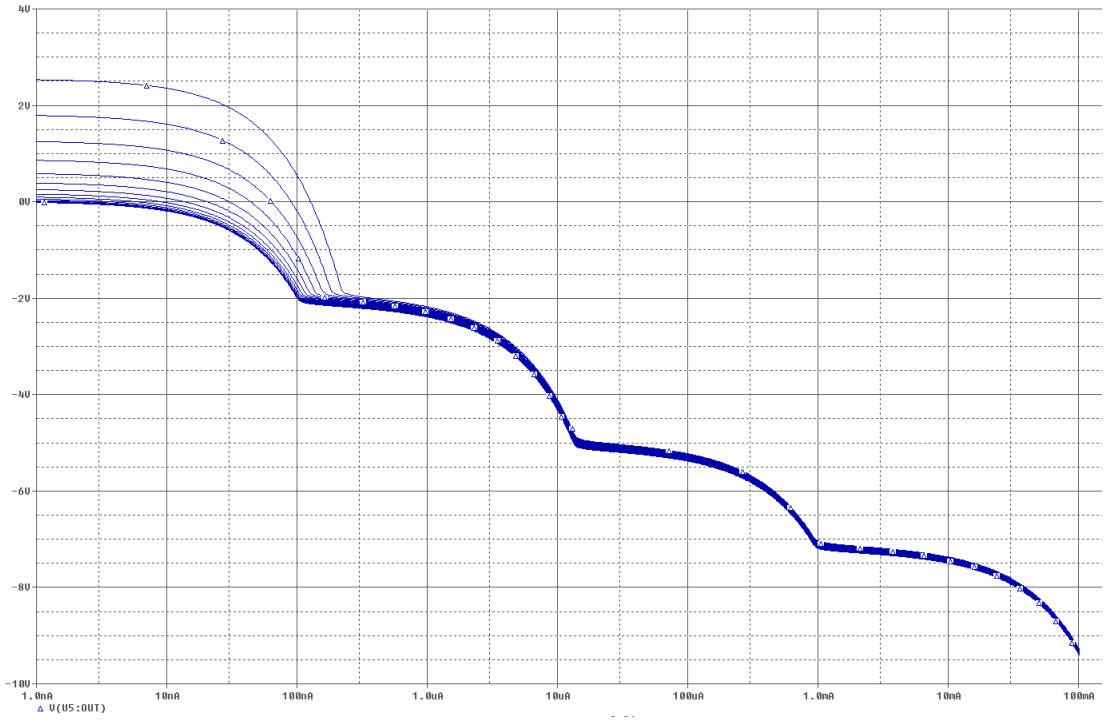


Figure 3.15: Output voltage versus input current for temperatures from 0 °C to 70 °C, step 5 °C, lower temperatures correspond to lower thresholds.

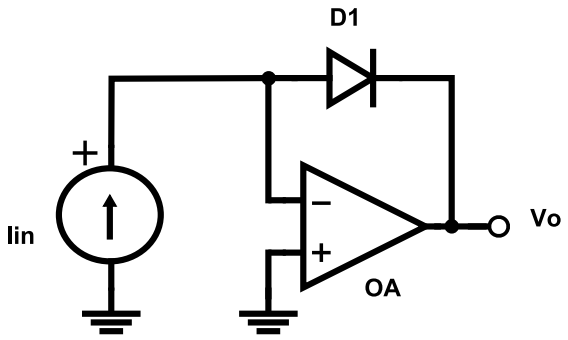


Figure 3.16: Logarithmic amplifier

3.5 Logarithmic Amplifier

Instead of composing the input output characteristic of the circuit through several linear intervals, it is possible to use a amplifier that has a non-linear compressive characteristic. The relationship between input and output has to be precisely known, in order for the result to be meaningful.

These amplifiers rely on a accurate relationship between voltage and current across a element, to perform the conversion between the input and the output signal. An example of such a component is a PN diode or a diode connected bipolar transistor.

In a logarithmic amplifier, the input and output variables are ideally related by the following equation:

$$V_o(I_{in}) = V_\alpha \ln\left(\frac{I_{in}}{I_o}\right) \tag{3.45}$$

I_{in} is the input current [A]

I_o is the intercept current, for which $V_o(I_o) = 0\,\mathrm{V}$ [A]

V_α is the volts-per-decade factor [V]

A simple logarithmic amplifier is composed by an operational amplifier and a diode connected in feedback, as shown in fig. 3.16 [4].

We'll show now that the feedback diode performs the required conversion.

The output voltage is from the considered circuit is:

$$V_o = -V_D(I_{in}) \tag{3.46}$$

Assuming that the diode has the current-voltage characteristic:

$$I_D = I_s \left[\exp\left(\frac{qV_D}{kT}\right) - 1 \right] \approx I_s \exp\left(\frac{qV_D}{kT}\right) \tag{3.47}$$

I is the current through the junction [A]

I_s is the reverse saturation current [A]

V_D is the voltage across the junction [V]

q is the magnitude of the electronic charge [1.6×10^{-19} C]

k is the Boltzmann constant [1.38×10^{-23} J K^{-1}]

T is the temperature in Kelvin degrees.

At room temperature, kT/q is equal to approximatively 26 mV, hence for voltages greater than 100 mV the exponential term predominates, inverting the relationship and substituting in eq. 3.46, we get the following expression:

$$V_o = -\frac{kT}{q} \ln\left(\frac{I_{in}}{I_s}\right) \tag{3.48}$$

Therefore, the amplifer has a intercept current equal to the diode reverse saturation current and a volt-per-decade factor equal to the thermic voltage, for every decade of input current change, the output voltage changes of a factor equal to kT/q.

There are several inconvenients that make a simple and attractive circuit such as the one in fig. 3.16 inappropriate for logarithmic current to voltage conversion.

The output voltage depends on the temperature. This dependance not only explicit in eq. 3.48 but also due to the variation of the reverse saturation current, which approximatively doubles every 10 degrees change in temperature.

Moreover, the relationship in eq. 3.47 doesn't describe accurately the behaviour of most diodes. To better describe the actual devices, eq. 3.47 has to be modified to introduce a ideality factor m [33]:

$$I_D = I_s \left[\exp\left(\frac{qV_D}{mkT}\right) - 1 \right] \tag{3.49}$$

For low currents, the trap-assisted recombination in the depletion region has an important effect on the overall current through the diode. In this region, the ideality factor is equal to two.

Increasing slightly the current, the effect of recombination is less important and the ideality factor m is approximatively unitary. In this region the voltage-current relationship resembles closely the one described in eq. 3.47.

For even higher currents, the current becomes limited by high injection effects and by the series bulk resistance.

High injection occurs when the injected minority carrier density exceeds the doping density, and therefore in it will occur first in the lowest doped region of the diode. The value of the forward voltage at which this occurs is:

$$V_D = \frac{2kT}{q} \ln\left(\frac{N_d}{n_i}\right) \tag{3.50}$$

n_i is the intrinsic carrier concentration $[cm^{-3}]$

N_d is the lowest doping concentration $[cm^{-3}]$

In this region, the ideality factor is again equal to two.

For higher bias voltages, the current no longer increases exponentially with voltage, but instead, its increase is linear due to the series resistance of the diode. The series resistance is composed of the contact resistance between the metal and the semiconductor,the resistivity of the semiconductor bulk and the resistance of the connecting wires.

In this region, the current-voltage characteristic may be approximated as:

$$V_D = V_D^* + I_D R_s \tag{3.51}$$

V_D^* is the forward bias voltage at which the series resistance becomes dominant [V]

R_s is the series resistance [Ω]

This behaviour makes the compensation of temperature variations more difficult because devices with matched ideality factors are required. The discrepancies between the ideal logarithmic and the actual characteristic of diodes can be partially overcome using diode-connected bipolar transistors.

An example of desensitization of the output from the variation of I_s is shown in fig. 3.17, whose voltage output is ideally given by the following relationship:

$$V_o = -\frac{kT}{q}\frac{R_1 + R_3}{R_3}\ln\left(\frac{I_{in}}{I_{ref}}\right) \tag{3.52}$$

It should be noticed that if the compensation was perfect, the output would still be linearly dependant on the absolute operating temperature (PTAT). By adding subsequent opportunely temperature compensated circuitry, for example if the value of R_3 is proportional to the temperature, the temperature dependence can be virtually eliminated, yielding the relationship shown in eq. 3.45. In addition, the elements introduced to perform the compensation also give the possibility of controlling the voltage-per-decade factor, enabling the designer to set the output swing according to the intended application.

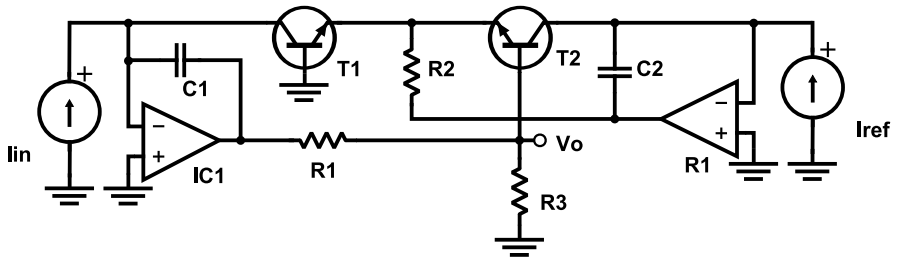


Figure 3.17: Improved logaritmic amplifier. [31]

To accurately compensate the temperature variation, rather elaborate circuits may be employed, in which a good matching and voltage or current references are required. Such circuits are less expensive and achieve better results if integrated. Tab. 3.2 shows a comparison of various integrated logarithmic amplifers available on the market. They were deemed unsuitable for this project because of their low bandwidth, especially with low input signal, due to the high value of the emitter at low input currents, the single polarity of the input current and additionally the low maximum input current.

3.6 Multiple stages transimpedance amplifier and single stage with current splitting

A direct extension of the circuit described in sect. 3.2 is a transimpedance amplifier with multiple gain stages. Instead of switching the feedback resistor, it is possible to generate multiple output signals and selecting the greatest unsaturated output (fig. 3.18).

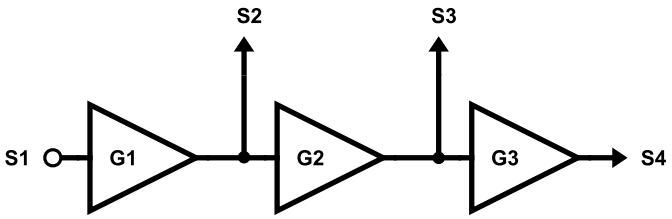


Figure 3.18: Multiple stages amplifier

If all the outputs are sampled, the actual choice can be made digitally, avoiding the switching issues.

Each gain stage adds its noise and offset to the following outputs. The degradation of the quality of the input signal with respect to the amplified output signal is usually expressed through the Noise Factor (F). Often the noise factor is expressed in decibels, in this case it is called Noise Figure.

By definition:

$$F_n = \frac{SNR_{in}}{SNR_{out}} \tag{3.53}$$

The overall Noise Factor for a cascade of M amplifiers characterized by a gain equal to G_i and a noise factor equal to F_i (where i is the number of the stage) can be evaluated through Friis' equation:

$$F_M = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_M - 1}{\prod_{j=i}^{M-1} G_j} \tag{3.54}$$

Under the same hypothesis, the DC output offset of the chain $V_{OS,in,i}$ – evaluated with zero input signal – is given by:

$$V_{OS,N} = \sum_{i=1}^{N} (V_{OS,out,i} \prod_{j=i}^{N} G_j) \tag{3.55}$$

The first stages, the very first one in particular, appear to be critical and should be designed carefully. Moreover, in the case of a low input signal, where the corrisponding output is located at the end of the chain, the signal is affected by the greatest offset and noise. This limits the number of stages that can compose the chain.

Another possibility would be to amplify separately the input signal with different gain stages, instead of cascading them. Since the input signal is a current, in order to do implement this amplifier, it is necessary to split the current in different ratios and to feed them to the different amplifiers, as shown in fig. 3.19.

In fig. 3.19, the splitting ratios $\{A_i\}$ have the following properties:

$$A_i > 0 \quad \forall i \tag{3.56}$$

$$\sum_i A_i = 1 \tag{3.57}$$

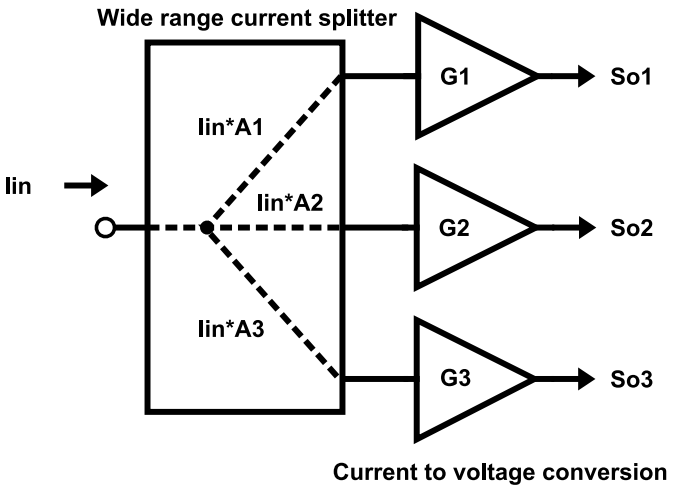


Figure 3.19: Current divider and multiple amplifiers

An advantage of this setup is that the current to voltage converters are staightforward to implement, since the dynamic range required for each one of them is less than the dynamic range of the whole system. The difficulty lays in the implementation of a current splitter able to provide the required division with high accuracy over the whole dynamic range.

3.7 Direct digital acquisition

Another possibility that has been taken in consideration is integrating the current signal directly with a current input analog to digital converter (ADC).

For this setup, Texas Instruments' DDC112 has been considered.

The device has a dual switching integrator as pre-amplifier. While the input current signal is converted to a voltage in one integrator, the other is connected to the input of the ADC through an analog multiplexer and its output signal is digitized. The main benefit of this architecture allows a continuous current integration and therefore an acquisition without dead time.

The ADC is constituted by a delta-sigma A/D modulator, followed by a digital filter. Overall, the delta-sigma architecture used provides a 20 bits resolution without missing codes, the maximum DR is hence $2^{10} \approx 10^6$. A single 20-bit conversion is accomplished by the delta-sigma converter in approximately 220 µs and the overall conversion ratio is 3 kHz. [49]

Additional features of the IC are: the full scale range may be modified through the use of external capacitors and the converter also provides a serial output and a daisy chain, for system with many inputs.

The maximum full scale charge is equal to 1000 pC, given that the integration time is equal to 333.3 µs, the maximum average value of the input current over the integration time is 3 µA, which is too low for the target application of this work. Moreover, only single polarity currents can be detected.

3.8 Current to frequency converter

A current to frequency converter (CFC) transfers an input signal into a pulse train with a linear relationship between input current and output frequency.

The reason that leads to the choice of a CFC is the fact that is easier to measure time interval than a voltage or a current over a wide dynamic range. Moreover, the required integration reduces to pulse counting. The accuracy of integration depends on the number of pulses within a time interval.

A CFC is hence a wide range current controlled oscillator with an ideally linear current-to-frequency characteristic.

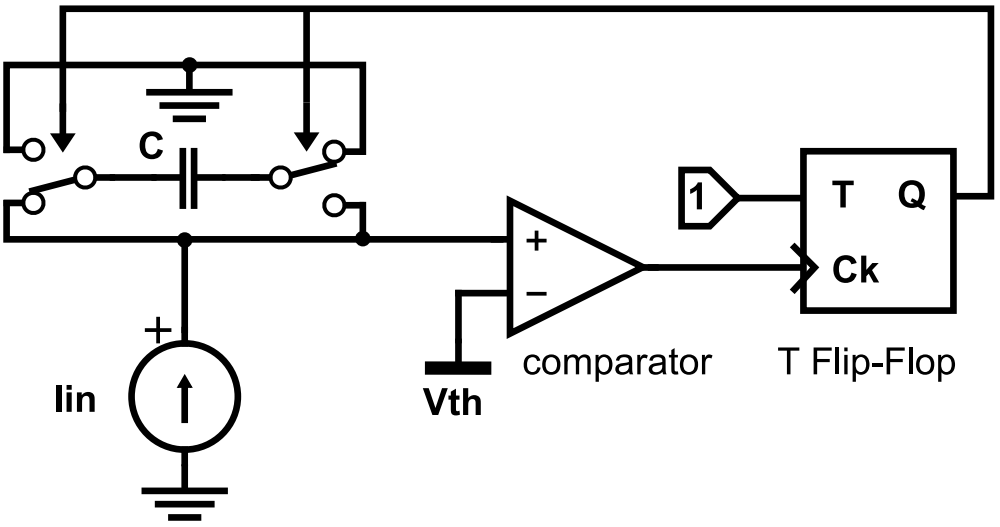


Figure 3.20: Current steering multivibrator, simplified schematic

3.8.1 Current steering multivibrator

A first architecture of CFC is shown in fig. 3.20, [55]. The input current charges a capacitor, whose voltage is compared to a reference (V_{th}) through a comparator.

Every time the threshold voltage is exceeded, the output of the comparator switches to the high level and triggers the toggle flip-flop. The output of the flip-flop switches to the complementary status and it changes the switches status, connecting the capacitor in the opposite direction. The same process repeats again.

The output variable is the switching frequency of the Q output of the flip-flop.

The voltage above the capacitor switches from $-V_{th}$ to $+V_{th}$. If the input current is constant and equal to I_{in}, the period of the waveform controlling the switches is $T_{out} = 2CV_{th}/I_{in}$, the corresponding frequency is hence $f_{out} = I_{in}/2CV_{th}$.

There are a number of issues to consider when designing such a circuit:

- The total input capacitance shunts the switching capacitor. The input capacitance is composed by the sensor output capacitance – which depends on the type of sensor being used – the cable capacitance, which varies with the type of cable and its length, and the capacitance associated with the circuit input.

It can be shown that this additional capacitance doesn't produce any error, but reduces the peak-to-peak output voltage swing of the waveform of a factor α given by:

$$\alpha = \frac{C}{C_p + C} \tag{3.58}$$

C is the switched capacitance value, as shown in fig. 3.20. $[F]$

C_p is the total shunting capacitance, as described above. $[F]$

The reduced voltage swing makes the circuit more sensitive to noise.

- If the total resistance seen from the input node to ground is equal to R_{in}, to reliably detect a current equal to I_{in}, the leakage current I_{leak}, whose maximum value is equal to V_{th}/R_{in}, has to be considerably less than I_{in}. If $V_{th} = 10\text{V}$, $I_{in,min} = 1\text{nA}$, R_{in} has to be greater than $10G\Omega$.
- The switching system has to be designed to ensure that in no occasion one of the switches can be closed before the other has been opened. Otherwise, part of the charge will be lost.

3.8.2 Charge balance integrator and derived architectures

A possibility to implement a CFC is integrating a current through an active integrator and periodically balancing the received charge with a predetermined reference charge.

Let's assume that the voltage across the capacitor that is responsible for the integration has a periodic steady state solution when there is a current $I(t)$ flowing through it. Then the current has to be periodic with the same period of $V(t)$ and its average value over an integer number of periods has to be zero.

In fact, if the following relationship is valid:

$$V(t_0) = V(t_0 + nT) \tag{3.59}$$

In eq. 3.59, T is the waveform's period, t_0 is an arbitrary time and $n > 0$ is an integer.

Then, from the constitutive relationship between voltage and current in a capacitor:

$$I(t) = C\frac{dV(t)}{dt} \tag{3.60}$$

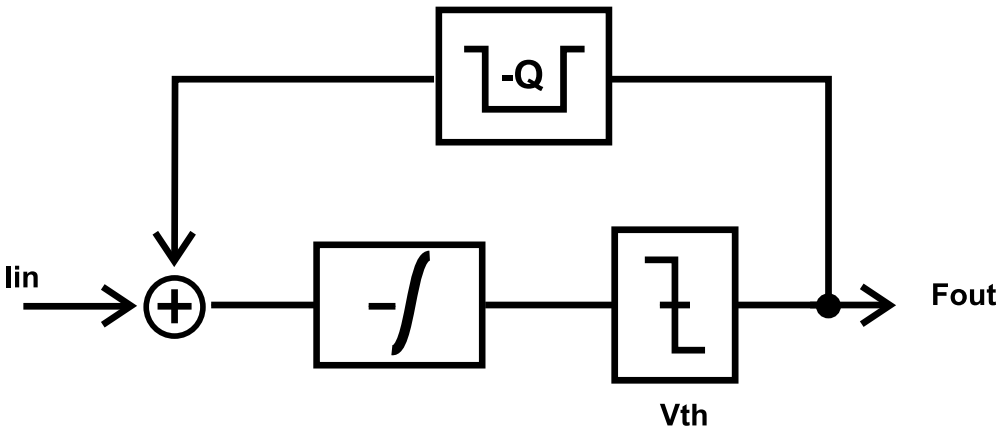


Figure 3.21: Diagram of an unipolar charge balance CFC.

It is immediately verified that the current is also periodic:

$$I(t_0) = C\frac{dV(t_0)}{dt} = C\frac{dV(t_0 + nT)}{dt} = I(t_0 + nT) \tag{3.61}$$

From eq. 3.60, we have:

$$V(t_0) = \int_{-\infty}^{t_0} \frac{I(\xi)}{C}\, d\xi \tag{3.62}$$

$$V(t_0 + nT) = \int_{-\infty}^{t_0+nT} \frac{I(\xi)}{C}\, d\xi \tag{3.63}$$

And from the periodicity condition 3.59:

$$V(t_0 + nT) - V(t_0) = \int_{0}^{nT} \frac{I(\xi)}{C}\, d\xi = 0 \tag{3.64}$$

Dividing by nT, we showed that the average current over an integer number of periods must be zero.

It can be also shown that if the current through a capacitor is periodic and has zero average value, then the voltage across it is periodic.

It is possible to build a measurement instrument based on this principle: we integrate the input current and every time the stored charge becomes equal to a defined threshold, a known charge is removed from the current integrator capacitor, ”balancing“ again the output [55]. The frequency of the occurrence of the balancing events, equal to the frequency of the output waveform, is then

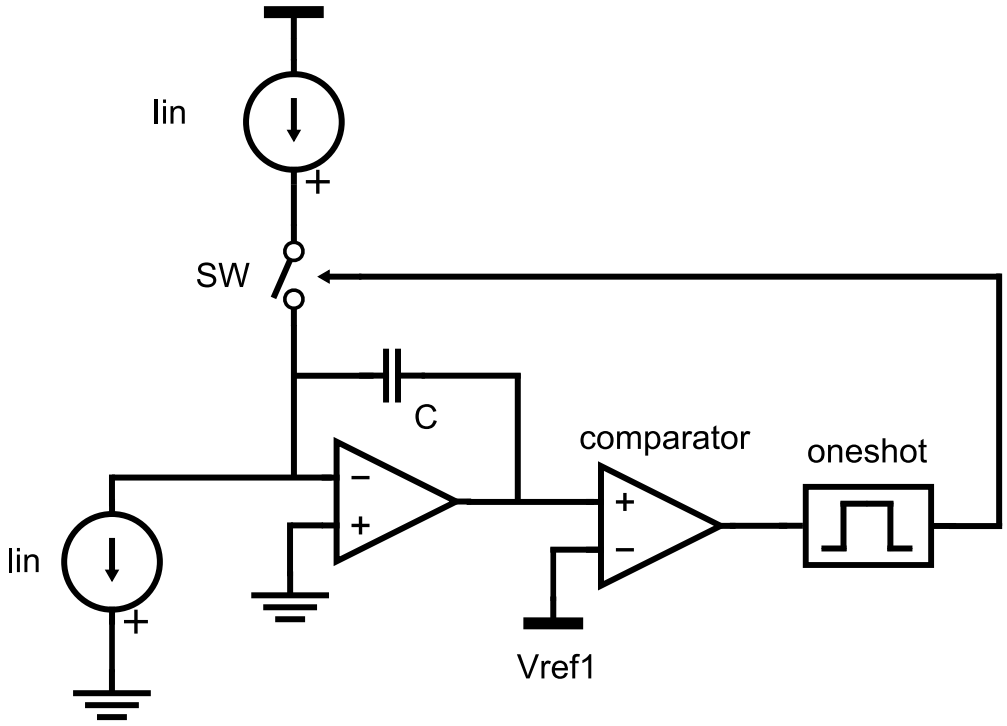


Figure 3.22: Possible implementation of the charge balance CFC.

measured. Hence, between two consecutive events, a charge Q_{REF} is added and removed from the capacitor. The diagram is shown in fig. 3.21 and a simplified schematic in fig. 3.22.

Measuring the period and knowing Q_{REF}, it is possible to evaluate the average value of the unknown current during the period.

Properties of the charge balance integrator

The main properties of a charge balance integrator are reviewed in the next sections.

Output frequency

We define as output frequency the distance between two consecutive raising edges of the square wave determined by the switching activity of the comparator. In addition, we assume that a periodic steady state solution exists and that the output frequency is constant.

Referring to fig. 3.22, in point of fact, the voltage threshold has to be crossed in order for a pulse to be generated at the output.

Under the assumption that the reference charge Q_{REF} is removed during a time interval equal to ΔT, this happens when:

$$-\int_0^{T-\Delta T} \frac{I_{in}(t)}{C}\, dt + V_o(0) = V_{TH} \tag{3.65}$$

V_o is the output voltage from the integrator $[V]$

ΔT is the time interval in which the charge Q_{REF} is removed $[s]$

$1/C$ is the proportionality constant $[F^{-1}]$

In eq. 3.65 an arbitrary cycle has been considered as reference. After the charge Q_{REF} is removed, the next cycle begins.

The output voltage of the integrator at the beginning of the next cycle, $V_o(0)$, can be expressed as:

$$V_o(0) = V_{TH} - \int_{\Delta T} \frac{I_{in}(t)}{C}\, dt + \frac{Q_{REF}}{C} \tag{3.66}$$

Because of the periodicity hypothesis, combining the previous expression with eq. 3.65:

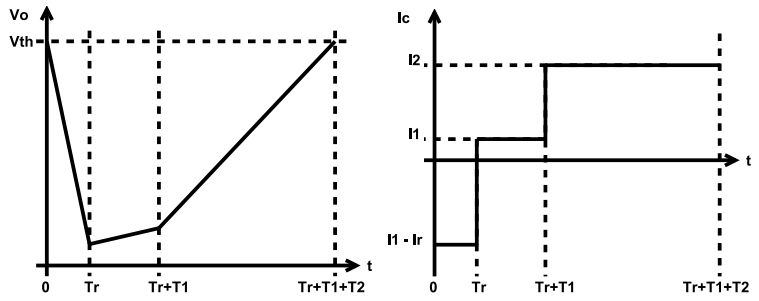
$$\int_0^T I_{in}(t)\, dt = Q_{REF} \tag{3.67}$$

Which is (3.64). Dividing by T and rearranging the terms:

$$f = \frac{\overline{I_{in}}|_T}{Q_{REF}} \tag{3.68}$$

$\overline{I_{in}}|_T$ is the average value of I_{in} during the time interval $(0, T)$ $[A]$

$f = 1/T$ is the output frequency $[Hz]$



(a) Output voltage of the integrator (b) Corresponding input current.

Figure 3.23: Response of the CFC to a current step.

Conversion time

The conversion time is the time required to have a rising edge at the output and it is a function of the integral value of the input current.

Hence, the conversion time depends on the input value. If we restrict our discussion to $I_{in}(t) = I_{in}$, a constant value, from eq. 3.68, it is apparent that it is necessary to wait an increasing time if I_{in} decreases,

$$T_{conv} = 1/f = \frac{Q_{REF}}{\overline{I_{in}|_T}} \tag{3.69}$$

Since in our application, there are different fixed measurement times, it is possible that the minimum current that has to be detected will not generate an output pulse in the given time interval. It is necessary to complement this system in order to provide output values at given time intervals. In this work, they will be referred to as fractional counts.

Settling cycles and response to an input current step

It is interesting to consider if, in the ideal charge balance CFC model considered in sect. 3.8.2, the considered architecture needs some cycles to settle to the correct value or if the acquisition is done completely in the active cycle and if the previous values of the input current produces an error in the successive cycle. From eq. 3.68, this should not happen.

For example, considering the circuit depicted in fig. 3.22, if the input current I_{in} is initially constant and equal to I_1 and successively switches to a value I_2 at after time T_1 from the last reset, then, since $V_o(0) = V_o(T_R + T_1 + T_2)$ (fig. 3.23a):

$$I_1 T_R - Q_{REF} + I_1 T_1 + I_2 T_2 = 0 \tag{3.70}$$

Rearranging and dividing by the total period:

$$\frac{1}{T_R + T_1 + T_2} = \frac{\overline{I_{in}(t)}|_{T_R+T_1+T_2}}{Q_{REF}} \tag{3.71}$$

The result confirms eq. 3.68 and shows that ideally the charge balance CFC is able to react to a current step in the active period and that the value of the previous conversion has no influence on the following one.

In the same way, a charge or voltage error in the active period has no influence on the following ones.

3.8.3 CFC with voltage reset of the integrating capacitor

It is challenging to design accurate current sources, especially if the dissipated power has to be kept to a minimum. Therefore, the possibility of resetting the voltage across the integrating capacitor is considered.

Suppose that I_{in} is a constant current positive in the direction shown in fig. 3.24. All components are considered as ideal.

The incoming current is integrated by the charge amplifier, the output is:

$$V_o(t) = \frac{1}{C} \int_0^t I_{in}(\xi)\, d\xi + V_0 \tag{3.72}$$

When:

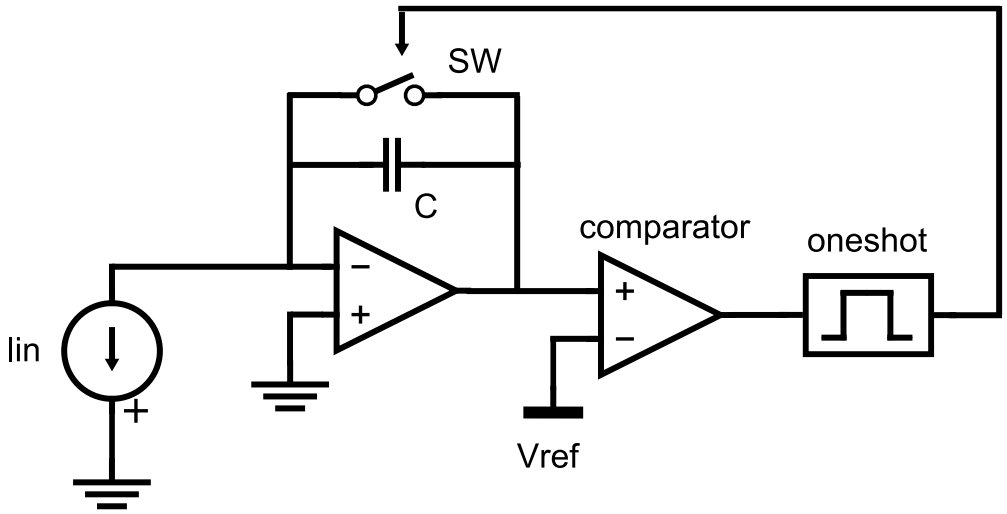


Figure 3.24: CFC with voltage reset.

$$V_o(t) = V_{REF} \tag{3.73}$$

The comparator's output switches enabling the timer – also known as one-shot. The one-shot produces a pulse that closes the switch, discharging the capacitor. The capacitor $C1$ loses a charge equal to CV_{REF} and the cycle restarts.

Ideally, not taking into account the reset time, the output relationship would be given by:

From equation 3.64:

$$\int_0^T \frac{I_{in}(\xi)}{C}\, d\xi - V_{REF} = 0 \tag{3.74}$$

We have:

$$\overline{Iin}|_T = \frac{C \cdot V_{REF}}{T} \tag{3.75}$$

The output frequency is then:

$$f = \frac{\overline{Iin}|_T}{CV_{REF}} \tag{3.76}$$

Taking into account the reset time and the propagation time of timer and comparator, the minimum time period is given by:

$$T_{min} = V_{REF}/SR + t_{p,comp} + t_{p,timer} + t_{reset} \tag{3.77}$$

SR is the operational amplifier slew rate $[V/s]$

V_{REF}/SR is the minimum time required by V_o to reach V_{REF}, starting from 0. $[s]$

$t_{p,comp}$ is the comparator propagation time. $[s]$

$t_{p,timer}$ is the oneshot propagation time. $[s]$

t_{reset} is the time required to reset the capacitor. $[s]$

It should be noted that the circuit is "blind" during the reset time. During that time interval, the integrating capacitor is shorted and the input current flows through the switch. This charge is lost and it doesn't determine any output variation.

This has an effect on the linearity of the circuit. Considering t_{reset} and an output period $T \geq T|_{min}$, then equation (3.74) becomes:

$$\int_0^{T-t_{reset}} \frac{I_{in}(\xi)}{C}\, d\xi - V_{REF} = 0 \tag{3.78}$$

Which leads to:

$$\overline{I_{in}}|_{T-t_{reset}} = \frac{CV_{REF}}{T - t_{reset}} \tag{3.79}$$

In this final equation, the output frequency and the average input current are not proportional. The error is small if $T \gg t_{reset}$.

For example, if $t_{reset} = 100$ns, the error is about 11% at 1MHz, 1% at 100kHz and 0.1% at 10kHz.

The error will be low as long as the output frequency is low enough compared to the theoretical maximum output frequency. For this reason, this circuit can operate only at relatively low frequencies.

It is possible to modify this circuit improving its linearity (sect. 3.8.3).

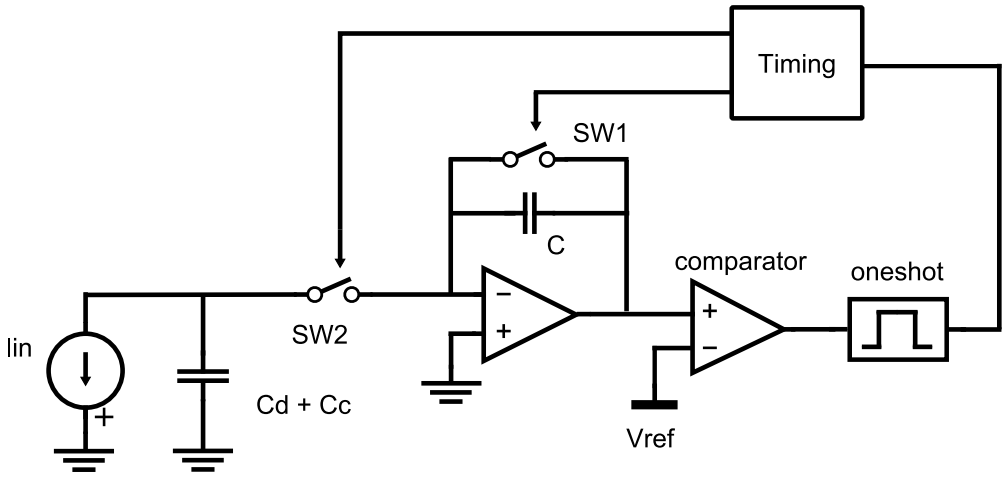


Figure 3.25: Improved CFC with voltage reset.

Current to frequency converter with voltage reset and without blind time

It is possible to modify the current-to-frequency converter in fig. 3.24 to avoid losing charge during the reset time. The proposed CFC is shown in the next figure (3.25). [11]

An additional switch is added at the input of the operational amplifier . When the threshold is reached, the hold switch is opened and the output voltage is sampled by the ADC. The circuit is in hold mode. The signal current charges the input capacitance, which is composed by the chamber plus cable capacitance. In the meanwhile, the reset switch is closed and the output voltage decreases to zero.

After the reset is completed, the integrator output is sampled again and the hold switch is opened. The accumulated charge on the input capacitance is integrated, resulting in a output step with amplitude equal to charge divided by the value of the integration capacitor.

This circuit requires a more sophisticated timing and additionally it's possible to eliminate charge injection error of the switches, but by the use of two samples per integration period, which constitute additional complexity.

3.9 $\Delta\Sigma$ current quantizer

A first order continuous time Delta-Sigma modulator ($\Delta\Sigma$ MOD1), as the one shown in fig. 3.26, may be used to digitize a current.

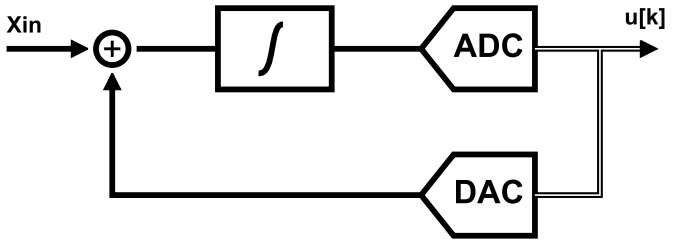


Figure 3.26: Scheme of a MOD1 ΔΣ converter.

The simplest analog-to-digital converter is a 1bit ADC, which is just a comparator. The digital-to-analog converter (DAC) can be implemented easily: the two symbols can be converted into charges with the same absolute value but opposite signs. The result is shown in fig. 3.27. It resembles closely the charge balance CFC.

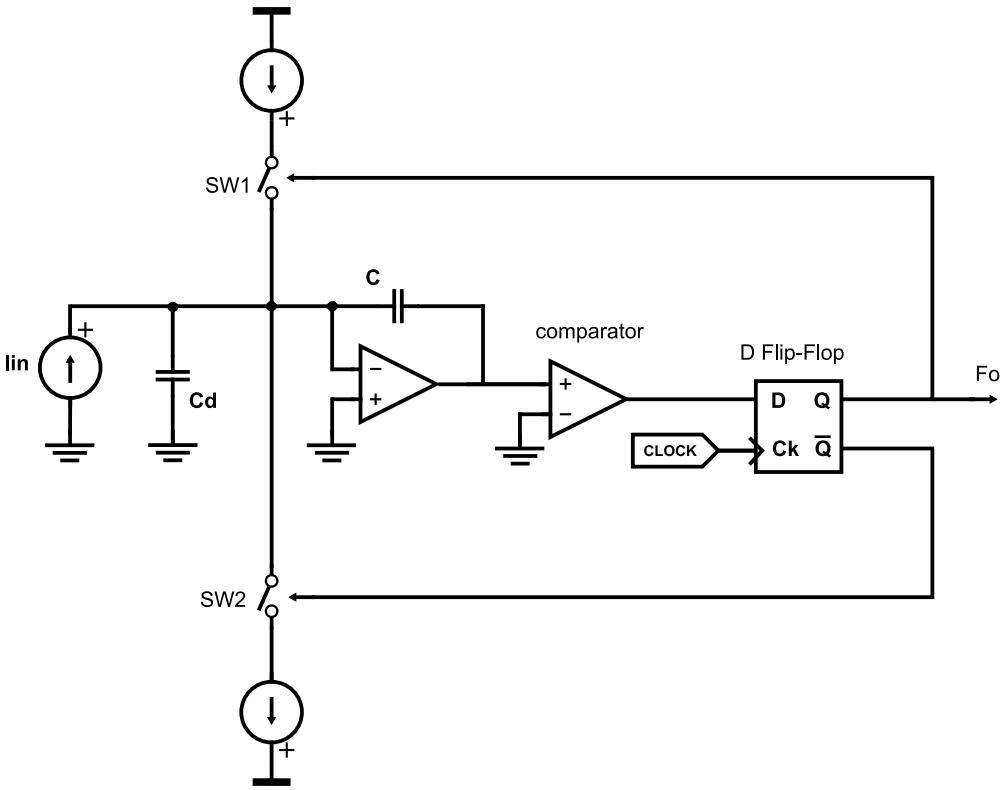


Figure 3.27: Current reset CFC based on a MOD1.

From a quick inspection, assuming all delays to be zero, $f_{ck} = 1/T_{ck}$, $V_o(nT_{ck})$ known:

$$V_o((n+1)T_{ck}) = -\frac{1}{C}\int_{nT_{ck}}^{(n+1)T_{ck}} \Big[I_{in}(t) + I_{ref} \cdot sgn(V_o(nT_{ck}))\Big]\,dt + V_o(nT_{ck}) \tag{3.80}$$

$$V_o((n+1)T_{ck}) = -\frac{1}{C}\int_{nT_{ck}}^{(n+1)T_{ck}} I_{in}(t)dt - \frac{I_{ref}T_{ck}\cdot sgn(V_o(nT_{ck}))}{C} + V_o(nT_{ck}) \tag{3.81}$$

If $I_{in}(t) = I_{in}$:

$$V_o((n+1)T_{ck}) = -\frac{I_{in}T_{ck} + I_{ref}T_{ck}\cdot sgn(V_o(nT_{ck}))}{C} + V_o(nT_{ck}) \tag{3.82}$$

From which the following finite difference equation is derived:

$$\dot{V}_o(n+1) = \frac{V_o(n+1) - V_o(n)}{T_{ck}} = -\frac{I_{in} + I_{ref}\cdot sgn(V_o(n))}{C} \tag{3.83}$$

Applying the scaling in eq. 3.86 to the variables involved, we get the difference equation 3.87 that describes a MOD1.

$$y(n) = \frac{V_o(n)}{T_{ck}} \tag{3.84}$$

$$u(n) = \frac{I_{in}}{C} \tag{3.85}$$

$$v(n) = \frac{I_{ref}\mathrm{sgn}(V_o(n))}{C} \tag{3.86}$$

$$y(n+1) = y(n) + u(n+1) - v(n) \tag{3.87}$$

Where in the common notation has been used: y is the output of the integrator, u is the input and v is the quantizer's output.

Combining equations for $n = 1 \ldots N$:

$$y(N) - y(0) = \sum_{n=0}^{N}[u(n) - v(n-1)] \tag{3.88}$$

If the output is bounded – and hence the loop is stable, it must be:

$$\lim_{N\to\infty} \frac{y(N) - y(0)}{N} = 0 \tag{3.89}$$

Then dividing by N, taking the limit for $N \to \infty$ both sides in eq. 3.88, we get:

$$\lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} u(n) = \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N-1} v(n) \tag{3.90}$$

The average value of the digital output v equals the average value of the analog – but discrete – input u.

The circuit doesn't behave as a current-to-frequency converter, but it is in fact a delta-sigma modulator. The output is a digital sequence, synchronous with the clock and a filter is necessary to reconstruct the conversion value.

The two reference currents, equal to the maximum input current the circuit can allow, provide the intrinsic limitation of the dynamic range the circuit may achieve. Their accuracy is practically limited to 0.1 % of their values, their temperature variation is also proportional to their absolute values as well as the entity of the inevitable random fluctuations. For example, a 100 mA current may be trimmed with an accuracy equal to 10 µA and this will inhibit the correct acquisition of currents lower than that value.

3.10 Current to frequency converter with feedback

It is reported that, to increase the linearity and the thermal stability of the circuit, it is possible to introduce a feedback loop around the current to frequency converter [55, 18].

Referring to fig. 3.28, the VFC is a fast, high output frequency, wide dynamic range voltage-to-frequency converter. In the feedback loop, there is a high-linearity, low-drift frequency to current converter (FCC). A possible implementation of this converted is a charge pump circuit driven by the output of the circuit. The frequency to current converter is responsible for the conversion, ideally all the current at the input would flow into the feedback branch and the output would be the frequency required to produce through the FCC a current that matches the previous.

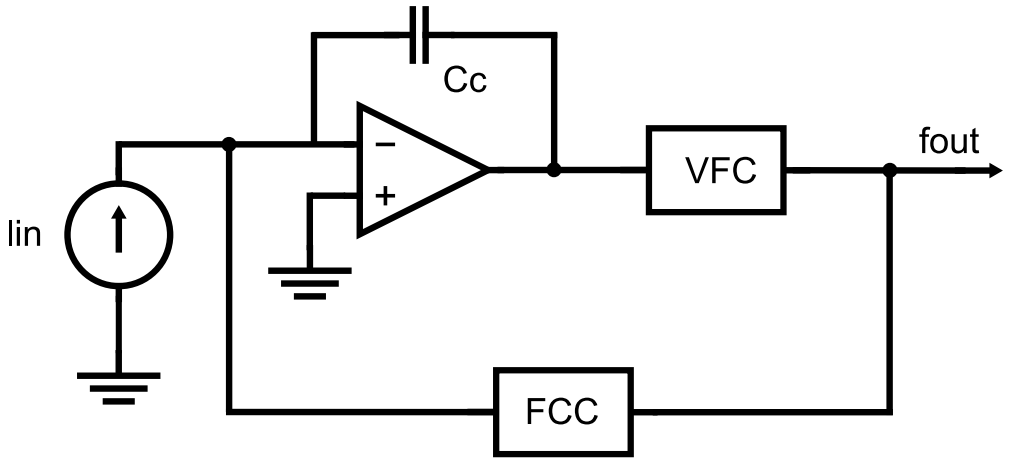


Figure 3.28: Architecture of a CFC with feedback.

The difference between them is the error signal that drives the CFC, for this reason, it was stated that a high output frequency VFC is preferable, as it would provide a fast switching signal for a small error signal. The capacitor C_c is required to compensate the circuit.

In this setup, some of the response speed of the CFC is traded for higher linearity and lower drift, if it is possible to implement a FCC with those superior characteristics.

The discussion of this circuit has been only qualitative. In fact, the circuit is not linear and the linear signal theory cannot be applied to it. A more complex model should be considered, but its analytical expression is troublesome. The value of the capacitor C_c is therefore chosen, in such a design, by trial and error.

Moreover, the additional complexity and reduced stability contitutes a cost that has to be taken into account.

This circuit was not further considered.

	MAX4206	**LOG114**	**ADL5306**
Current range	10 nA - 1 mA (DR 1×10^5)	0.1 nA - 10 mA (DR 1×10^8)	100 nA - 100 µA(DR 1×10^3)
V_α	250 mV	375 mV	200 mV
Log conformity error	2 mV	50 mV up to 3.5 mA	58 mV
dV_α/dt	80 µV °C^{-1}	25 mV °C^{-1}	15 µV °C^{-1}
Voltage noise	$\sqrt{S_V}$ = 800 nV Hz$^{-0.5}$, f = 5 kHz	$\sqrt{S_V}$ = 30 nV Hz$^{-0.5}$, f = 1 kHz	$\sqrt{S_V}$ = 700 nV Hz$^{-0.5}$
Current noise	N.A.	$\sqrt{S_I}$ = 4 fA Hz$^{-0.5}$, f = 1 kHz	N.A.
Voltage Supply	V_{SS} = –5 V, V_{DD} = 5 V	V_{SS} = –5 V, V_{DD} = 5 V	V_{SS} = 0 V, V_{DD} = 5 V
Bandwidth, approx	30 kHz - 1 MHz	5 kHz - 50 MHz	100 kHz - 4 MHz
Notes			

Table 3.2: Comparison of commercial DC LOG amplifiers

Chapter 4

Circuit architectures for single bunch losses measurements

To measure the current induced in a ionization chamber by the losses of a single bunch of particles, a different type of electronic system from the one presented in the previous chapter has to be employed.

The output signal from the detector is constituted by a series of equally spaced current pulses of the same approximative width. The aim of the front-end board is to measure the charge associated with each of the pulses.

An important difference from the previous type of electronics is that in this situation it is possible to couple the circuit in AC. The design is carried out to maximize the signal to noise ratio and withstand the input pulse rate.

4.1 Overview of the system

The structure of a typical detector system for spettroscopy is composed of detector, preamplifier, pulse shaper and an analog to digital converter (fig. 4.1).

The incoming radiation is absorbed by the sensor and converted in an electric signal, usually a short current pulse. Since the height of the pulse may be very small, a preamplifier produces the

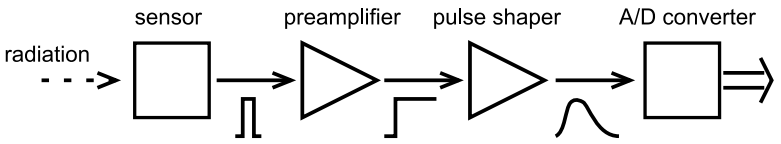


Figure 4.1: Detector system chain

necessary amplification. The type of amplifer is chosen according to the type of measurement that is carried out by the instrument. The current signal is integrated in a charge sensitive amplifier. The output of the preamplifier is fed to a linear network known as pulse shaper.

The primary function of the pulse shaper is to improve the signal-to-noise ratio of the measurement. Considering the frequency response of the pulse shaping network, if the spectral characteristics of the incoming signal and input referred noise of the preamplifier are know, it is possible to create a network that priviledges the signal with respect to the noise. Traditionally, the study of the pulse shaper is done in the time domain, through its pulse or step response.

The peak of the output pulse of shaper arrives after a known delay from the input pulse and it will be acquired by the subsequent digitizing electronics. Additionally, it should be noted that it is characterized by a width that is greater than the width of the pulse that was fed to the preamplifier and it has a long tail. If it is not taken into account, the tail may have an effect known as signal pile-up – the next pulse will be superimposed to the tail, producing an error in the peak measurement.

The peak of the signal at the output of the pulse shaper is acquired directly through a peak-sensitive ADC or the whole signal is acquired and the peak is detected through digital processing. The digitized measurement value is transmitted on a bus, CAMAC, VME64 or PCI, for example, to a computer.

4.2 A universal limit on the signal to noise ratio

To design the front-end electronics, it is necessary to know what are the results that are possibly achievable. The most important result is a limit to the maximum signal-to-noise ratio that will affect the measurement. In this section, its value is derived. [36]

We consider an input signal $x(t)$ characterized by a fixed shape $h(t)$ and a variable amplitude, $x(t) = a_k h(t - t_k)$ where a_k is the amplitude of the k-th pulse and t_k is the instant at which the

pulse arrives at the input. The deterministic signal has superimposed a stationary noise $n(t)$, specified by the power density spectrum $S_n(\omega)$, the question that needs to be answered is what is the transfer function of the amplifier that maximizes the signal to noise ratio.

Limiting the scope to linear signal processing, if the amplifier has a transfer function $G(\omega)$, then the output $y(t)$ corresponding to a single pulse $a_0 h(t)$ at the input is given by:

$$y(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} a_0 H(\omega) G(\omega) e^{j\omega t} d\omega \tag{4.1}$$

The variance of the output noise is:

$$\sigma^2 = \frac{1}{2\pi} \int_{0}^{+\infty} S_n(\omega) \left|G(\omega)\right|^2 d\omega \tag{4.2}$$

If the network is time invariant, the output noise is stationary, therefore, if the output signal has a maximum at an instant t_m, the S/N ratio at the amplifier output is,

$$(S/N)^2 = \left(\frac{y(t_m)}{\sigma}\right)^2 = \frac{1}{\pi} \frac{\left|\int_{-\infty}^{+\infty} a_0 H(\omega) G(\omega) e^{j\omega t} d\omega\right|^2}{\int_{-\infty}^{+\infty} S_n(\omega) \left|G(\omega)\right|^2 d\omega} \tag{4.3}$$

This result may also be generalized to linear time variant networks and no distintion is made here. [8]

Schwartz's inequality gives the following relation for two complex functions $A(z)$ and $B(z)$:

$$\left|\int_b^a A^*(x) B(x) dx\right|^2 \leq \int_b^a \left|A(x)\right|^2 dx \int_b^a \left|B(x)\right|^2 dx \tag{4.4}$$

Substituting:

$$A(\omega) = \frac{a_0 H^*(\omega)}{\sqrt{S_n(\omega)}} e^{-j\omega t_m} \tag{4.5}$$

$$B(\omega) = G(\omega) \sqrt{S_n(\omega)} \tag{4.6}$$

Taking the limit for $a, b \to +\infty$,

$$\left|\int_{-\infty}^{+\infty} a_0 H(\omega) G(\omega) d\omega\right|^2 \leq \int_{-\infty}^{+\infty} \frac{\left|a_0 H(\omega)\right|^2}{S_n(\omega)} d\omega \int_{-\infty}^{+\infty} \left|G(\omega)\right|^2 S_n(\omega) d\omega \tag{4.7}$$

Substituting in eq. 4.3 and simplifying, we get

$$(S/N)^2 \leq \frac{2}{\pi}\int_0^{+\infty} \frac{|a_0 H(\omega)|^2}{S_n(\omega)} d\omega \tag{4.8}$$

Whichever transfer function is chosen, the signal to noise ratio will never be greater than the one indicated in eq. 4.8, the maximum SNR achievable.

The equal sign applies in Schwartz inequality if $A(x)$ and $B(x)$ are differ only of a proportionality constant. In the following, a single proportionality constant c_1 will be used, also taking into account a_0.

$$\frac{H^*(\omega)}{\sqrt{S_n(\omega)}} e^{-j\omega t_m} = c_1 G(\omega)\sqrt{S_n(\omega)} \tag{4.9}$$

From which the optimum transfer function is:

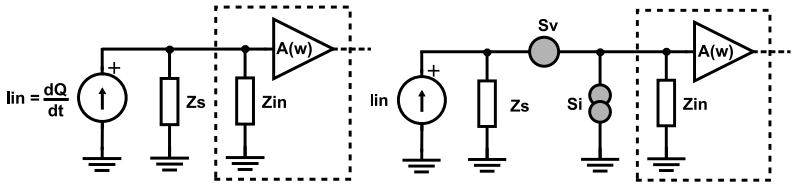
$$G_{opt}(\omega) = \frac{1}{c_1}\frac{H^*(\omega)}{S_n(\omega)} e^{-j\omega t_m} \tag{4.10}$$

The last term is only a delay and can be disregarded. The amplifier output signal is,

$$Y(\omega) = a_0 G_{opt}(\omega) H(\omega) \propto \frac{|H(\omega)|^2}{S_n(\omega)} \quad \text{and} \quad y(t) = \mathcal{F}^{-1}(Y(\omega))(t) \tag{4.11}$$

4.3 Noise and signal at the input of the amplifier

The ionization chamber, wire and input of the amplifier may be modeled as in fig. 4.2. [38]



(a) Only deterministic signals (b) Noise sources

Figure 4.2: Equivalent circuit of the connection between ionization chamber and amplifier.

The total capacitance at the input is given by the sensor, the wires and the input capacitance of the amplifier. It will be here referred to as C. The total shunt resistance is determined by the output resistance of the ionization chamber, the total leaking resistance of the interconnections and the input resistance of the amplifer. The amplifier type is transimpedance, as the input signal is a current and the output a voltage. It is represented here with its input impedance Z_{in} followed by a voltage amplifier of gain equal to $A(\omega)$. It is useful to keep separated its input impedance from the other components. Typically, the real part of Z_{in} will be much lower than the real part of Z_s, which is greater than 10 MΩ.

The noise of the amplifier can be represented with two signal generators at the input, a series voltage generator and a shunt current source. They are characterized by their power spectral densities.

From this model, we derive the parameters of the model in fig. 4.3. The noise signal $n(t)$ will be characterized by its power spectral density, $S_n(\omega)$.

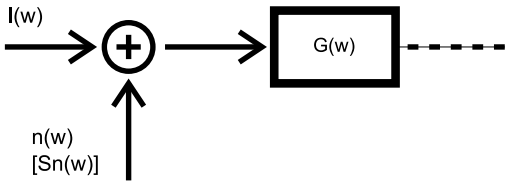


Figure 4.3: General linear model

In a charge measurement, the amplifier in fig. 4.2 is charge sensitive, it is a charge amplifer as seen in sect. 3.3. The relationship between the equivalent noise at the input of the charge amplifier and the equivalent noise at the input of device that provides the gain inside the preamplifier, being it an operational amplifier or a transistor amplifier is,

$$S_v(\omega) \approx S_{v,OA}(\omega) \quad \text{for} \quad A(\omega)C_i \gg C_D \tag{4.12}$$

$$S_i(\omega) = S_{i,OA}(\omega) \tag{4.13}$$

C_D is the total capacitance given by sensor and stray capacitances at the input of the amplifier.

$S_{v,OA}(\omega)$ is the power spectral density of the series noise of the gain device in the charge amplifier.

$S_{i,OA}(\omega)$ is the power spectral density of the parallel noise of the gain device in the charge amplifier.

$A(\omega)$ is the gain of the amplifier.

C_i is the integrating capacitance.

with the above results, the parameters of the general model in fig. 4.2 are:

$$S_n(\omega) = S_i(\omega) + S_v(\omega)\,|\omega C|^2 \tag{4.14}$$

$$G(\omega) = \frac{Z_s(\omega)\,Z_{in}(\omega)}{Z_s(\omega) + Z_{in}(\omega)} A(\omega) \tag{4.15}$$

C is the total capacitance seen at the input node in absence of feedback, or $C = (C_D + C_i)$.

The parameters are:

$$I(\omega) = I_{in}(\omega) \tag{4.16}$$

$$S_n(\omega) = S_i(\omega) + S_v(\omega)\,|\omega C|^2 \tag{4.17}$$

$$G(\omega) = \frac{Z_s(\omega)\,Z_{in}(\omega)}{Z_s(\omega) + Z_{in}(\omega)} A(\omega) \tag{4.18}$$

It is also necessary to characterize the incoming signal. A variable number of high energy particles are lost by every bunch in the accelerator at every turn. A single particle traversing the ionization chamber will create an average number $N = Q/q$ of electron-ion pairs, where Q is the total charge of the ions. The number depends on the energy of the incoming particle and the angle between its trajectory and the axis of the detector. Each positive ion and electron pair is separated by the electric field and the appropriate particle is collected by cathode and anode. The induced current signal ceases to exist as soon as all the particles are collected, therefore the bandwidth of the ionization chamber is determined by the transit time of the carrier with the lowest mobility.

The shape of the pulse generated by a single pair depends on the geometry of the detector and on where the pair is generated. The following approximations are done: the shape is approximated with an average waveform, equal to $h(t)$ scaled so that it has a unity time integral.

The current signal from the chamber can be written as,

$$i(t) = \sum_{n=1}^{N} Q h_n(t - t_n) \tag{4.19}$$

Two ways may be followed from this point: if the arrival time of the particles at the electrodes has a known distribution, $f_n(t)$, so that the average number of particles that arrive at a time between t and $t + dt$ is given by,

$$n_p(t)dt = Nf_n(t)dt \tag{4.20}$$

Then 4.19 can be rewritten as the convolution of $f_n(t)$ and $h(t)$,

$$i(t) = Q \int_{-\infty}^{+\infty} h(t - t')f_n(t')dt' \tag{4.21}$$

Which has a Fourier transform $I(\omega) = QH(\omega)F_n(\omega)$. The tail of $h(t)$ has to be removed to allow an high rate of bunches of lost particles to be detected avoiding signal pile-up (cfr. [38]). Therefore the signal is due only to the electrons, because of their higher drift speed and $h(t)$ will assume an exponential form with a time constant negligible with respect to the time spread distribution. In this situation, it is possible to approximate $h(t) \approx \delta(t)$.

Undere these hypothesis, the optimum achievable signal-to-noise ratio for the average signal and the optimum transfer function are given by,

$$\left(\frac{S}{N}\right)^2 = \frac{Q^2}{\pi} \int_{-\infty}^{+\infty} \frac{|N(\omega)|^2}{S_n(\omega)} d\omega \tag{4.22}$$

$$A_{opt}(\omega) \propto \frac{N^*(\omega)}{S_n(\omega)} \tag{4.23}$$

The second possibility arises from the observation that the global pulse will be different depending on the incident angle, the path length variation and diffusion, while the model developed here aims to be approximate but independent from the configuration, which will vary case by case. Because of this, it is possible to neglect the the time spread of the single pulses, to obtain, from eq. 4.19. the approssimation of $i(t) \approx QNh(t)$. In this case, the optimum achievable signal-to-noise ratio for the average signal is,

$$\left(\frac{S}{N}\right)^2 = \frac{Q^2N^2}{\pi} \int_{-\infty}^{+\infty} \frac{|H(\omega)|}{S_n(\omega)} d\omega \tag{4.24}$$

$$A_{opt}(\omega) \propto \frac{H^*(\omega)}{S_n(\omega)} \tag{4.25}$$

4.4 Practical signal processing

From the previous section, the choice of the shaping waveform is done according to eq. 4.25 or eq. 4.23. The results do not garantee that the shaping network will be realizable.[13, 14]

In fact, if we let $h(t) = \delta(t)$ in eq. 4.25, using the model developed in sect. 4.3, we get,

$$A_{opt}(\omega) \propto \frac{1}{S_n(\omega)} = \frac{1}{S_i^2(\omega) + S_v^2(\omega)\omega^2 C^2} \tag{4.26}$$

$$a(t) = \mathcal{F}^{-1}(A_{opt}(\omega))(t) \propto e^{-|t|/\tau_c} \tag{4.27}$$

Where τ_c is known as the noise corner time constant and its value is $C\sqrt{S_v/S_i}$. This delta response is called infinite cusp and, under the hypothesis of the presence of white noise components only, is the shape of the pulse response of the system that delivers the optimum signal-to-noise ratio. It is shown in fig. 4.4.

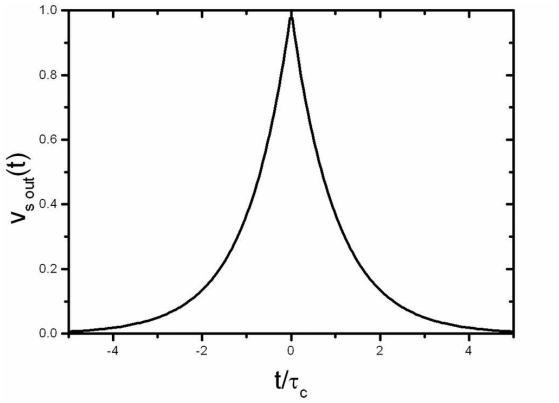


Figure 4.4: Infinite cusp

This shaping function is unrealistic, due to the bilateral infinite width. Nevertheless, the result, discending form the optimum filtering theory, is very useful as term of comparison for any other filtering.

Other of shaping methods that allow finite measurement time per event have been developed, with different complexity, to approach as much as possible the signal to noise ratio of the infinite cusp shaping. The alternative shaping methods take into account, besides the optimum signal to noise ratio, other constraints e.g., flat top and short pulse width.

In pulse height spettroscopy, both time invariant and time variant techniques can be used. Two filters in these categories are the unipolar and bipolar shapers, belonging to the former one and

the gated integrator, a time variant linear filter. A time variant technique generally requires a more sophisticated circuit than a time invariant one, but the former method usually has shorter pulse width, thus decreasing the system dead time and allowing an higer pulse rate.

The choice between the available shapings is therefore often determined by other costraints, set by the measurement system.

The output noise is specified through the equivalent noise charge (ENC), the input signal charge that gives a output signal equal to the rms noise level. It is given by: [36]

$$ENC^2 = \frac{1}{2}S_i \int_{-\infty}^{+\infty} a^2(t)dt + \frac{1}{2}C^2 S_v \int_{-\infty}^{+\infty} \frac{da(t)}{dt}^2 dt \tag{4.28}$$

The previous equation can be extended to include the $1/f$ noise that has been neglected up to now. In this case, solving the integrals it is possible to derive,

$$ENC^2 = S_v \frac{A_1}{\tau} C^2 + 2\pi a_f A_2 C^2 + S_i A_3 \tau \tag{4.29}$$

- τ is the time parameter proportional to the width of the signal processor [36]
- A_1, A_2 and A_3 are dimensionless coefficients that depend only on the shape of the filter response, their values are tabulated in tab. 4.1.
- a_f is a coefficient of the $1/f$ noise referred to the input.

If a given shaping function has been chosen, the coefficients A1, A2 and A3 of the filter are also set. The ENC in eq. 4.29 can be optimized with respect to the characteristic shaping time τ of the filter. We can observe that the three addenda are proportional to the power spectral density of the series, $1/f$ and parallel noises referred to the input of the amplifier and at the same time they are respectively: inversely proportional to the optimization parameter, indipendent from it and directly proportional to the optimization parameter. Therefore, the shaping time τ_{opt} that minimizes the ENC is the one for which the series and parallel noise contribution are equal, given in eq. 4.30.

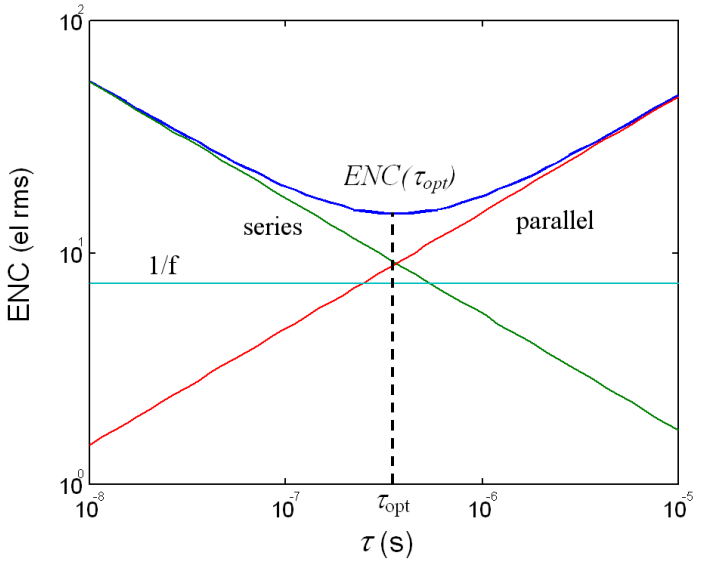
$$\tau_{opt} = C\sqrt{\frac{A_1}{A_3}\frac{S_v}{S_i}} \tag{4.30}$$

Correspondingly, the ENC^2 in this case is given by:

$$ENC^2(\tau_{opt}) = 2C\sqrt{S_v S_i}\sqrt{A_1 A_3} + 2\pi a_f A_2 C^2 \tag{4.31}$$

The ratio between the noise corner time constant τ_c previously defined and the characteristic shaping time of the filter is given by,

$$\frac{\tau_{opt}}{\tau_c} = \sqrt{\frac{A_1}{A_3}} \tag{4.32}$$



As it has been observed before, the noise in the ideal case in which an infinite cusp shaping filter is used is taken as reference to evaluate the results. In this ideal case, where $1/f$ noise is neglected, the ENC^2 is,

$$ENC^2_{w,cusp} = 2C\sqrt{S_v S_i} \tag{4.33}$$

Which compared to the result for a generic shaping (eq. 4.31), neglecting the $1/f$ term for coherence, gives the following ratio, reported in tab. 4.1 for different shaping functions.

$$\frac{ENC^2(\tau_{opt})}{ENC^2_{w,cusp}} = \sqrt{A_1 A_3} \tag{4.34}$$

4.5 Detector output capacitance

Considering eq. 4.29, some observations can be made regarding the capacitance C in the formula: the capacitance value is the sum of all the capacitances at the input node of the charge

Shaping	τ	A_1	A_2	A_3	$\sqrt{A_1 A_3}$	$\sqrt{A_1/A_3}$
Infinite cusp	τ	1.00	0.64	1.00	1.00	1.00
Triangular	$T_{base}/2$	2.00	0.88	0.67	1.16	1.73
Gaussian	σ	0.89	1.00	1.77	1.26	0.71
CR-RC	RC	1.85	1.18	1.85	1.85	1.00
CR-RC6	RC	0.51	1.04	3.58	1.35	0.38
CR-RC6	t_{peak}	3.06	1.04	0.60	1.35	2.26
Semigaussian 7 poles	σ	0.92	1.03	1.83	1.30	0.71
Semigaussian 7 poles	t_{peak}	2.70	1.03	0.62	1.30	2.08
Trapezoidal ($T_f = 0.5T_r$)	T_r	2.00	1.18	1.16	1.52	1.31
Trapezoidal ($T_f = T_r$)	T_r	2.00	1.38	1.67	1.83	1.09
Trapezoidal ($T_f = 2T_r$)	T_r	2.00	1.64	2.67	2.31	0.87

Table 4.1: Shape factors for different shapings. [12, 8, 22]

sensitive amplifier. In order to minimise the equivalent noise charge, the capacitance C should be as low as possible. In practice, the lowest value achivable of this capacitance will be limited by the detector capacitance, which is determined by the type, its structure and the sensitive area.

Moreover, in an integrated circuit or an amplifier with a discrete FET at the input, the input transistors gate capacitance, their transconductance and their equivalent input referred noise spectra (in particular the $1/f$ and the series white noise) are not independent. Adjusting the size of the device it is possible to further tailor the ENC^2. This procedure is referred to as capacitance matching.[36]

In a real scenario, the application requirements set which detector has to be chosen and therefore set the value of the detector capacitance. It can be shown that minimizing the white and 1/f series noise contributions with respect to the gate capacitance of the input FET is equivalent to minimizing the factor $M = \sqrt{C_D/C_G} + \sqrt{C_G/C_D}$, called matching factor. Thus, the gate capacitance of the input FET of the preamplifier should be equal to the detector capacitance.

The input capacitance seen by the preamplifier in the application we are considering depends on the cable length and is in the order of 1-10 nF. It is not possible to match this high capacitance value to the gate-source capacitance of the typical field effect transistor, 1-10 pF. The unmatched input would result in approximatively a ten-fold of the ENC, compared with the matched case.

Using more or very large transistors to compensate, to some extent, the mismatch increases the power consumption. A possible solution is the use of a signal transformer with a ratio $n = \sqrt{C_D/C_{GS}}$, with the added benefit of no additional power consumption.

Chapter 5

Analog and digital circuits, board design

In this chapter, the analog and digital part of the design are presented.

5.1 Analog front-end circuits

After reviewing the possibilities described in chap. 3 and 4, several different analog front-end circuits have been selected, simulated, tested through small wire-wrap boards and successively included in a test board.

One of the key points was the fact that the measurement of different signals is made in several different points and the result have to be compared. Therefore, the acquisition electronics have to be the least dependent as possible on parameters that are not well defined, such as the characteristics of an active device or the temperature.

For this reason, the possibility of implementing a discrete component logarithmic amplifier was ruled out and on the other hand, no commercially available product corresponding to the specifications was found. The same problem applies to the non linear amplifiers described in sect. 3.4, where the gain can vary sensibly with the temperature.

A current input ADC would have provided a very quick and inexpensive solution, but no device with the required characteristics is available on the market today.

The current to frequency converter has the peculiar characteristic of transmitting the input signal through a variable, a frequency, that may variate over a higher dynamic range than a voltage level. This category was therefore studied in detail.

An approach based on the measurement of the charge associated with the particle loss from a single bunch and enhancing the dynamic range minimizing the equivalent noise charge was also considered. This circuit would have required a tecnique to suppress the long signal tail of the incoming signal, to prevent the pile-up of the pulses incoming at 1 MHz, and therefore introduces a variable error in the measurement, since a variable amount of the charge from the ionization chamber is acquired. For this reason, it was not implemented.

5.1.1 Extension of a current to frequency converter to dual input polarity

This circuit is an extension of the CFC presented in sect. 3.8.2. Several modifications with respect with the standard design of this current-to-frequency converter, shown in fig. 3.21, were introduced.

One of the problems of a unipolar CFC is consists of the fact that, if the input current changes polarity, after a time dependent on the initial status, the operational amplifier output will eventually saturate to one of the rail voltages. The device will recover from saturation after a time that depends on the component choice that can be as long as several microseconds. Due to interference picked up by the cables, it is possible that the input signal will unexpectedly be negative.

It is possible to modify the model to allow an input current of any polarity, as conceptually shown in the diagram in fig. 5.1.

Another comparator and another threshold – of opposite polarity compared with the other – are added to the circuit. When the positive threshold $V_{th,p}$ is crossed, a positive charge is added at the input, when the negative threshold $V_{th,n}$ is crossed a negative charge is added to the input.

There are therefore two output signals in this circuit, one corresponding to a positive input current, the other to a negative one. As before, the information about the average current during the active period is carried by the duration of the period itself. The evaluation of the charge integrated in a time window is performed subtracting the measurements.

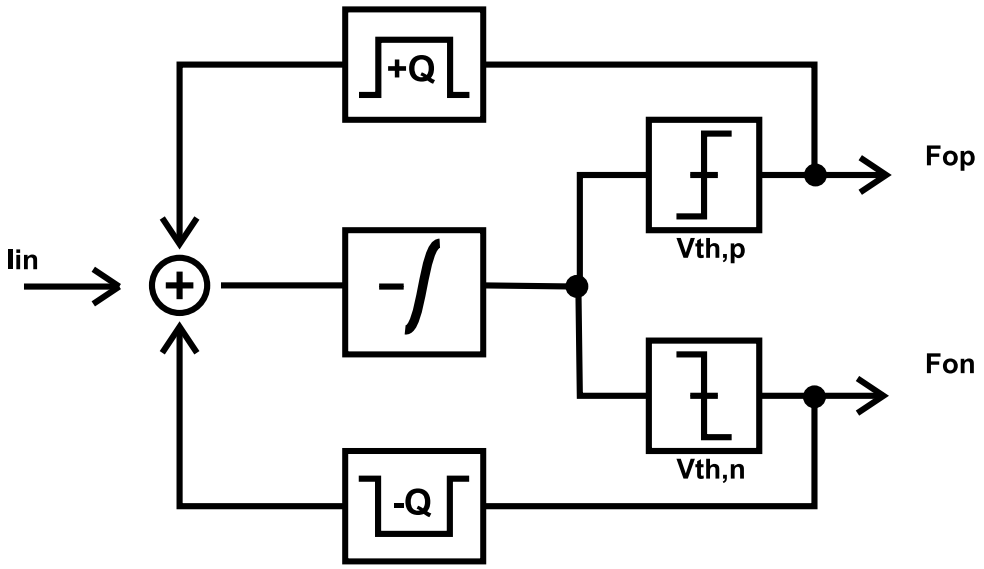


Figure 5.1: Diagram of a modified CFC to allow bipolar current input.

5.1.2 Current to frequency converter with a switched capacitor

Fig. 5.2 shows the simplified schematic of the proposed circuit.

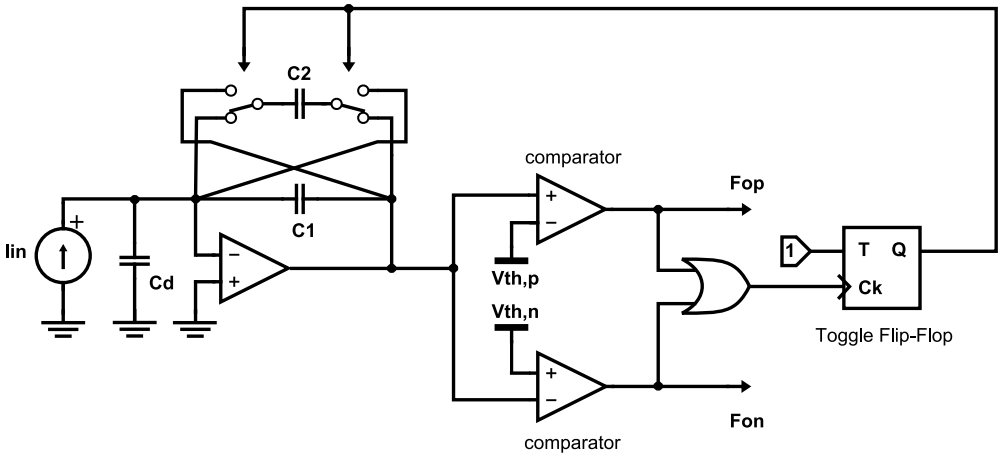


Figure 5.2: CFC implementation through a switched capacitor.

The capacitor is switched through two single-pole double-throw (SPDT) switches controlled by a toggle flip-flop. The memory element status is toggled between 1 and 0 by the output of the comparators. Every time the status of the switches changes, a charge equal to C_2V_o is subtracted or added to C_1. When this happens, V_o is either equal to $V_{th,p}$ or to $V_{th,n}$.

The input output relationship is therefore, $f_{out} = I_{in}/(2C_2V_{th,p,n})$. The circuit is able to detect

currents of both polarities, to distinguish to which polarity corresponds an output pulse, it is necessary to check the output of the comparators.

If the switches have a resistance R_{sw} and the capacitors a series resistance R_{sc}, then the peak current flowing through the capacitor at the switching instant is equal to:

$$I_{pk} = \frac{2 \cdot V_{th,p,n}}{2(R_{sw} + R_{sc})} = \frac{V_{th,p,n}}{R_{sw} + R_{sc}} \tag{5.1}$$

And the current's expression is:

$$i(t) = I_{pk} \cdot e^{-t/\tau} \tag{5.2}$$

The time constant τ is given by:

$$\tau = 2(R_{sw} + R_{sc}) \frac{C_1 C_2}{C_1 + C_2} \tag{5.3}$$

To transfer all the charge it is necessary to wait an infinite time. The transferred charge is given by the integral of eq. 5.2 over the time from two consecutive flip-flop toggles.

In the worst case, this time is the smallest. This happens at $f = f_{MAX}$.

$$\begin{aligned} Q(T_{min}) &= \int_0^{T_{min}} i(t)dt = \int_0^{T_{min}} I_{pk} \cdot e^{-t/\tau} dt \\ &= I_{pk} \cdot (-\tau) \cdot [e^{-t/\tau}]_0^{T_{min}} = I_{pk}\tau \left[1 - e^{-T_{min}/\tau}\right] \end{aligned} \tag{5.4}$$

Correctly, if $T_{min} \to \infty$, then – using eq. 5.1 and 5.3:

$$\lim_{T_{min} \to +\infty} Q(T_{min}) = 2V_{th,p} \frac{C_1 C_2}{C_1 + C_2} \tag{5.5}$$

Hence, the charge on the switched capacitor is:

$$Q_{C2}(\infty) = -C_2 V_{th,p} + 2V_{th,p} \frac{C_1 C_2}{C_1 + C_2} = C_2 V_{th,p} \frac{C_1 - C_2}{C_1 + C_2} \tag{5.6}$$

While C_1 has a charge equal to:

$$Q_{C1}(\infty) = C_1 V_{th,p} - 2V_{th,p}\frac{C_1 C_2}{C_1 + C_2} = C_1 V_{th,p}\frac{C_1 - C_2}{C_1 + C_2} \tag{5.7}$$

The voltage across each capacitor is equal and given by:

$$V_{C1}(\infty) = V_{C2}(\infty) = V_{th,p}\frac{C_1 - C_2}{C_1 + C_2} \tag{5.8}$$

This is a valid approximation only if $T_{min}/\tau \gg 1$. Using the known expressions that link the output frequency and the input current, we can evaluate the minimum amount of charge that is transferred calculating the ratio of the minimum available time that can be available to share the charge and the τ of the exponential decay of the charge,

$$\frac{T_{min}}{\tau} = \frac{1}{f_{MAX}\tau} = \frac{C_1 + C_2}{(R_{sw} + R_{sc})C_1}\frac{2V_{th,p,n}}{I_{MAX}} \tag{5.9}$$

To achieve a small error, it is necessary to work at low frequency or to use switches and capacitors with small series resistance.

The circuit is powered with 5 V, −5 V supplies and uses a maximum current of 120 mA, when the input current is maximum and equal to 100 mA.

The thresholds $V_{th,p}$ and $V_{th,n}$ are set to 3 V and −3 V.

From the relationship between the input current and the output frequency, choosing an output frequency equal to 1 MHz in correspondence of $I_{in} = 100$ mA, the reference charge is equal to 100 nC and the capacitor value is 16.7 nF. The closest standard capacitor value is 15 nF, changing the reference voltages to 3.3 V, - 3.3 V gives the same reference charge.

Two different analog switches were chosen to be included in this design, Analog Devices ADG1436 [3] and DG642 [53], produced by Vishay. Their characteristic parameters are listed in tab. 5.1

At the maximum frequency of operation, equal to 1 MHz, the current flowing through the feedback capacitor is a square wave of half the frequency with current pulses in correspondence of every commutation of the capacitor, due to charge sharing. The two switches selected have

Switch	DG642	ADG1436
Type of switch	SPDT	SPDT
Break-before-make	Yes	Yes
Channel resistance [Ω]	5 typ.	3.3 typ
Channel resistances matching [Ω]	0.5 typ.	0.13
Analog signal range [SIV]	3.4, -5	5,-5 (rail to rail)
Maximum DC current (pulsed) [A]	100 (300, pulsed 1 ms, 10% duty cycle)	240 (600, pulsed 1 ms, 10% duty cycle)
Leakage current [pA]	40 typ.	30 typ.
Bandwidth [MHz]	500	85
Turn on and turn off times [ns]	60, 40 typ.	255, 215 typ.
Supplies in test conditions [V]	15, −3	5, -5

Table 5.1: Parameters of the analog switches employed, from [53, 3]

different characteristics that better suit different aspect of the design. The DG642 has higher bandwidth and lower turn on and turn off times, on the other hand, the ADG1436 has lower channel resistance, that reduces the incomplete discharge error and allows higher currents.

The factor T_{MIN}/τ is equal to 13.3, if the DG642 is used or 20.2 is the ADG1436 is employed instead.

The logic gate is a 74LVC1G00GW produced by NXP and the flip-flop register is a 74AC109, produced by Fairchild Semiconductors. The comparators are MAX912, low power precision TTL comparators. The detailed schematic can be found in the appendix.

As operational amplifier, after a comparison of the available integrated on the market, Texas Instruments THS4631 was chosen. The amplifier has a FET input, determining a very low leakage current, equal to 50 pA at 25 C and to 1.5 nA at 75 C, a gain bandwidth product equal to 210 MHz and a slew rate of 1 kV μs^{-1}. **??**

The output of this amplifier is not rail to rail, but limited to $V_{sat,oa}$ 4.5 V, -4.5 V. If these values are exceeded, the amplifier saturates and it will recover in some hundreds of nano seconds, in the meantime, it will not work correctly. Thus, care has to be taken not to let the amplifier saturate.

From the instant in which the threshold is crossed, the time required to activate the switches has to be lower than the time required for the amplifier to saturate, in absence of feedback action.

The maximum derivative of the output signal is,

$$\left|\frac{dV_o}{dt}\right|_{max} = \frac{I_{max}}{C_1 + C_2} \tag{5.10}$$

Setting $C_1 = C_2 = 15$ nF, its value is 3.3 V μs^{-1}, compatible with the slew rate of the operational amplifier. The maximum delay for the commutation of the switches is,

$$T_{D,max} = (V_{sat,oa} - V_{th,p}) / \left|\frac{dV_o}{dt}\right|_{max} = 450\,\text{ns} \tag{5.11}$$

From sect. 3.2, it is possible to calculate the position of the zero and the pole: the feedback resistance is the leakage resistance of the capacitors, measured approximatively equal to 1 MΩ, with a capacitor equal to 1 nF connected between the input node and ground – required for input

protection as it will be seen – the total 30 nF feedback capacitance determines $\omega_z \approx \omega_p \approx 4.5$ Hz and a bandwidth (sect. 3.3) 4 Hz-210 MHz.

Since the propagation time of the 74LVC1G00GW gate is 1.8 ns [29] and the time necessary for the MAX912 comparator and the 74AC109 J-K flip flop to commutate is 10 ns [10, 24], any of the two switches may be employed and it will still comply with the requirements.

As it will be seen, the fact that the output voltage from the integrator exceeds the threshold will introduce some non-idealities.

5.1.3 Charge balance integrator

Because of its absence of blind time and high dynamic range, the charge balance integrator, discussed in sect. 3.8.2 was dimensioned and included in the prototype.

Considering the input-output characteristic for a charge balance CFC shown in eq. 3.68, it can be evinced that the circuits that implement the charge subtraction and addition constitute one of the most critical parts of the design. Several choices can be made in the implementation, providing different advantages and drawbacks. [15, 23]

A first possibility is the connection of a current source to the input node for a predefined amount of time. While this circuit resembles closely the block diagram of the charge balance integrator, since the current source does not modify the impedance seen at the inverting node of the operational amplifier, it determines a high power dissipation.

It can be shown as follows: we set the maximum output frequency, corresponding to the maximum input current to 1 MHz, as in the previous case (sect. 5.1.2). Again, the reference charge will be equal to 100 nC.

This charge has to be injected by the reference currents in a time ΔT inferior to 1 µs. It is usually required that ΔT is less or equal to $1/(2f_{MAX})$, to avoid distorting excessively the output waveform.

From this,

$$I_{REF} = 2Q_{REF}f_{MAX} = 200\,\text{mA} \tag{5.12}$$

A current source is shown in fig. 5.4, proposed for a previous implementation of a CFC.

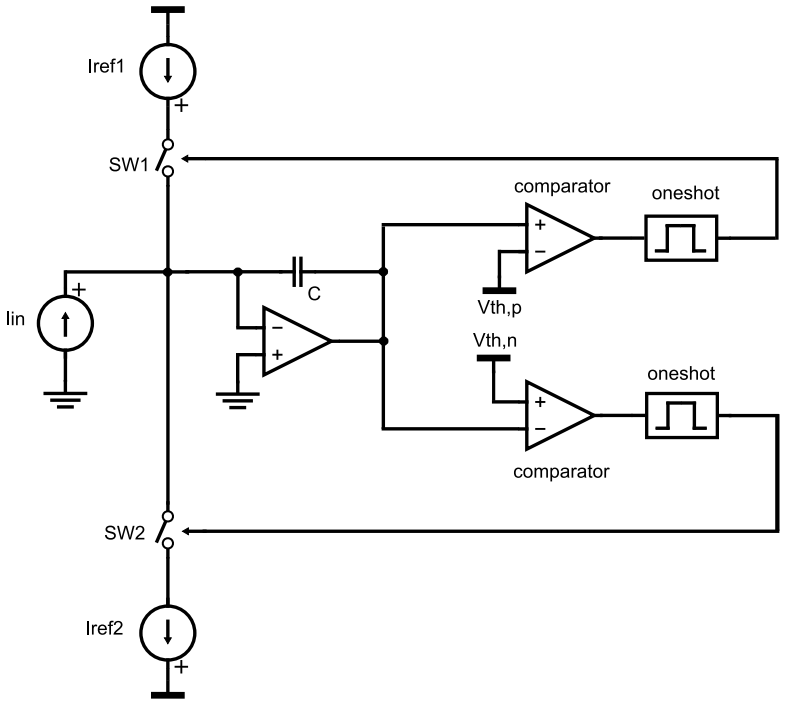


Figure 5.3: Modified current reset CFC.

Referring to the mentioned figure, the degeneration resistor is used to set the output current, independently of the transistor parameters. Neglecting the base current I_B, the base voltage V_B is set by the voltage divider composed by R_8 and R_9.

The output current is given by,

$$I_{REF} = \frac{V_B - V_{BE}}{R_{10}} \quad \text{for} \quad I_{REF}R_{10} \gg \frac{kT}{q} \tag{5.13}$$

The overall voltage drop above R_{10} and Q_1 is 15 V, determining a power dissipation of 3 W, which is too high for an electronic board that will be located in a rack.

The most efficient current source is a simple resistor connected to the lowest analog voltage available and to the input by a transistor used as a switch.

The resistor current source was implemented as shown in fig. 5.5. The MOSFET power transistor N/P pair FDG6332 is switched through a LM5112 MOS driver. The transistors were chosen for their low gate charge and low channel resistance, 300 mΩ and 400 mΩ, for N channel and P channel MOS, respectively.

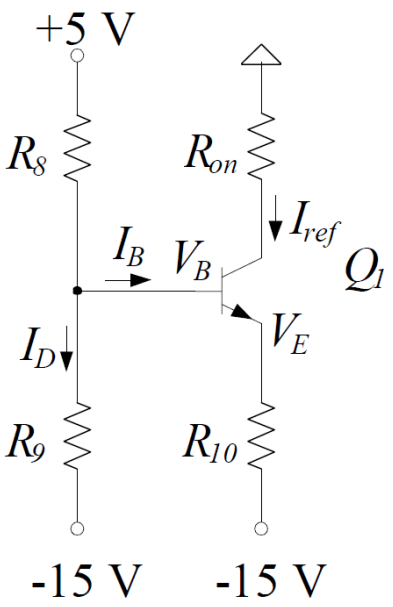


Figure 5.4: Degenerated transistor current source, from [11].

No power transistor able to withstand a 200 mA current with a leakage below 10 nA was found. For this reason, the low leakage MMBD1501 diodes were introduced in the circuit. When the current source is off, the secondary transistor of the FDG6332 pair is turned on and reverse biases the diode which leaks to the output a current smaller than 1 nA.

In fig. 5.5, the output current I_{REF} is set by R_{191} and R_{159} and it is equal to 277 mA. (Note: in a previous version, a diode with a higher leakage was erroneously used instead of MMBD1501, the problem has since been corrected.)

The problem affecting this solution is inherent its nature: the resistor is not a good current source. In fact, the result relies on the assumption that the inverting node of the amplifier is a perfect virtual ground. In reality, this node will not be a zero potential. Moreover, the presence of a shunting resistor connected to the inverting node of the amplifier affects error due to the offset voltage. The offset voltage produces a current that flows into the integrating capacitor that is usually negligible, because of the very high output resistance of the ionization chamber. When the lower resistor is connected, the 260 µV offset voltage determines a current of approximatively 17.3 nA that will contribute 8.3 pC to the reference charge value.

Another solution that is proposed, to avoid the use of a current source and connecting a low value resistor to the input, is injecting a charge in the integrator through charge sharing. The

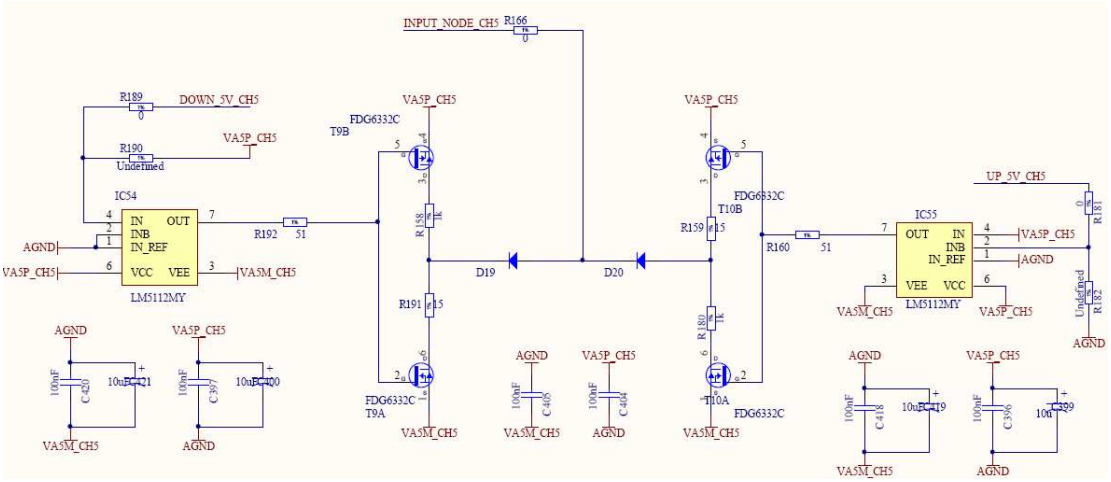


Figure 5.5: Double current source with reduced leakage.

operation can be performed pre-charging an additional capacitor to a reference voltage and connecting it to the summing node.

In this case, $Q_{REF} = C_2 V_{REF}$.

Since Q_{REF} depends on the capacitor value, the input-output relationship will depend as well on it. The value of the capacitance can change significantly with temperature and aging, to limit the error, a capacitor of type NP0 is used. These capacitors are based on titanate formulas and are those with the lowest temperature dependence commercially available, equal to 30 ppm per degree of temperature variation.

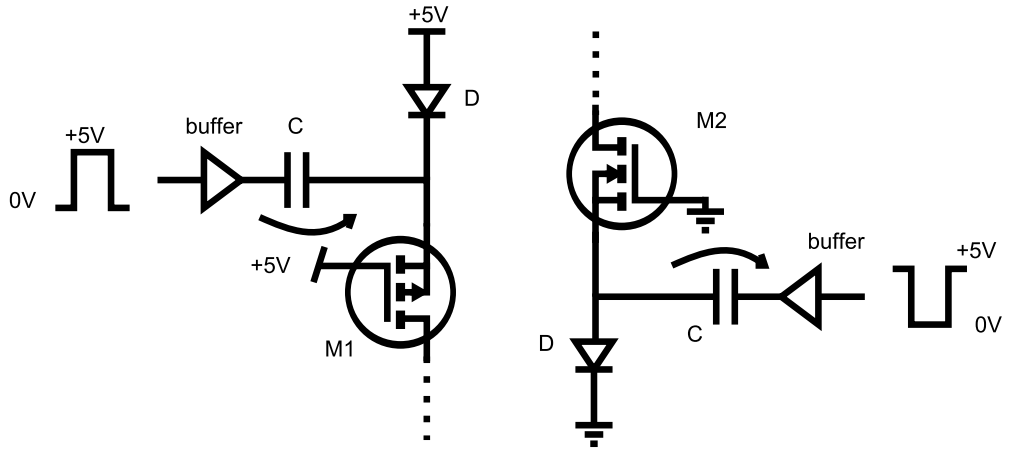


Figure 5.6: Circuit for charge subtraction with a pre-charged capacitor.

The circuit that was designed for this purpose is depicted in fig. 5.6.

Considering first the left-hand part, suppose that at the beginning the signal applied to the buffer is 0 V. The capacitor is charged through the diode to 5 V, neglecting the voltage across the diode. The PMOS has a V_{SG} voltage equal to 0 V and it is therefore not conducting. As soon as the control signal switches to 5 V, the source potential of the PMOS reaches 10 V. Therefore its V_{SG} is equal to 5 V and the MOSFET is turned on. The charge from the capacitor flows through the transistor until the source potential reaches 5 V + V_T, where V_T is the threshold voltage of the MOS.

The circuit in the right-hand side of fig. 5.6 works in a similar way: supposing that at the beginning the signal applied to the buffer is 5 V, the capacitor is charged through the diode to 5 V, neglecting again the voltage across the diode. The NMOS has a V_{GS} equal to 0 V and it is not conducting. As soon as the control signal switches to 0 V, the source potential of the PMOS reaches −5 V. Therefore V_{GS} is equal to 5 V and the transistor is turned on. The charge from the capacitor flows through the transistor until the source potential reaches 0 V − V_T, where V_T is the NMOS threshold voltage.

The same low channel resistance FDG6332 transistors were employed. The MOSFET have a 1.1 V (NMOS) and 1.2 V (PMOS) threshold voltages.

The transferred charge is equal to,

$$Q_{REF} = C(5\,\mathrm{V} - V_{TH}) \tag{5.14}$$

Setting $Q_{REF} = 100\,\mathrm{nC}$, the closest capacitance value available is 8.2 nF.

The diodes employed are MMBD4448, fast switching diodes and as buffers the wide band high output current LME49600, made by National, were selected.

The disadvantage of this technique is the impossibility of calibrating the injected charge Q_{REF}. In fact, in the previous case, it was possible to adjust its value changing the reference time ΔT during which the current source is connected to the input.

It is apparent that, not depending on the choice of the technique employed,

5.1.4 Timing

The charge balance integrator with a current source requires a precise timing signal to define the reference charge, Q_{REF}. This timing information can be provided by a mono-stable, based

on the relaxation time of a resistor-capacitor network. In the RC network, the capacitor used is again of type NP0, to decrease the sensitivity of the input-output relationship to temperature variations. It is also possible to rely on a reference clock to further decrease the sensitivity. In this case, the converter is said to be synchronous, as the switching action can happen only in correspondence of the clock edges. This solution clock (fig. 5.7 shows a bipolar version).

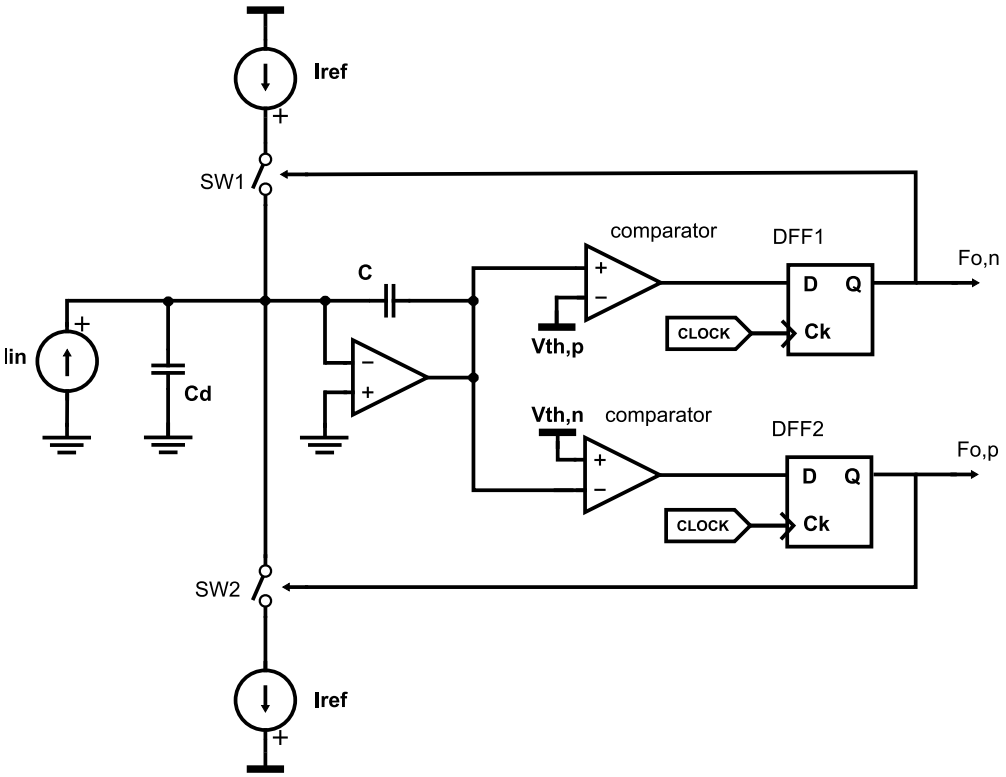


Figure 5.7: Synchronous CFC implementation.

In a synchronous charge-balance CFC, the mono-stable is replaced by a bistable, driven by an external clock. The clock signal is derived from a crystal oscillator or from another high accuracy oscillator (usually 20-40ppm).

The precision current discharges the integrator for a time equal to an integer multiple of the clock period, defined by a counter, the integrated circuit SN74HC161D was selected, for is low cost.

The circuit benefits from the improved linearity and stability due to the clock high accuracy compared to a RC-based one-shot.

The output signal is hence synchronous with the clock reference and can be easily acquired by

a counter or other post processing logic circuits. This also eliminates the errors due to crosstalk problems commonly found in the asynchronous version.

The disadvantages are mainly two: the output pulses are affected by jitter, with a maximum error equal to $1/f_{ck}$, and measurements have shown that the capacitive coupling of the clock into the comparator causes injection-lock effects when the output frequency is at $2/3$ or $1/2$ of f_{MAX}, causing a small dead zone in its response.

5.1.5 Dual integrator stage

To avoid the need of the current sources, a possibility is the use of two switched integrators, as schematically shown in fig. 5.8.

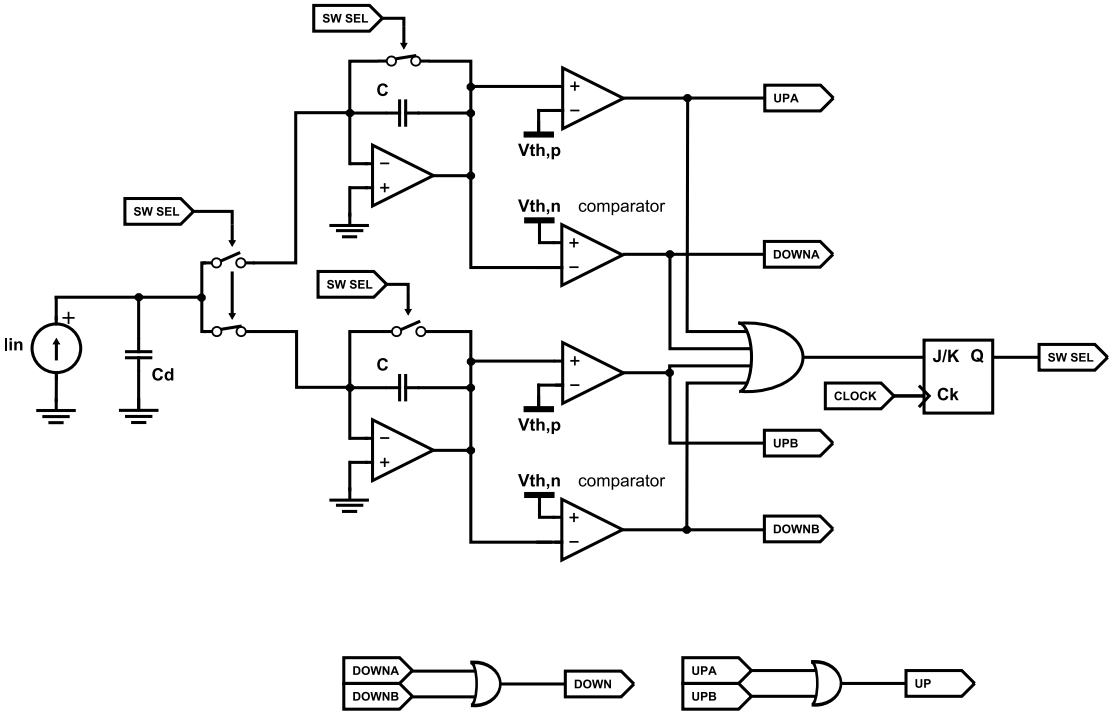


Figure 5.8: Dual integrator stage, simplified schematic

One of the integrators is connected to the input and the incoming signal is integrated. As soon as one of the threshold is reached, the other integrator is connected to the input and the integrating capacitor of the previous one is short-circuited with a switch.

The frequency of the switching between the integrators is given by,

$$f_{out} = \frac{I_{in}}{CV_{TH}} \tag{5.15}$$

And it is therefore dimensioned as the previous circuits. NP0 capacitors are used in the integrators, to reduce the sensitivity with the temperature variation.

This circuit is expected to show an increasing nonlinearity as the output frequency increases, due to charge injection from the input switch and the switching time becomes of the same order of magnitude of the output period.

5.1.6 Common analog parts

Some of the common electronics used in all the circuits is described in the following sections.

Voltage references

Although in the design it was attempted not to rely for the measurement on the value of any voltage, in some cases the thresholds used in the comparators have a direct influence on the conversion.

For this reason, precision low power voltage reference were used.

To set the thresholds $V_{th,p}$ and $V_{th,n}$ the integrated circuit LM285 made by National [1] has been used. Its output is adjustable from 1.24 V to 5.30 V, it has a low power consumption, due to an operating current as low as 10 µA. In some circuits, the value of the threshold determines the input-output relationship of the converter. This voltage reference has a 1% initial tolerance and a low temperature coefficient, from −55 °C to 100 °C the output voltage changes only of a maximum of 20 mV. The dynamic output impedance is equal to 10 Ω.

Referring to $V_{th,m}$ in fig. 5.9, the output voltage is given by,

$$V_{th,p} = V_{1.24}\left(\frac{P_{19} + R_{69}}{R_{67}} + 1\right) - 5\,\mathrm{V} \tag{5.16}$$

A similar result applies for the other reference. Adjusting the potentiometers allows the variation of the reference voltages, in absolute value, from 2.4 V to 3.6 V.

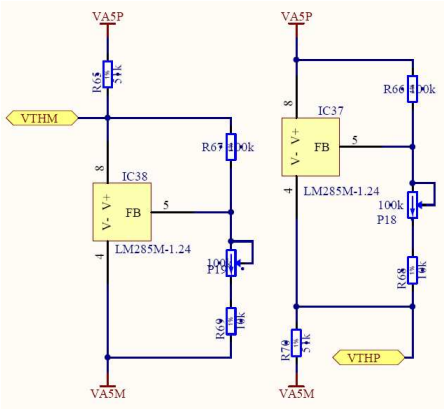


Figure 5.9: Voltage references

Injection of an adjustable current to compensate the leakage

In all the circuits designed, it was foreseen the possibility of compensating the leakage current with an adjustable current, fed by a highly resistive network and regulated through a potentiometer. The accuracy of the matching is practically limited to 0.1 measurementpercentage of the leakage value, and the temperature variation will have different effects on the two currents, ruining their initial agreement. Therefore, the possibility of triggering the measurement of the current, to be used in absence of signal at the input, was foreseen. The value of the measured current is stored in the internal memory of the FPGA and subtracted from all the subsequent measurements. Additionally, the circuit will report a failure in case the leakage current exceeds 1 nA.

Input protection

Although the input of the operational amplifier is already internally protected, I was asked to include additional protection of the input, even if at the cost of reduced circuit performance. To protect the input from transient high input voltages, a low pass filter has been inserted. The filter is composed by a 100 Ω resistor and a 1 nF capacitor, giving a time constant equal to 100 ns and providing protection for spikes of short duration, variable depending on the peak amplitude. To increase further increase the resistance, a pair of BAV199 diodes was connected to the ground voltage and to the input.

5.2 Limitations of the analog channels designed

5.2.1 Voltage range at the input of the ADC

The measurement window over which the current is integrated is variable[1]. It is possible that the window lasts only for a short time and, if the input current is low enough, the comparator will not commutate. In this situation, there is no output count.

To solve this problem, the integrator's output waveform is sampled through an ADC and the sample value is converted to a charge and hence to a fractionary count.

This is done for every acquisition, but is particularly significant when the number of counts – or equivalently the output frequency – is low.

The triangle waveform has some peculiar characteristics which have to be carefully taken into account while designing the circuit and processing the ADC sample data.

First of all, not all sampled values are meaningful. Considering a charge balance CFC, if the measurement window ends during the reset time, the ADC value has to be discarded. To avoid acquiring during this time interval, it is possible to monitor the one-shot's output. When it is in high state, the data is invalid.

Another problem comes from the fact that the output waveform's minima are not exactly zero. This happens because at the beginning of the reset time $V_o = V_{REF}$, then during this time a charge equal to $I_{REF}\Delta T$ is removed from the capacitor and a charge equal to $I_{in}\Delta T$ is added. Overall, the voltage difference at the end of the time interval is:

$$\Delta Vo|_{duringreset} = \frac{I_{REF}\Delta T}{C} + \frac{I_{In}\Delta T}{C} = \frac{(I_{REF} - I_{In})\Delta T}{C} \tag{5.17}$$

Hence, the lower value of the triangle wave depends on the input current.

If a value V^* is acquired by the ADC at time t^* – referred to the beginning of the integrating interval, if we assume that the input current is constant in the previous reset interval and in the time interval $(0, t^*)$, then it is possible to estimate the value of V_{os}.

[1] If the length of the window would have been $n \cdot 20$ ms (where n is an integer) the interference from 50Hz power lines can be filtered or at least greatly reduced. It is also possible to alternate the length of the window to filter – up to some extent – both 50Hz and 60Hz interferences, if required.

$$\begin{cases} V_{os} = V_{TH} - (I_{REF} - I_{in})\dfrac{\Delta T}{C} \\ I_{in} = \dfrac{V^* - V_{os}}{t^*}C \end{cases} \tag{5.18}$$

Solving the system we get:

$$\begin{cases} I_{in} = \dfrac{CV_{REF} - I_{REF}\Delta T - CV^*}{\Delta T + t^*} \\ V_{os} = \dfrac{(CV_{REF} - I_{REF}\Delta T)t^* + CV^*\Delta T}{C(\Delta T + t^*)} \end{cases} \tag{5.19}$$

The peak value is not constant neither. The total delay between the crossing of the threshold level and the switch turn on is $t_{p,comp} + t_{p,timer} + t_{sw,on}$. Since the triangle wave has a rising slope equal to I_{in}/C, the peak value is actually:

$$V_o|_{MAX} = V_{REF} + \frac{I_{in}(t_{p,comp} + t_{p,timer} + t_{sw,on})}{C} \tag{5.20}$$

Which is also dependent on the input current value.

If we suppose: $t_{p,comp} + t_{p,timer} + t_{sw,on} = 100$ns, $I_{in} = 70$mA, $C = 12$nF, then $V_o|_{MAX} - V_{REF} = 0.58$V, which is not negligible.

Combining both of them, we get the following system:

$$\begin{cases} V_{os} = V_{TH} + V_{e,up} - (I_{REF} - I_{in})\dfrac{\Delta T}{C} \\ I_{in} = \dfrac{V^* - V_{os}}{t^*}C \\ V_{e,up} = \dfrac{I_{in}(t_{p,comp} + t_{p,timer} + t_{sw,on})}{C} \end{cases} \tag{5.21}$$

The system can be solved for I_{in}, V_{os} and $V_{e,up}$.

$$\begin{cases} V_{os} = \dfrac{(CV_{REF} - \Delta T I_{REF})t^* + C(\Delta T + t_{d,tot})V^*}{C(\Delta T + t_{d,tot} + t^*)} \\ I_{av} = \dfrac{\Delta T I_{REF} - CV_{REF} + CV^*}{\Delta T + t_{d,tot} + t^*} \\ V_e = \dfrac{\Delta T I_{REF} - CV_{REF} + CV^*}{(\Delta T + t_{d,tot} + t^*)}\dfrac{t_{d,tot}}{C} \end{cases} \tag{5.22}$$

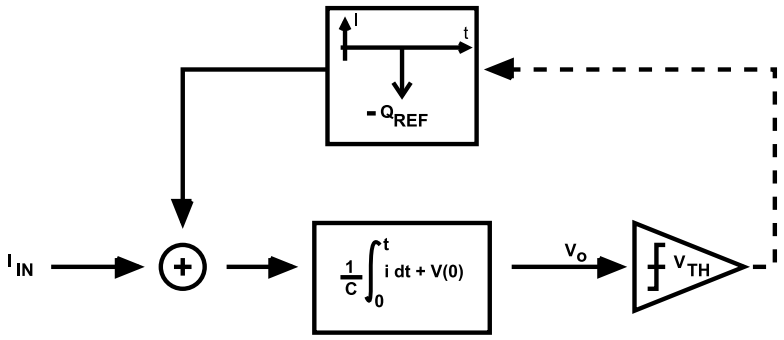


Figure 5.10: Model of the current to frequency converter used in the evaluation of the output noise, or timing jitter, of the output waveform.

The output of the circuit was scaled and converted to differential with a variable gain, before connecting it to the ADC. The gain was left variable to be able to adjust it according to which circuit is used.

5.2.2 Resolution limit of the current to frequency converter

Corresponding to an input current, the output is a sequence of pulses, where the time interval between two consecutive edges of the same sign is the variable of interest. It is inversely proportional to the average value of the current during the said time interval.

In reality, when a constant current is fed to the input, the time interval, and therefore the output frequency of the circuit, is fluctuating statistically around the expected value, due to various noise sources ineliminable from the circuit.

To study the statistics of the fluctuation, the non-linear model shown in fig. 5.10 was used.

In this model, we can take into account the following sources of noise:

- The input noise of the charge amplifier, modeled with a current noise referred to the input.
- The statistical error of the reference charge.
- The statistical delay of the switching of the injection of the current from the instant in which the threshold is crossed.

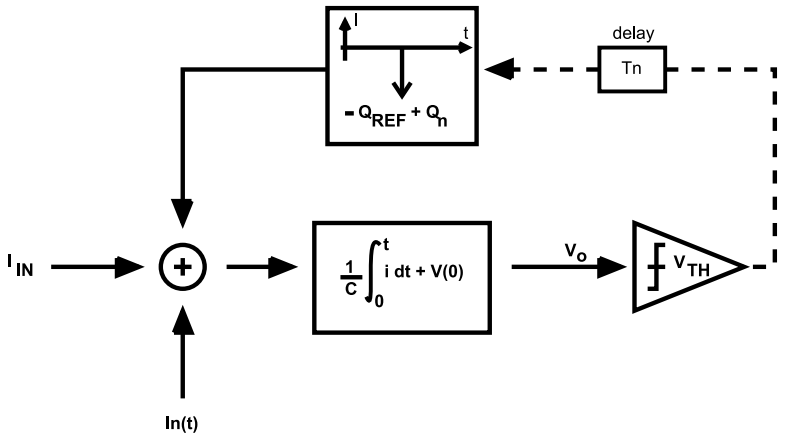


Figure 5.11: Model of fig. 5.10 with noise sources in evidence.

The model is then modified as in fig. 5.11.

If we assume to measure the output period T_{OUT}, then if it is possible to predict the variance $\sigma_T = E[(T_{OUT} - E[T_{OUT}])^2]$, the signal to noise ratio can be written as:

$$SNR = \frac{T_{OUT}}{\sigma_T} \tag{5.23}$$

The absence of informations about the statistical distribution of Q_n and T_n prevents their inclusion in analytical calculations. The input noise current has been considered as a stochastic Gaussian process with zero mean and white power density spectrum.

Preliminary qualitative considerations

The switch event of the comparator determines the positions of the edges of the square wave. Referring to fig. 5.12, the more time the output voltage of the comparator remains close to the threshold before exceeding it, the higher are the chances that the noise will influence the instant at which this happens.

If we consider a voltage noise of standard deviation σ_n superimposed to the output of the integrator, then, from geometrical considerations,

$$\sigma_T \frac{dV}{dt} = \sigma_V \tag{5.24}$$

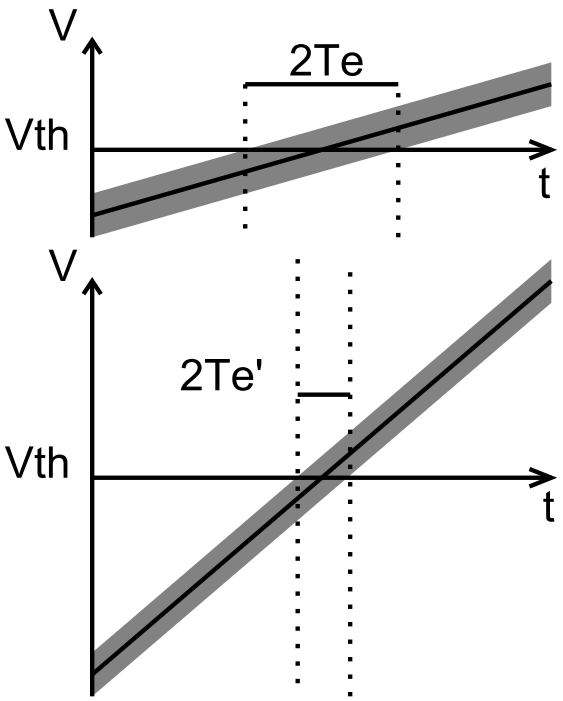


Figure 5.12: Crossing of the threshold with different slopes. The same standard deviation is assumed and it is visually indicated in the figure with a gray region.

Therefore, the uncertainty of the switching event is expected to decrease with I_{IN}. Moreover, the integral of a gaussian noise is a WIener process and it is characterized by a variance that increases linearly with time. Then σ_V in the previous equation will increase quadratically with the time period or equivalently with the reciprocal of the signal current squared. Overall, a proportionality factor equal to I_{in}^{-3} is expected.

The dependence of σ_T with Q_{REF}, at a fixed input signal, follows a similar reasoning. If the reference charge is doubled, then the input current I_{IN} will have to supply twice the charge to determine a commutation and therefore the average time period is doubled. The variance of the charge is proportional to the time period and hence the variance of σ_T is expected to double as well.

Analytical results

Considering only the noise current at the input equal to the power spectral density of the operational amplifier, under the hypothesis that the process has a zero mean and a gaussian distribution, it can be shown that,

$$T_{out} = \frac{Q_{REF}}{I_{IN}} \tag{5.25}$$

While the variance of the output period is,

$$\sigma_T{}^2 = S_I \frac{Q_{REF}}{I_{IN}^3} \tag{5.26}$$

Giving a SNR ratio equal to,

$$S/N = \sqrt{\frac{Q_{REF} I_{IN}}{S_I}} \tag{5.27}$$

The results agree with the expectations.

The following conclusions can be drawn:

- The input noise should be as low as possible.
- The SNR increases if the input signal does.
- If the input signal is fixed, the noise can be reduced increasing the reference charge.

Measurements and limits of the validity of the results

The output period and its variance were measured on the unipolar charge balance CFC described in [9].

The amplifier is a OPA627 which has an input referred current noise with a power spectral density equal to $10 \times 10^{-30}\ \mathrm{A^2\ s^{-1}}$. The average value of the reference charge has been measured equal to 18.8 nC.

The system was supplied with a KEITHLEY 6430 precision current source and the output period was measured with an AGILENT 53131A timer, the data was retrieved over a GBIP bus and processed with a LABVIEW program written ad hoc. In fig. 5.13, for every current, 50 measurements have been taken.

A factor equal to three times the full shot noise associated with the signal current has been added to take into account its noise, as no precise data was supplied by the manufacturer. This

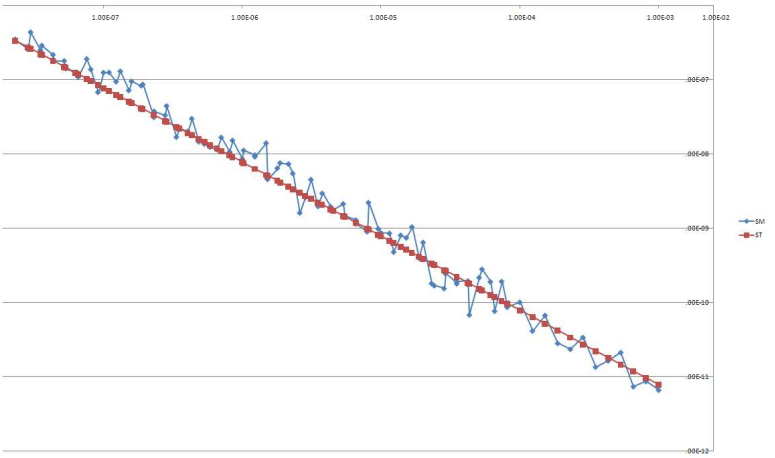


Figure 5.13: Measured (SM) and theoretical (ST) standard deviation of the output waveforms.

term dominates over the whole range with respect to the input referred current noise of the operational amplifier.

The following limits apply to the results:

- As the output frequency increases, the effect of the statistical error of the reference charge will increase as well, reducing the agreement of the expected values and the measurements.
- The integrator was considered an ideal, perfect integrator. Bandwidth limits of the operational amplifier and finite low frequency gain determine an approximate integrator.
- The input-referred voltage noise of the operational amplifier can be converted to a current noise, if the source is known. With a capacitive source, its power density spectrum is not white, but it increases with the second power of the angular frequency.
- Every component connected to the input has to be taken into account. In particular, low value resistors should be avoided. The circuit employed to protect the input has been neglected.
- The model only takes into account a white spectrum. The input-referred power density spectrum of a charge amplifier is actually $S_{I,in,TOT} = S_{I,OA} + S_{v,OA}(C_D + C_f)^2\omega^2$. In the case considered, the two components are equal at approximatively 600 kHz, before this frequency the current noise is greater and the model should still provide results relatively close to reality.

- The model considered doesn't take into account the noise of the threshold, which also has an influence on the switching time.

5.2.3 Maximum output frequency

Instead of using a ADC to increase the resolution, it would have been possible to decrease the reference charge in the current to frequency converter in order to have a commutation if there is a current equal to I_{min} flowing in the input for a time equal to the shortest window. This would have required to change the maximum output frequency, which is set by several limitations. the two most important ones are the bandwidth of the charge amplifier and the charge injection. The output frequency should be kept at least one decade below the high frequency limit of the operational amplifier and the charge injection has to be performed in a time interval equal or smaller than the shortest output period. Therefore the output frequency was set to 1 MHz, depending on the circuit considered, and the ADC was introduced.

5.2.4 Minimum detectable input current

The minimum detectable current is limited by the fact that the bias current is also integrated. Its effect can be compensated adding current of equal magnitude and opposite sign at the input, for example through a potentiometer connected to one of the supplies, but the matching is limited to some percentage.

A special setup is required to track the variations of both currents due to temperature changes and aging. In fact, these two effects will determine a fluctuation of the difference of the two currents with time.

Moreover, the offset voltage is converted to a current through the output impedance of the current source and is also integrated. If the source impedance has a high resistance value, as in the current source case, this problem is secondary.

In practice, the output signal will be affected by an offset due to inevitable mismatch between the input bias current and the compensation current. The minimum output frequency – or equivalently the maximum output period – is limited by noise.

In this work, it is proposed to add the possibility of remotely requesting, over the VME bus, a measurement of the output frequency to be triggered when there is not input signal, the accelerator is not operational. The measured current is the sum of the leakage current coming

from the detector the connectors and the input of the amplifier. The value is afterwards stored and subtracted from the subsequent measurements. Additionally, if the measured leakage is too high, over 1 nA, an error flag is set, as the board or the detector has a problem.

5.3 Digital circuits

The purposes of the digital circuits designed are:

- Provide additional resolution in the integration of the input signal over the window.
- Synchronize the measurement with the machine operation.
- Acquire the measurement in the specified time windows.
- Process the measured values and store them in memory.
- Implement the protocol necessary to communicate over the VME64 bus and provide the data when requested.
- Provide and keep updated the post mortem buffer.
- Report possible problems, such as missing supplies or ADC input out of range.
- Provide a bidirectional voltage level translation to the VME64 bus.

A Cyclone III FPGA was selected for this purpose.

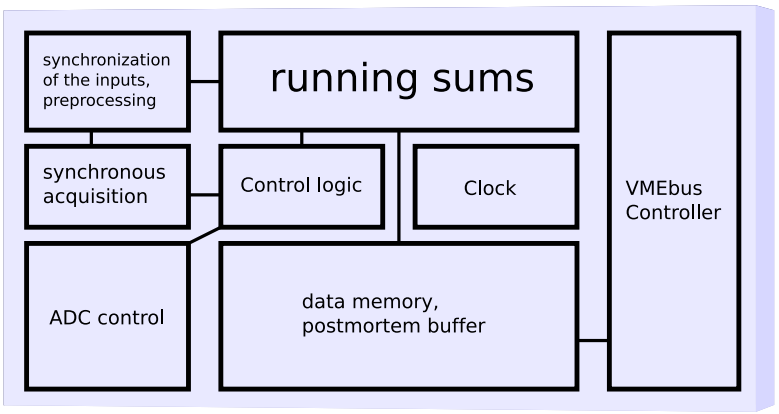


Figure 5.14: Diagram of the processing in the FPGA.

5.3.1 Fractional counts

To provide additional resolution, an ADC was added to the circuit. At every time in which the output of the integrator is sampled, the output of the current to frequency converter is checked as well, to verify if there was a commutation. Each commutation corresponds to a charge equal to Q_{REF} supplied by the detector and the output value of the ADC is mapped to a corresponding charge.

The ADS809, made by Texas Instruments was chosen for this purpose. It is a 12bit, 80 MHz analog to digital converter.

In the FPGA, a value equal to $2^{12} - 1$ is summed or subtracted from the data supplied by the converter if there was respectively a positive or negative commutation of the output in a 14 bit integer. At every clock cycle, the difference between the current data and the last input is supplied to the data processing part.

5.3.2 Data processing: running sum

At every clock cycle, the value of the measurement over the last time window is updated and made available to the VME64 controller.

To avoid an excessive use of the memory, the data is organized recursively in running sums.

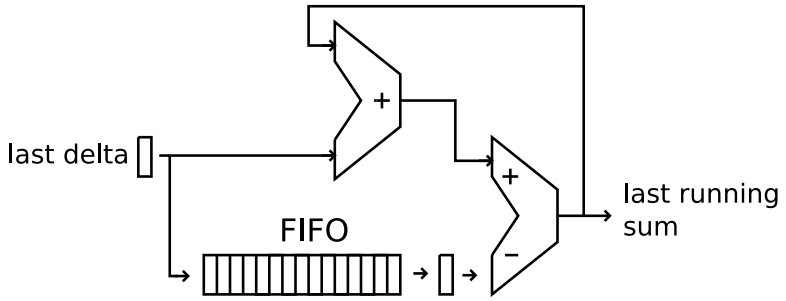


Figure 5.15: Running sum.

Referring to the scheme in fig. 5.15, the incoming data is the digitized value of the charge received from the input in the current clock cycle. This value is summed to the running sum and added on top of a first-in first-out (FIFO) buffer, with N elements. The N-th element of the

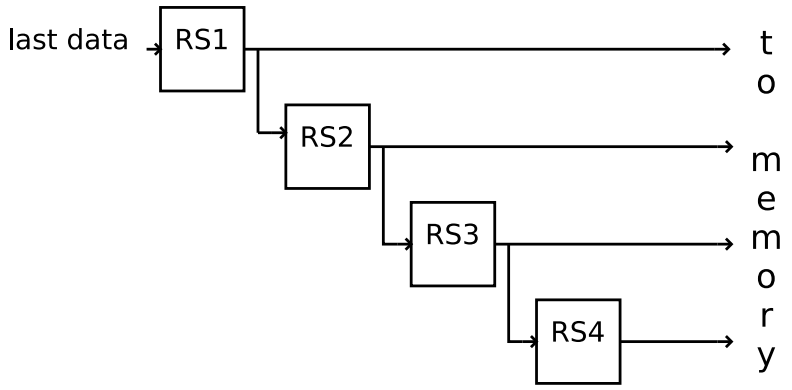


Figure 5.16: Organization of the measurements over the different time windows as running sums of other measurements.

buffer is pushed out. This is the amount of charge that was received $N + 1$ clock cycles ago and it is not part any more of the running sum and it is therefore subtracted. .

As shown in fig. 5.16, the values for the shortest time window are combined in measurements over longer time intervals. The VHDL code written is scalable, allowing an arbitrary choice of the length of clock cycles in each measurement. The most interesting parts are in appendix F.

5.3.3 VMEbus Controller

The VME bus is a is an asynchronous computer bus standard, standardized by the International Electrotechnical Commission (IEC) as ANSI/IEEE 1014-1987 and by the VME International Trade Association (VITA) in different revisions. ANSI/VITA 1-1994 defines VME64, the data bus width is increased to 64 bits and the connectors P1 and P2 have up to 5 rows and the throughput has been raised to 80MBps. [54]

The arbitration bus, the data transfer bus, the priority interrupt bus and the utility bus compose the VMEbus. The arbitration bus controls the requests from the different devices connected to the bus, giving permission to each device to transmit or signaling to the devices that the bus is busy. The arbiter module is responsible for the correct operation of this bus and resides in the first slot of the backplane. The data transfer bus is used for reading and writing operations between modules. The interrupt bus handles interrupt requests, there are seven numbered interrupts defined, IRQ7 being the one with the highest priority. A utility bus is also provided for secondary functionality, such as clocks.

Three main types of cards reside on the bus. A controller, which supervises bus activity, master boards which read or write data to a slave device, and a slave boards which provides the data replying to the read and write requests initiated by a master board.

The two main types of data transfers are the single cycle transfer and the multiple block transfer (MBLT). In a single cycle, the master board performs an address cycle, where the address of the slave board is pushed to the bus, followed by a data transfer cycle. On the other hand, block transfers were introduced to increase the throughput of the bus, reducing the over head of multiple access cycles to the same slave. A block transfer consists again of an address cycle, followed by a variable number of data transfer cycles, up to 256.

A VME64 controller was implemented in VHDL to allow plugging the board in a VME64 rack. The controller implements a subset of the specification: 8, 16 and 32 bit addressing, data transfers of words of the same width and MBLT transfers.

Interrupts are also handled by the interface, but are not planned to be used. The code is in appendix F.

Chapter 6

Conclusions

A study on the possible electronics for the measurement of the losses from a particle beam in accelerators was performed, targeting a realistic scenario.

The possible architectures were reviewed, a subset was chosen, dimensioned and included in a test board. Due to delays in the production of the PCB, it was not possible to test the electronics at the moment this thesis is being written.

Further developments of this work would be a complete testing of the radiation tolerance of the design, that was not required in the specifications but would allow a placement of the rack closer to the detectors and greatly reduce the length of the cables that connect them.

Optical insulation may also be included in the next designs, to protect the back end from accidental connections of the input to the high voltage.

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List of Figures

Appendix A

Key events of the history of CERN

Year	Event
1954	CERN officially comes into being
1957	600MeV Synchrocyclotron commissioned
1959	28GeV Proton Synchrotron (PS) commissioned
1963	Bubble Chambers give first evidence of neutrino interactions
1965	CERN extends into France to build the Intersecting Storage Rings (ISR)
1967	ISOLDE commissioned
	Gargamella Bubble Chamber agreed
1968	Multi-Wire Chambers tested in PS Beam-Line
1971	ISR commissioned
	Super Proton Synchrotron (SPS) project approved
1972	800MeV Booster added to the PS Injector
1973	Neutral Currents discovery ratified
1976	SPS commissioned
1978	LINAC added to PS Injector
	Stochastic Cooling demonstrated
	$p\bar{p}$ proposed for the SPS
	SPS reaches 500GeV
1981	$p\bar{p}$ collisions in SPS at 270GeV
	Large Electron Positron collider (LEP) approved
	Research into a superconducting proton-proton collider (LHC) starts
1983	W and Z Bosons discovered at SPS
	LEP construction begins
1984	Nobel Prize awarded to C. Rubbia and S van der Meer for W and Z bosons
1989	LEP is operational
1990	T. Berners-Lee proposes the World Wide Web (www)
1991	LHC proposed to CERN council
1992	Nobel Prize awarded to G. Charpak for Multi-Wire Chambers
1994	LHC approved by CERN council
1995	anti-matter created from anti-particles
1996	LEP energy increased (LEP-II)
2000	LEP decommissioned to make room for the LHC
2001	Charge-Parity (CP) Violation results verified
2005	LHC tunnel receives first LHC dipole
2006	CERN Neutrinos to Gran Sasso Project (CNGS) begins
2007	SPS to LHC Transfer Lines commissioning begins
2008	First beam in the LHC

Table A.1: Key events of CERN's history by year, adapted from [5].

Appendix B

PS accelerator loss measurements

The measurements have been done with a Tektronics TPS2000 Series Digital oscilloscope. The oscilloscope has a 200MHz bandwidth. The probe has been matched to the coaxial's characteristic impedance, 50Ω.

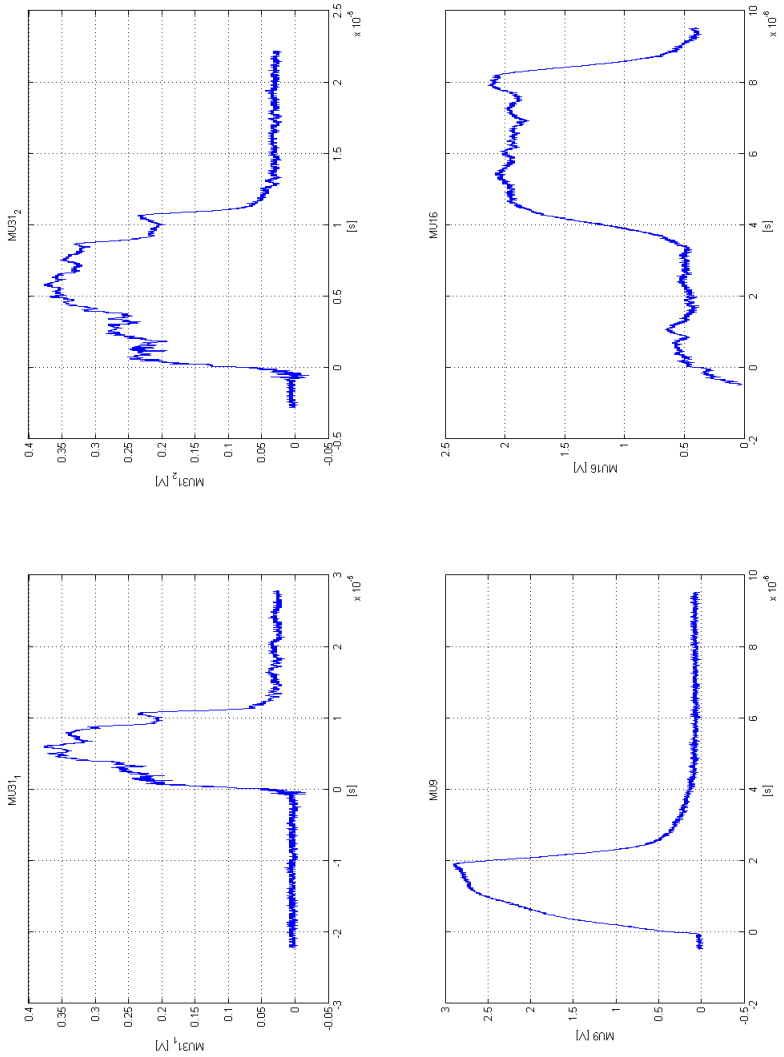

Figure B.1: Ionization chamber measurements 1/3.

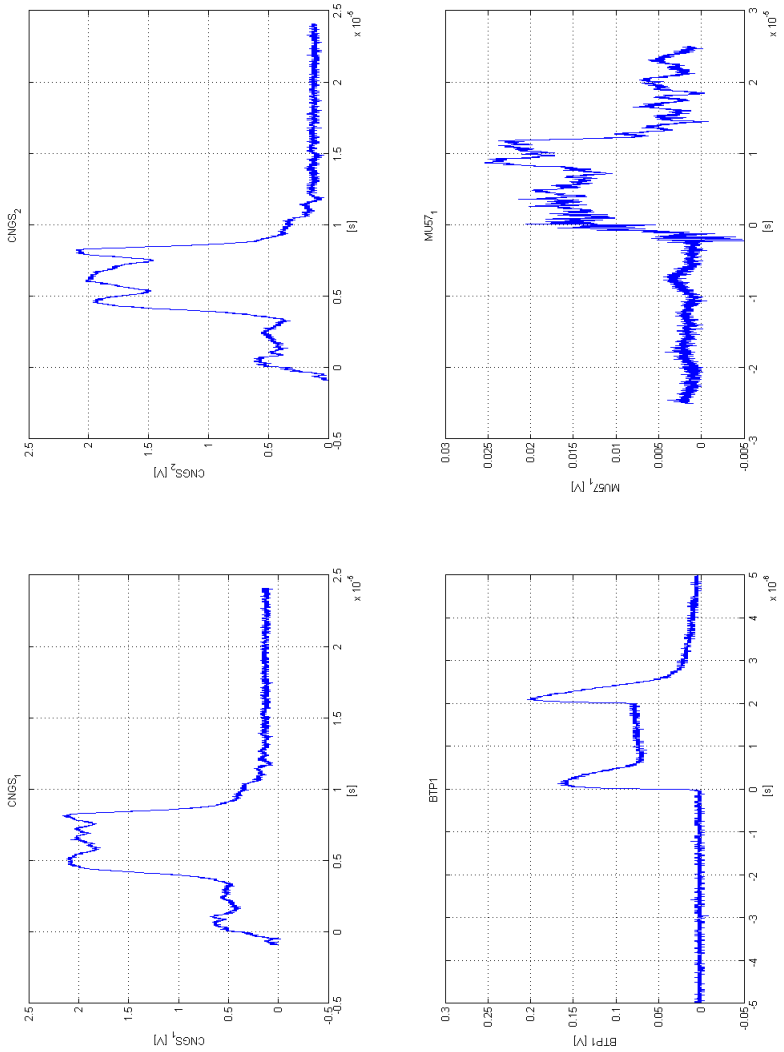

Figure B.2: Ionization chamber measurements 2/3.

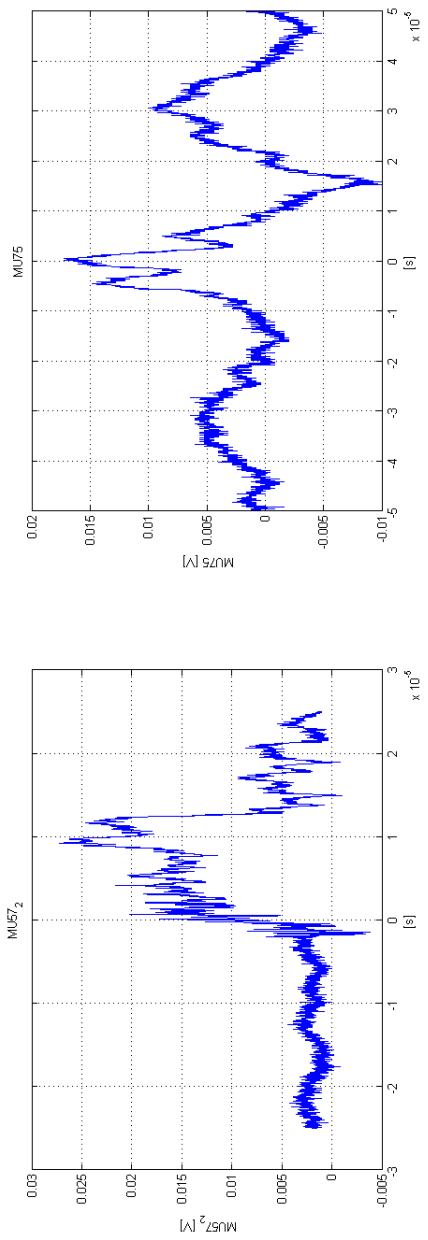

Figure B.3: Ionization chamber measurements 3/3.

Appendix C

LHC ionization chamber: technical drawing

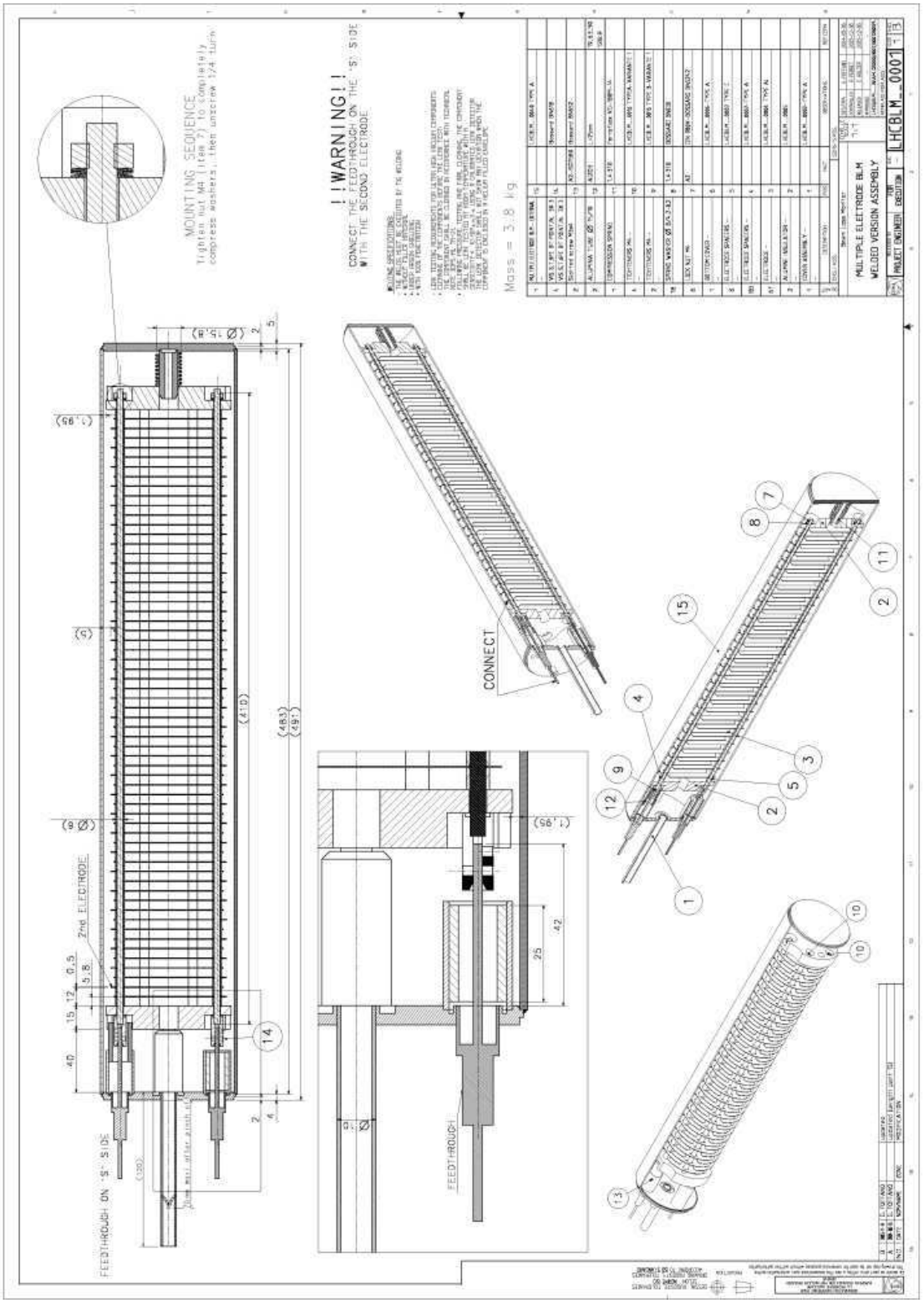

Figure C.1: Technical drawing of the LHC detector

Appendix D

SPS ionization chamber: technical drawing

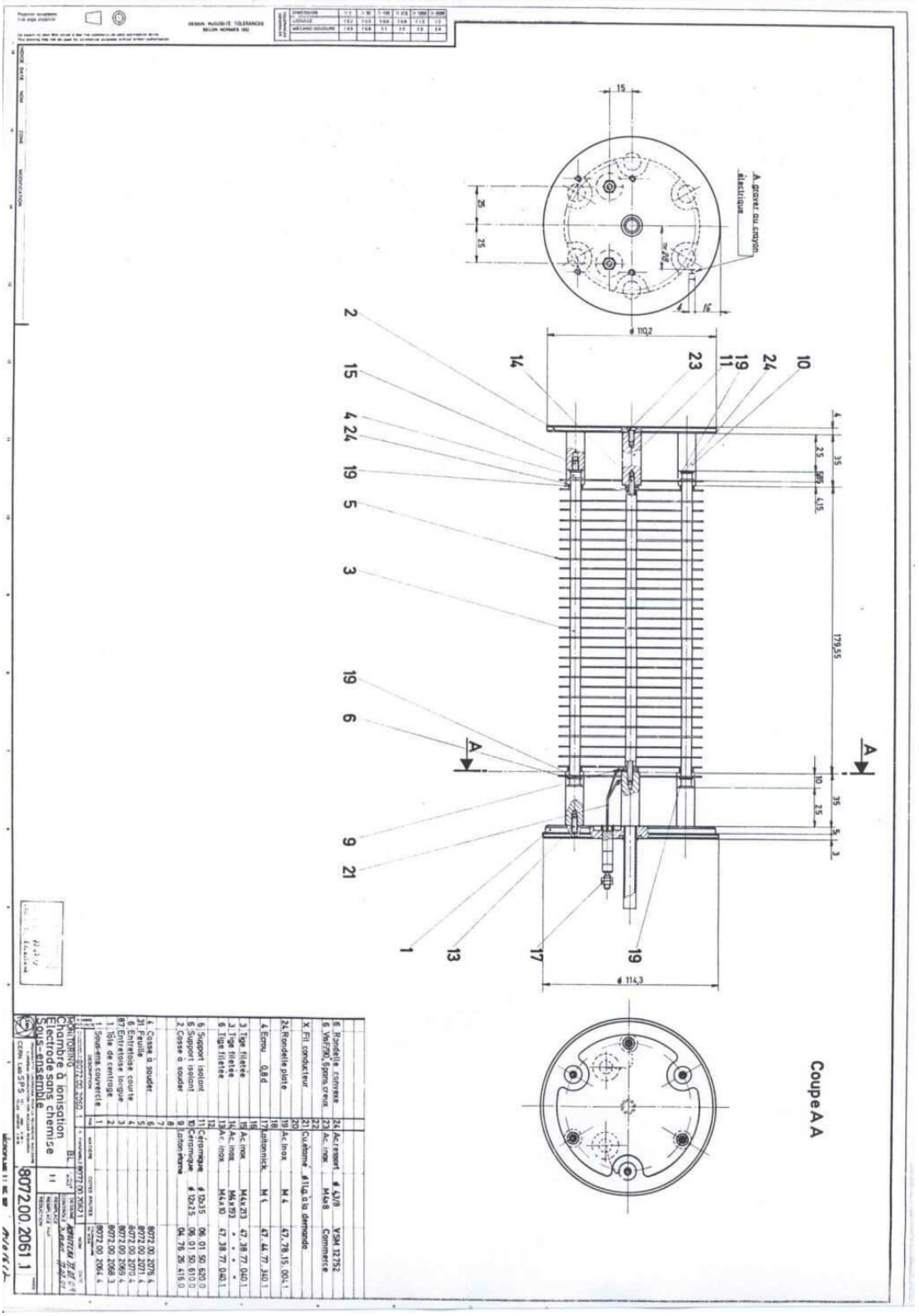

Figure D.1: Technical drawing of the SPS detector

Appendix E

Circuit simulations

The circuit has been simulated with SPICE. Fig. E.1 shows the response to a 70mA input step applied in $t = 0.5\mu$s. Limitations in the SPICE simulator prevent a complete simulation of the circuit's linearity.

The output has the following characteristics:

- Rise time (10% $\rightarrow$ 90%): 12.8μs
- Settling time ($\xi = 2\%$): 49.5μs
- Overshoot: 3.6%

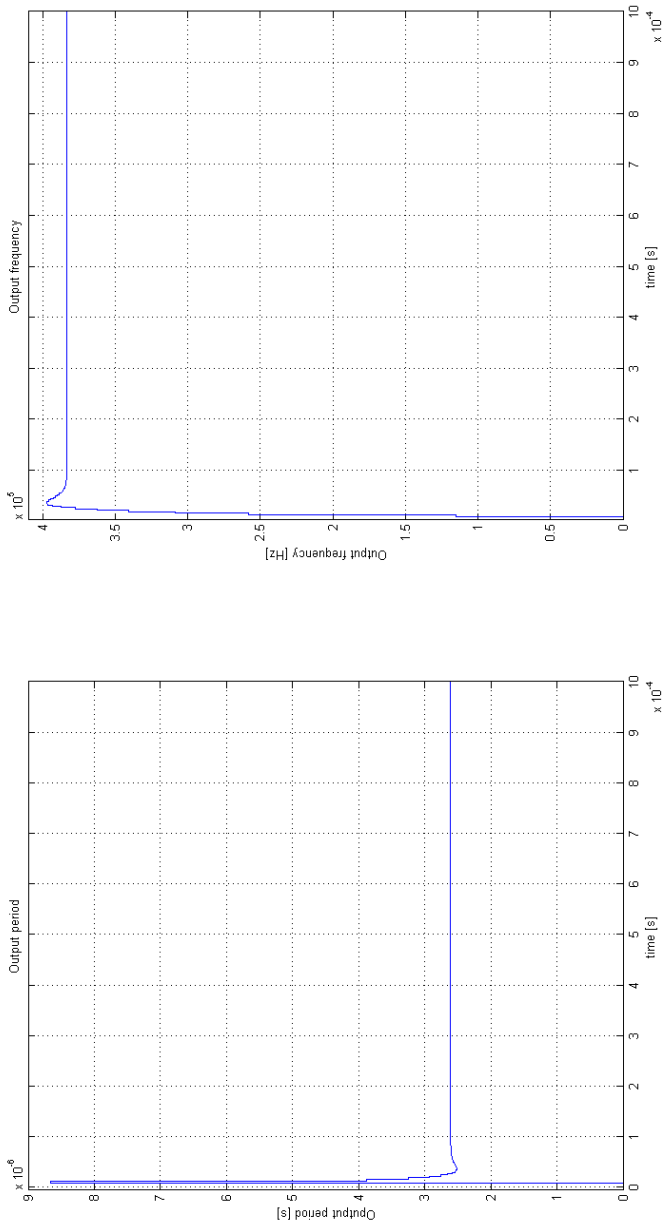

Figure E.1: Response to input step.