The service telemetry and control device for space experiment “GRIS”

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Abstract. Problems of scientific devices control (for example, fine control of measuring paths), collecting auxiliary (service information about working capacity, conditions of experiment carrying out, etc.) and preliminary data processing are actual for any space device. Modern devices for space research it is impossible to imagine without devices that didn't use digital data processing methods and specialized or standard interfaces and computing facilities. For realization of these functions in "GRIS" experiment onboard ISS for purposes minimization of dimensions, power consumption, the concept "system-on-chip" was chosen and realized. In the programmable logical integrated scheme by Microsemi from ProASIC3 family with maximum capacity up to 3M system gates, the computing kernel and all necessary peripherals are created. In this paper we discuss structure, possibilities and resources the service telemetry and control device for "GRIS" space experiment.

1. Introduction

"GRIS" (Gamma and Roentgen Irradiation of the Sun) is a scientific instrument for detection of hard X-rays and gamma-rays of solar flares and gamma-rays bursts onboard the Service Module "Zvezda" in the Russian Segment of the International Space Station. Information about this experiment is presented in [1]. Not only for this experiment, but for all space experiments the problems of scientific devices control, service data acquisition and preliminary data processing are actual.

Typical control problems are: precision control detector parameters by high-voltage regulation, fine thresholds changing (analog regulation), different switching on/off (in real time), statistical analysis of data flows and change of operation modes of the device, etc.

Typical internal data acquisition problems are: temperature measurements in different equipment parts (in power supplies, on scintillation crystals for energy ranges correction etc.), precision thresholds measurements in discrimination circuits, status different switching on/off (in real time), statistical analysis of data flows and searching for event type solar flare or gamma ray bursts with the change of operation modes of the device, etc.

Next, look at the different approaches to the implementation of the device.

2. Selecting components for the creation of unit

There are 3 main ways to realize onboard specialized control and data acquisition unit:

- the use of standard devices and components;
- the creation of specialized units based on programmable logic integrated schemes (PLIS);
- the development and use of application-specific integrated circuit (ASIC).

Obviously, the use of standard components in comparison with PLIS and ASIC, has major flaws – notably the large size, weight and power consumption. Also look problematic features meet the requirements on reliability (due to excess of functions and/or hardware interfaces) and, probably, radiation tolerance (RT).

The PLIS vs. ASIC:

- there is no time and cost in production of ready software implementation of the node (IP);
- quick adaptation of the design to the requirements of the task;
- cheaper in small and medium batches.

There are two main classes of PLIS: complex programmable logic device (CPLD) and field-programmable gate array (FPGA).

Microsemi and Xilinx are world leaders in PLIS fabrication for space applications: in RAM based technology (multiple-programmable) – Xilinx; Flash based technology (multiple-programmable) and Antifuse technology (once-programmable) – Microsemi.

Using of flash-based interconnects present some unique opportunities and advantages to designers of space-flight electronic hardware:

- The flash cells are reprogrammable. This allows the designer to change the design of the FPGA without removing the FPGA from the board, making prototyping easier. It also allows last-minute design change and code update to provide maximum design flexibility.
- The flash cells are nonvolatile. This means that flash-based FPGAs are standalone devices which do not require the provision of external code-storage devices, unlike SRAM-based FPGAs. This minimizes the board space used, and has an associated saving in mass.
- RT ProASIC3 FPGAs are operating almost at the instant of power-up, which is another advantage of the nonvolatility of the flash programming cells. There is no boot sequence required, as in SRAM-based FPGAs which need to download their configuration code from an external storage device.
- The flash cells do not exhibit single-event upsets in the presence of heavy ion radiation. Therefore no triple-chip redundancy to mitigate configuration upsets is required, unlike SRAM FPGAs.

RT ProASIC3 FPGAs are the first to offer designers of space-flight hardware a Radiation-Tolerent (RT), reprogrammable, nonvolatile logic integration vehicle. They are intended for low-power space applications requiring up to 350 MHz operation and up to 3 million system gates.

RT ProASIC3 devices use the same silicon design and process as the commercial UMC 0.13 μm ProASIC3EL family. RT3PE600L uses the same silicon as the A3PE600L, and RT3PE3000L uses the same silicon as the A3PE3000L.

3. Functional scheme and operation

Functional diagram of the developed device is shown in figure 1. This device is called “controller” on this scheme. All the basic functions of the “system-on-chip” implemented in the FPGA A3PE3000L. Information about this FPGA and any soft-realized modules is presented in [2]. The lack of a significant amount of on-chip Flash-memory necessitates the use of an additional EPROM chip with volume 64KB. As a basic processor in this system is used soft realization of most popular Intel 8051 processor with RISC organization (IP Core8051s).

The Core8051s is a high-performance, eight-bit microcontroller IP Core. It is a fully functional eight-bit embedded controller that executes all ASM51 instructions and has the same instruction set as the 80C31. Core8051s provides software and hardware interrupts. The Core8051s architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Since a cycle is aligned with memory fetch when possible, most of the one-byte instructions are performed in a single cycle. Core8051s uses one clock per cycle. This leads to an average performance improvement rate of 8.0 (in terms of MIPS) with respect to the Intel device working with the same clock frequency. Available optional and can be turned off to conserve FPGA resources: multiply and

divide instructions (MUL, DIV and DA) in our project is disabled, (but can be implemented as NOP), and the second data pointer (data pointer 1), in our project is used.

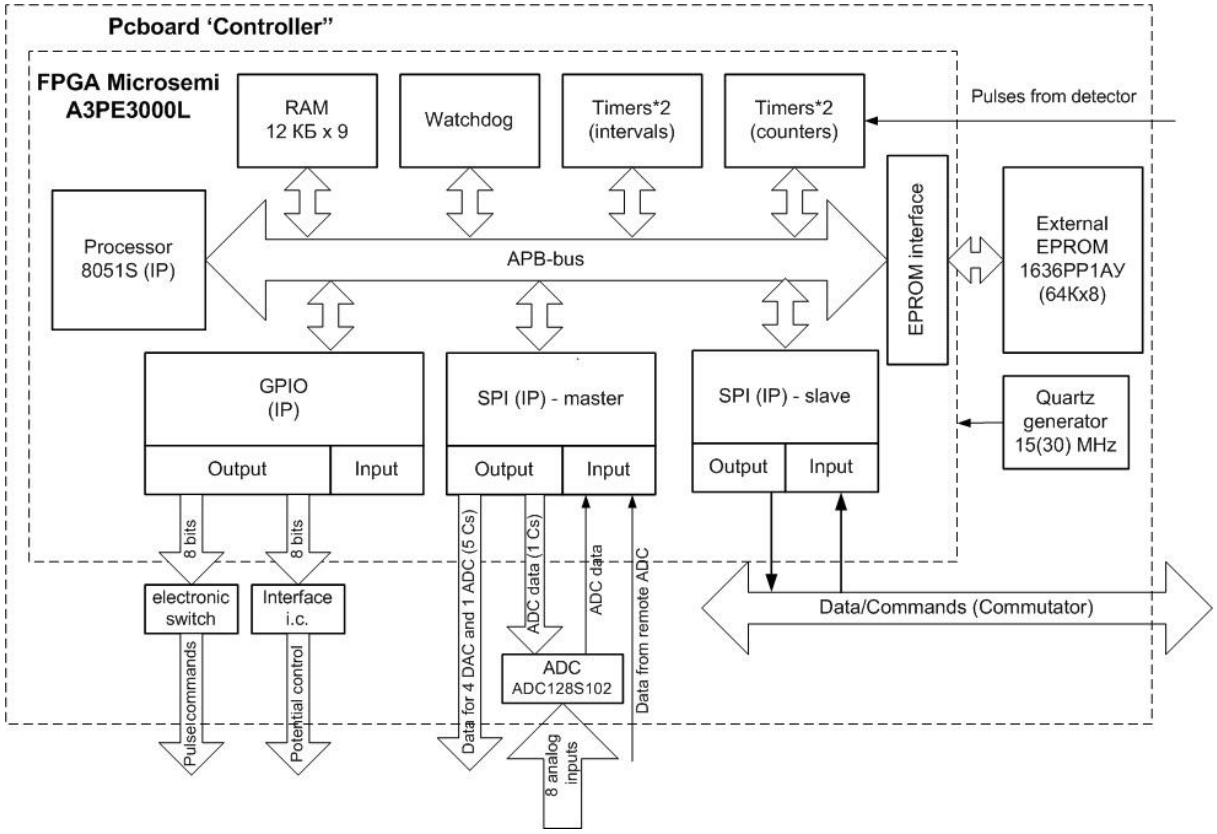

Figure 1. Functional diagram of the developed device.

The advanced peripheral bus (APB) version 3 interface of Core8051s connected to the mirrored master interface of CoreAPB3, with various APB or APB3 slaves connected to the slave interfaces of CoreAPB3 (up to 16 slots). This design implements an 8051-based microcontroller system. In addition to the Core8051s microcontroller core, this system consists of the following peripherals: CoreSPI (two parts), CoreTimer (4 parts), CoreWatchdog, CoreGPIO and Internal RAM (12 KB).

In our design is used 32-bits APB-bus. CoreGPIO is available with the APB slave interface and provide 8 bits-pulse commands and 8-bits potential commands. Also 8 bits can be used as inputs for external status digital signals.

CoreSPI is a serial peripheral interface allowing high-speed synchronous serial data transfers between the 8051 and peripheral devices. This component supports full duplex operation with 8-32 bit serial data transfer and acts as a master or slave. SPI is a point-to-point bus standard used in a variety of embedded applications. One SPI interface is used as slave for data and command interchange with "commutator" device (system for control and data acquisition for all parts of "GRIS"). Other SPI interface is used in master mode to control 4 remote DAC ic's (each 2 channels 12 bit DAC) and 2 8 channels ADC (1 on pcboard of "controller" and one – remote). Thus, this device provides 8 channels DAC and 16 channels ADC.

The CoreTimer module is an APB slave that provides access to an interrupt-generating, programmable decrementing counter. Two counters are used as timers for determination of pulse duration (for pulse commands) and counting interval for statistical analysis of data flows and searching for event type solar flare or gamma ray bursts. Other two timers are used as a counters of photons for event searching.

CoreWatchdog is intended for use with Processor-Based Systems to Protect and Recover from Software Errors. CoreWatchdog is an APB slave that provides a means of recovering from software crashes. When enabled, CoreWatchdog will generate a soft reset for the system if the microprocessor fails to refresh it on a regular basis.

On PCB “controller” are used 8 electronic switches for pulse commands generation and additional interface ic’s for transmitting potential commands to remote units of “GRIS”.

For FPGA power is used +1,5V (for FPGA core) and +3,3V (for FPGA interface part) to ensure compatibility with LVTTL logical levels. Full power dissipation for “controller” PCB is less 100 mW.

4. Conclusion

It was developed service telemetry and control device for internal control, data acquisition and preliminary data processing for “GRIS” experiment onboard ISS based on "system-on-chip" concept.

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References

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