ILC Vertex Detector Issues and Thoughts

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There appears to be a bewildering variety of vertex detector technologies being developed for the ILC. The technologies aim to meet the stringent goals of low mass, precise resolution, and good time resolution. We describe some of the design goals required by the physics, detector constraints imposed by the machine, and how various candidate technologies address these problems.

1 Physics Requirements

The ILC is intended to perform precise measurements of new particles produced with the low cross sections characteristic of high energy e^+e^- collisions. Figure 1 shows cross sections and event yields for a $500^{-1}fb$ data sample for various established and hypothetical processes. Cross sections are low, typical event yields for supersymmetric particles are a few thousand per channel. The angular distributions due to s-channel spin 1 exchange are forward peaked, putting a premium on good coverage of the forward direction.

Although the range of new physics to be studied at the ILC is not yet clear, there are a few flagship measurements which can drive detector design. One example is the set of measurements of Higgs couplings to quarks and bosons. These measurements, which will span more than two orders of magnitude in mass and coupling strength, require excellent separation of b, c, and light quark vertices. A related measurement is the self-coupling of the Higgs. Here the signal reaction, $e^+e^- \rightarrow Z^0H^0H^0 \rightarrow qqbbbb$ with four b-jets must be separated from backgrounds like $tt \rightarrow bbcscs$, ZZZ, and ZZH. This physics requires efficient B tagging and excellent b/c separation in complex events. Different constraints on the vertex detector come from measurements like heavy quark forward-backward asymmetry. Here the emphasis is on forward tracking with flavor tagging and determination of the charge of the parent b quark. Whether the ultimate focus is on Higgs, supersymmetry, or other new physics phenomena, it is likely that precise measurements of heavy quark jets and their decay vertices will play a crucial role [1] in ILC physics.

2 Detector Goals.

The relatively low event yield motivates a design that optimizes the vertex information for each event. This has to be done within the constraints imposed by beam backgrounds, ILC bunch structure and integration with other components of the detector. The successful SLC CCD-based VXD3 vertex detector, with $< 5\mu$ resolution and 0.4% radiation length per layer [2], provides a basis for extrapolating performance of thin, finely pixelated detectors to the ILC.

An set of goals has been formulated taking these opportunities and constraints into account:

- Good angular coverage with many layers close to the interaction point

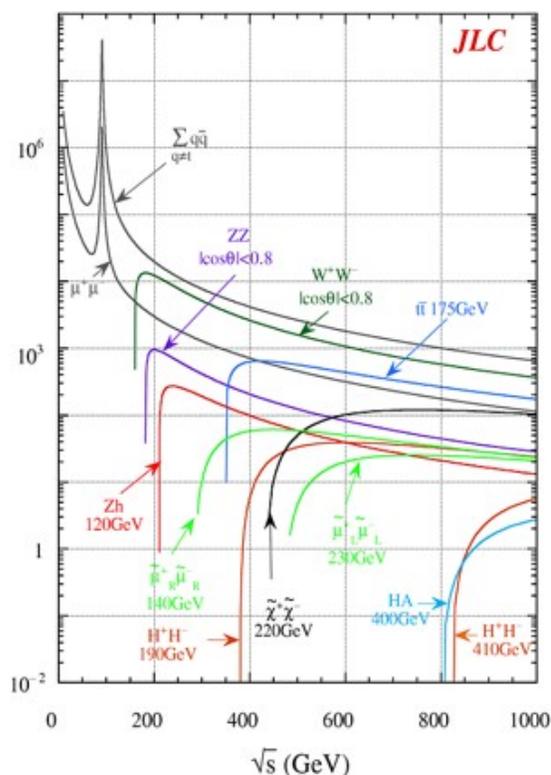- Excellent spacepoint precision ($< 5\mu m$)

Figure 1: Cross sections and event yields for various physics processes as a function of center of mass energy.

- Superb impact parameter resolution ($5\mu m + 10\mu m/(psin^{3/2}\theta)$)

- Low mass ($\approx 0.1\% X_0$ per layer). This translates to a power constraint based on gas cooling of < 20 Watts in the barrel.

- Integration over < 150 bunch crossings ($45\mu sec$)

- Electromagnetic Interference (EMI) immunity

- Moderately radiation hard ($< 1MRad$)

Overall vertex detector performance is a function of inner radius, scattering material, and detector position resolution. Figure 2 shows the results of a parametric simulation of impact parameter resolution as a function of these variables for 1 GeV tracks. For the ILC simultaneous optimization of all three parameters is necessary.

Most goals are individually achievable within current technologies. For example point resolutions below 5 microns have been demonstrated in several detector types (DEPFET, CCD, MAPs). Achieving all of the resolution, mass, time resolution, and power goals is the real challenge. Small pixels needed for good resolution require either high clock speeds to

achieve good time resolution in devices which depend on continuous readout, or a higher density of circuitry with more power for technologies with in-pixel processing.

A set of candidate vertex detector designs exist for the SID, GLC, LDC, and 4th concepts. The inner radii are generally set by the strength of the magnetic field, which defines the radius of the beamstralung cone. Each concept has 5 or 6 layers of pixels in the central barrel. SiD has forward pixel disks as well.
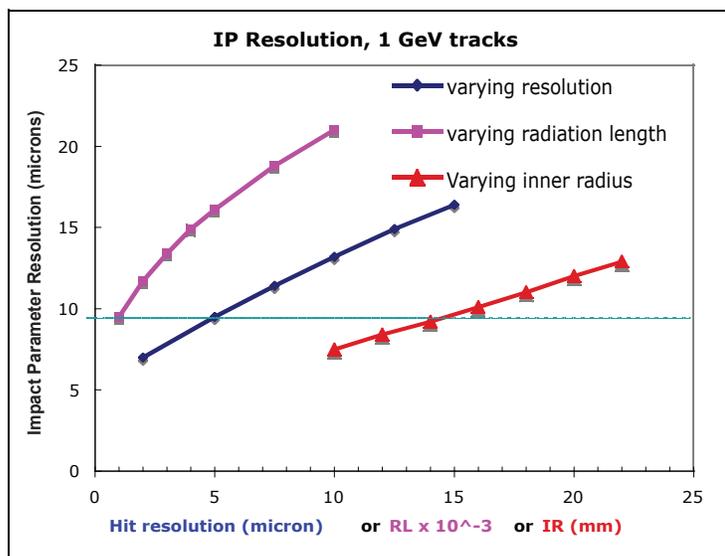

Figure 2: Parametric simulation of impact parameter resolution as a function of inner radius, detector resolution and mass using the SID geometry where the "nominal" detector (horizontal line) has $5\mu m$ resolution, 0.1% radiation length per layer, and a 1.4 cm inner radius.

3 The ILC Environment.

Events at the ILC are accompanied by a huge beamstralung background. Each crossing produces a large flux of electrons and photons caused by pair production and bremstasslung in the intense fields at the interaction point. Charged particles fan out of the IR in a cone whose radius depends on the central magnetic field. The vertex detector will be subject to direct impact of the high angle component, conversions in the beam pipe, and backscatter from the forward calorimeters and beam transport. The primary constraint on the geometrical design of the vertex detector is imposed by the electomagnetic background associated with the beam-beam interaction. The requirement that the inner layer avoid this cone constrains both the inner radius and length [3] of the vertex barrel.

Figure 3 shows the bunch structure anticipated for the ILC, 2820 beam crossings, each separated by 337 ns are followed by a 199 ms inter-train gap. The low event rate and moderate background allow a variety of strategies to be considered to optimize the vertex detector. The long inter-train gap raises the possibility of detector readout during the gap,

rather than during the train. The low duty factor means that the average power can be reduced by cycling power off between bunch trains, thereby reducing the mass needed for cooling.
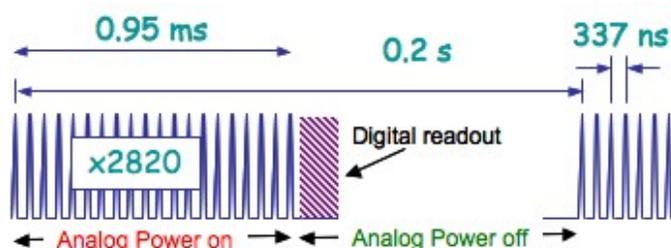

Figure 3: ILC bunch timing including possible readout and power cycling options.

4 Time Resolution

The time resolution required for the vertex detector depends on the machine background rate as well as the pattern recognition ambiguity tolerable in the context of the overall experiment design. Early pattern recognition studies indicated that a $50\mu s$ integration time might be tolerable. Machine operating parameters will play a role. The various machine design reference points, such as "high luminosity" or "1 TeV" each produce different background environments. In addition beamstralung is strongly dependent on the relative alignment of the electron and positron beams. For example, the first few hundred crossings in a train will be used to feedback the electron and positron beam positions to achieve head-on collisions. Additional background is generated by the large dipole field during this tuning process, which implies uneven occupancy during the train and different angular distributions. In the absence of other constraints shorter integration times are clearly better. We need to understand what the tradeoffs are in the various technologies and what level of background is really tolerable.

There have been several approaches to achieving acceptable time resolution. They can be classified into "rolling shutter" approaches, where the detector is read out several times during the bunch train, on-pixel sampling, where charge on a pixel is sampled several times per train and stored locally, and time stamping, where the pixel stores the time of the signal. Several CMOS MAPS devices and the DEPFET prototypes utilize a "rolling shutter" design, with a full frame readout every $\approx 50\mu sec$. For CCDs, the column parallel approach attempts to achieve 50 MHz clock rates with individual amplifiers on each column for faster frame readout. The ISIS CCD and FAPS and CAPS CMOS MAPS devices sample charge in time segments, either in the silicon bulk for ISIS, or on external capacitors for the FAPS and CAPS devices [4] [5]. The Fermilab SOI and 3D devices [6], and the Chronopixel [7] concept, utilize the fact that the per pixel occupancy is small during a train to store a data driven time stamp in the pixel for each hit. This approach has the prospect of allowing crossing-level accuracy for the time stamp.
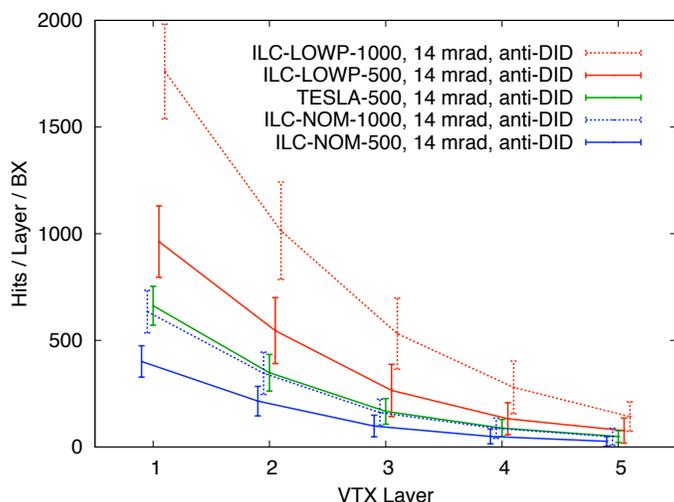
Figure 4: Vertex detector hits per beam crossing as a function of radius for various ILC operating scenarios. [16]

5 Technologies

There has been a revolution in the technologies available for the design and fabrication of sensors for particle physics. The ILC, with it's requirements for thin, precise devices with low power, complex circuitry, is in an excellent position to benefit . Thin CMOS and CCD sensors utilized in the camera and cell phone industries use technologies which can be directly applied to ILC silicon detectors. TCAD software packages which provide 3D physical simulation of silicon-based devices allow us to make detailed models of device geometry, simulate charge collection, and understand details of implantation and doping. Silicon fabs offer a increasing variety of process variations, feature sizes, and substrate options which allow detector integration. Finally, vertically integrated (3D) technologies offer options for unprecedented levels of detector and readout integration.

Each sensor technology has features which will affect any vertex detector system which utilizes them.

- CCDs - This technology was utilized for SLD, an application which bears the closest resemblance to an ILC vertex system. A standard serial readout CCD does not have sufficient time resolution to limit beam-related backgrounds. Alternative readout devices either using a column-parallel approach (CPCCD) or in-pixel storage (ISIS) are being pursued [8].

- CMOS Active Pixels - This technology is based on collection of charge by diffusion in the high resistivity epitaxial layer utilized in several CMOS processes. The technology is commercially available and utilized in cameras and other imagers. The process naturally includes the ability to add in-pixel processing . However the circuits are usually limited to NMOS transistors to avoid parasitic charge collection by the PMOS implants [9].

- SOI - This is a new technology which utilizes the "handle wafer", which is the base of a handle/oxide($\approx 200nm$)/silicon($\approx 20nm$) sandwich where the sensor is formed in the handle and a full CMOS process is utilized for the top silicon. First prototypes are just becoming available from commercial vendors [10].

- 3D - This is also a new technology which utilizes vertical integration of several layers of electronics, each layer ≈ 7 microns thick, vertically integrated with micron-sized vias. This technology allows sophisticated processing within each pixel and the possibility of processing a field of pixels in higher tiers. The first chips utilizing this technology will be available this year [6].

- DEPFET - This technology utilizes a front-end transistor integrated into a fully depleted detector, providing both charge storage and amplification. This device can have very low noise and excellent position resolution. The current designs require readout and processing chips at the ends of columns [11].

Each technology has it's advantages. CMOS active pixels can be fabricated in many available CMOS processes, but depend on the thin epitaxial layer for charge collection and have low signal/noise. CCDs are a well understood technology employed for optical sensors and the SLD vertex detector, but the intrinsic serial nature of the readout requires very fast clocks or innovative readout structures. SOI and 3D promise good integration of detector and electronics but depend on emerging technologies from a limited number of vendors. DEPFETs have very good signal/noise. They require peripheral readout circuitry and allow only limited functionality on the pixel. Tradeoffs between speed and power differ in each technology. In a optimal ILC vertex detector a mix of technologies may provide the best solution; for example utilizing 3D sensors on the inner layers, CCDs on the outer barrel layers and DEPFETs in disks.

6 Mechanical design

The barrel section of the ILC vertex detector is about 12 cm long with a 6 cm outer radius. To meet the goal of 0.1 % radiation length per layer both the sensors and support structures must be as thin as possible. Silicon wafer thinning technology is well developed by industry. However handling these devices and keeping them flat in the face of substantial internal stresses can be challenging. Techniques for handling thinned wafers include:

- Bare wafer thinning

- Rim thinning, where the edge of the wafer remains at full thickness and is available for support,

- Attachment to a support silicon "handle" wafer using epoxy. The support is then thinned and etched to the epoxy layer.

- Attachment to a glass handle wafer using a UV release adhesive. The devices are transferred to dicing tape by shining UV light on the back of the glass wafer.

LBL has demonstrated thinning of individual CMOS sensor chips using a wax grinding process. Fermilab is working on the glass handle process, and has successfully removed 50 micron thick sensor prototypes from the glass handle, diced them, removed the diced sensors
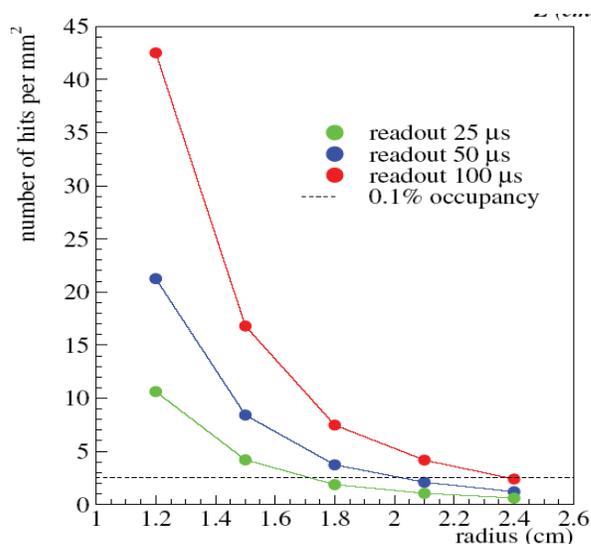
Figure 5: LDC simulation of hit density in the vertex detector as a function of radius for various integration times [12]

from the tape, and transferred the resulting sensors to support structures.The Max Plank Institute has developed a thinning technique based on an SOI etch stop for their DEPFET technology.

Several options for support structures are being developed. A carbon-fiber support, based on a few layers of fiber with holes to reduce mass has been prototyped by a Fermilab/Wasington group. Several groups (LCFI, LBL) are experimenting with silicon carbide and reticulated vitreous carbon foam sandwich supports. The Max Plank Institute has developed a pure silicon "picture frame" support utilizing wafer bonding, thinning and etching technology.

In all of these cases a number of issues depending on sensor technology will need to be addressed before an optimal support design is available. The planarity of the sensors must be understood and whether the support structure is required to also flatten the sensors. Thermal bowing must be understood. This depends on the difference between assembly and operating temperature, which could be large for CCDs operated cryogenically. Another technology-dependent question is whether the ladder is composed of full sized single sensors (CCDs or DEPFETS) or a matrix of sensors whose size is limited to a typical CMOS optical reticle, about 2×2 cm (SOI, 3D, MAPS).

The interconnection problem is likely to be significant. There are a number of outstanding questions that require either more work or a technology decision. Can wirebonds can be made reliably to thinned silicon without fracturing the material? What services are needed by the sensors? How much bypass capacitance is needed and where is it located? How is power coupled to the sensor and routed among sensors? What support stiffness is needed to absorb cable torque? What independent position monitoring is needed? How would optical signals be coupled? How are cables routed and how much do they add to the overall mass.

7 Power

Power is a driving consideration in any vertex technology. Gas cooling is a necessity to minimize mass within the vertex detector. Given the precision necessary for the tracking and low mass of the supports gas flow probably must be limited to the laminar flow region. Given this constraint and the total volume available for gas flow one can estimate the maximum total power dissipation allowable in the vertex region. This been estimated for the SiD barrel as a total of about 20 watts, or $131\mu W/mm^2$, with a maximum temperature rise of $6-8^oC$ [13]. Other concepts obtain similar limits. This is a constraint on average power, and many schemes rely on power cycling, turning on the power only during the $1ms$ crossing period, and off between trains, as a way of meeting the average power constraint.

7.1 Technologies

Technologies are very different in their power requirements. The column parallel CCD must drive 50 MHz of capacitive clock phase lines at cryogenic temperatures. This corresponds to about 10 amps per CCD plane. The overall power can be reduced by minimizing gate electrode capacitance or reducing clock voltages, and both schemes are being explored. ISIS-style devices, which incorporate in-pixel charge storage, can spread the power consumption throughout the $200ms$ cycle, reducing peak currents with respect to the column parallel design. Power for CMOS MAPS, 3D and SOI technologies are dominated by power in the front end transistors.

The required power in these devices is a tradeoff between technology, speed, and noise. The thermal noise in such devices can be expressed as [14]:

$$ENC^2 = (C_{det} + C_{gate})^2 \frac{Kkt}{g_m t_s} \tag{1}$$

Where kt is the usual Boltzmann factor, C_{det} and C_{gate} are the detector load and input transistor gate capacitances, K is a constant which depends on the silicon technology (usually close to 1), g_m is the input transistor transductance, and t_s is the characteristic time of the amplifier. Pixel front end amplifiers usually operate in weak inversion where g_m is independent of device geometry and proportional to $\frac{I_d q_e}{kt}$, where I_d is the input transistor drain current. Noise therefore scales as C_{load} and $\frac{1}{\sqrt{I_d}}$.

With an overall power constraint of $130\mu W/cm^2$, assuming 20 micron pitch pixels, and a duty factor of 100 for power cycling we have a constraint of less than $5.2\mu W/pixel$; or a drain current less than $3.5\mu A$ at $1.5V$. This is to be compared with $29\mu W/pixel$ power and $194mW/cm^2$, power density for CMS pixels, where the pixels are a factor of 37.5 times larger. Both low power front ends and efficient power cycling will be crucial. Fermilab and Brookhaven have shown preamp designs with as little as $500nA$ drain current and

$\approx 100ns$ shaping time. In these designs a load capacitance of 100 femtofarads (ff) gives a 35-50 electron noise level. Lower load capacitances of $\approx$ 10ff should be achievable in SOI-based technologies, and 25-50 ff might be achievable in CMOS MAPS. Signal levels for a MAPs device with a 10 micron epitaxial layer is about 800 electrons, while a fully depleted technology like SOI or DEPFET will collect 4000 electrons in a 50 micron thick device, giving signal to noise ratios 15-100:1.

7.2 Power Distribution

Even if we are able to meet the average power constraint for the vertex detector, we must face the issue of power distribution. A hypothetical column parallel CCD-based system might have $\approx$ 20 modules, each utilizing 20 amps, or 4000 amps of peak clock power. A MAPS or SOI detector which meets the 20 W average barrel power constraint using power cycling will require 1333 amps of peak current if the power is delivered at 1.5 volts with a duty factor of 100. If the required voltage stability is 50 mV a 3 cm diameter copper cable is required on each side. The mass of the supply cables is unacceptable unless something is done.

A promising technology to address cable mass is serial powering. A serial powering scheme delivers power at higher voltage, thus reducing peak currents and IR drops, enabling much lower mass cables. Each module individually regulates it's voltage, passing current on to the next module at lower potential. Peak currents are reduced by a factor equal to the number of modules in series. This scheme has been tested with ATLAS strip and pixel modules and seems to work well, with no increase in overall system noise. A straw-man design for the SiD detector which includes a multiplex factor of between 9 and 15 would reduce the copper area by a factor of 12 (ignoring regulator overhead) for a given voltage drop in the supply line. The addition of the shunt/linear regulators would also relax constraints on the voltage drop allowed on the supply lines providing another large factor in the reduction of copper area.

Fermilab has begun design of a rad-hard serial power control chip. This chip is intended to facilitate serial power R&D for both LHC and ILC applications. It includes a shunt regulator with monitoring and power switching features as well as an AC coupled control interface. LBL has developed a series of DC-DC converter chips which would serve a similar purpose.

These developments are only a start. Any power control system would have to address the rapid turn-on and off of a pulsed power system. A proper system design would probably include smart local regulation which could selectively depower the analog, digital, or both sections of a chip. Switching transients would have to be understood and the current supply properly synched to the detector modules to avoid overcurrent and local heating in the shunt regulator. Forces induced by the supply-return current loop have to be carefully balanced to avoid excessive torques on the low mass detector elements. Finally the mechanical and thermal effects of power switching at 5 Hz will need to be understood and carefully tested.

8 Conclusions

The ILC vertex detector presents a series of challenges to sensor technology, power control and distribution, and mechanical support. At the same time new technologies and tools are becoming available. The electronics industry, in moving toward thinned wafers and
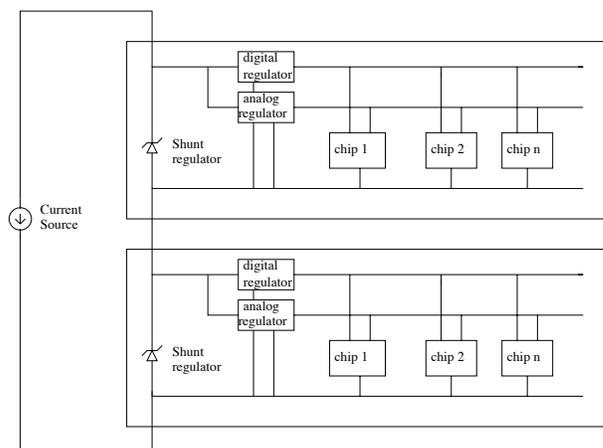
Figure 6: Schematic of a serial powering system.

3D technology is just one example. Achieving the 0.1% layer radiation length goal will require a substantial effort in sensor design, power distribution, support structures, and interconnection. Sensor research is well-established. R&D on system design, including power delivery, cabling, and supports is every bit as difficult and has not yet received the attention it deserves.

References

[1] M. Battaglia, T. Barklow, M. Peskin, Y. Okada, S. Yamashita and P. Zerwas, *In the Proceedings of 2005 International Linear Collider Workshop (LCWS 2005), Stanford, California, 18-22 Mar 2005, pp 1602* [arXiv:hep-ex/0603010].

[2] T. Abe [SLD Collaboration], Nucl. Instrum. Meth. A **447**, 90 (2000) [arXiv:hep-ex/9909048].

[3] C. Rimbault, P. Bambade, K. Monig and D. Schulte, Phys. Rev. ST Accel. Beams **9**, 034402 (2006).

[4] R. Turchetta et al., Nucl. Instr. and Meth. A 560 (2006), p. 139.

[5] G. Varner, Nucl. Instr. and Meth. A 541 (2005) p. 166.

[6] R. Yarema, *In the Proceedings of 12th Workshop on Electronics For LHC and Future Experiments LECC 2006*, http://doc.cern.ch/yellowrep/2007/2007-001/p71.pdf

[7] J. Brau, *Linear Collider Workshop 2007*: http://www-zeuthen.desy.de/ILC/lcws07/pdf/Tracking_VTX/brau_james2.pdf

[8] K. Stefanov, *Linear Collider Workshop 2007*: http://www-zeuthen.desy.de/ILC/lcws07/pdf/Tracking_VTX/stefanov_konstantin.pdf

[9] G. Deptuch et al., Nucl. Instrum. Meth. A **535**, 366 (2004).

[10] Y. Arai et al., *In the Proceedings of International Symposium on Detector Development for Particle, Astroparticle and Synchrotron Radiation Experiments (SNIC 2006), Menlo Park, California, 3-6 Apr 2006, pp 0016*.

[11] J. Kemmer and G. Lutz, Nucl. Instr. and Meth. A 288 (1990), p. 92.

[12] LDC Detector Outline Document: http://www.ilcldc.org/documents/dod/

[13] W. E. Cooper, *ILC VTX Workshop at Ringberg Castle May 28, 2006 - May 31, 2006*: http://www.hll.mpg.de/~lca/ringberg/Talks/1-Monday/3-1-cooper.ppt

[14] P. OConnor, G. De Geronimo, Nucl. Instrum. Meth. A **480**, 713 (2006).

[15] R. Horisburger, `http://dpnc.unige.ch/atlas/mariane/SeminairesUni/R_Horisberger_Talk_21Apr04.pdf`

[16] Adrian Vogel, *Linear Collider Workshop 2007*:
      `http://ilcagenda.linearcollider.org/conferenceOtherViews.py?view=standard&confId=1296`

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