SCT LV-3

VME SCT LV Power Supply

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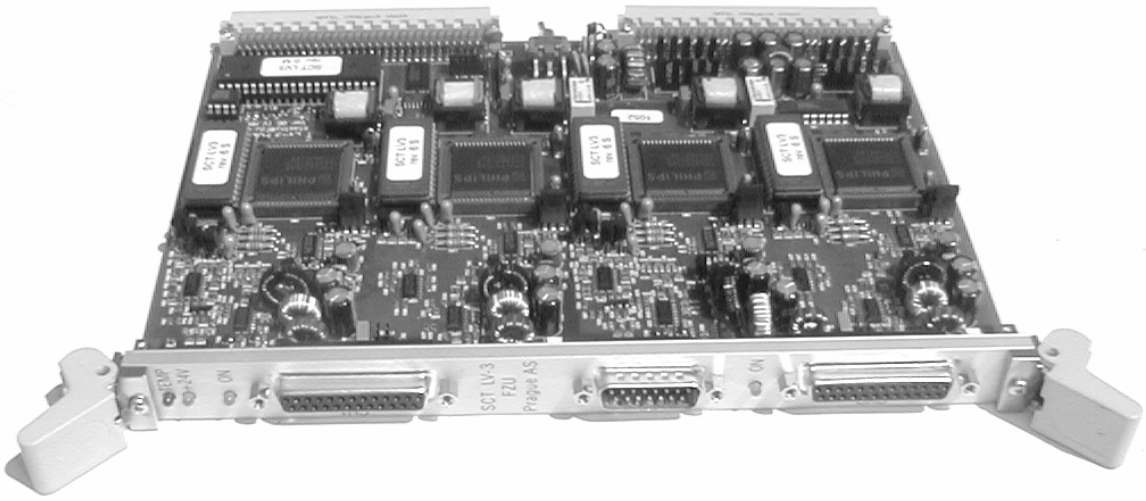

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CAUTION

Cooling:

It is imperative for the VME SCT LV Power Supply to be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50 degrees C.

Installation:

Crate power should be turned off during insertion or removal of modules in accordance with the VME specification.

It is strongly recomended to check the pinning of J2 connector (VME user-defined pins) before starting the VME crate, to avoid malfunction or fire on the backplane! See chapter `2.4 Connectors` **on this paper.**

ATTENTION

This product contains discharge sensitive devices, observe precautions for handling.

General Information

1.1 Purpose

This manual is intended to provide instruction regarding setup and operation of the VME SCT LV Power Supply.

1.2 Unpacking and Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. If the shipment is damaged in any way, please notify the consigner. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

1.3 Warranty

Firm Rybka warrants its instrument products to operate within specifications under normal use and service for a period of one year from date of shipment. Component products, replacement parts, and repairs are warranted for 90 days.

1.4 Product Assistance

Contact person for questions concerning installation and use of the VME SCT LV Power Supply:

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Product Description

2.1 Introduction

The VME SCT LV Power supply is a low voltage two channels power supply designed for feeding of ATLAS SCT modules. Each channel consist of two fully separated multi-voltage supplies, one for analogue and another for digital voltages. Both supplies are insulated from ground, i.e. from the crate power supply and VME parts by HF transformers.

2.2 Controls

The VME SCT LV Power Supply consist of two independent power channels. Each channel provides 5 power outputs, two current sources and two logical signals. Each power output is controlled in voltage, or in current limit. The logical signals are CMOS logic, LOW level is return sense voltage and HIGH level is Vdd sense voltage.

See next chapter for details.

2.3 Specifications

- Standard VME 6U by 160mm, single width
- A24/A16/D16/D08(O) VME module
- Responds to the following address modifier (AM) codes: 29, 2D, 39, 3D
- Input: 100mA at 5V, 2.5A at +12V & -12V (full load),auxiliary power input on P2
- Overheat indication at 60 deg C (Red LED on front panel is on)
- Output:

	Vcc	Temp.meas.	Vdd	VCSel0/1	PIN Bias
Vout min	3.2V	0	3.2V	0	0
Vout max/trip	9.5/9.8V	10.0V	9.5/9.8V	6.6V	10V
Iout max/trip	1.4/1.5A	80µA/-	1.4/1.5A	8mA	1mA/2mA
Monitoring	V/I	V	V/I	V	V/I
Prog.curr.limit/Warning	-/Yes	-/Disconnect	-/Yes	-/Yes	-/Yes
Set/Mon resolution	20mV/10mA	-/1°C	20mV/10mA	40mV/-	50mV/10µA

2.4 Connectors

The front panel of the VME SCT LV Power Supply supports three CANNON D-SUB connectors. Two female 25 pin connectors (CH0, CH1) for outputs and one male 15 pin connector (AUX) for interconnection to HV Bias Power Supply and HW Interlock.

P2 VME - Auxiliary Power Input Connector

+12V = 1c – 5c, Return = VME Gnd

-12V = 1a – 5a, Return = VME Gnd

Front Panel Connectors Pin Layout

CH0, CH1 - Female CANNON D-SUB 25 pins

		13	VCSel1
VCSel0	25		
		12	Vdd
Vdd Sense	24		
		11	Vdd Return
Vdd Ret.Sense	23		
		10	RESET
CLOCK SEL	22		
		9	PIN Bias
NC	21		
		8	NC
HV Return	20		
		7	TM2
HV Bias	19		
		6	TM1
SCREEN	18		
		5	NC
Vcc Sense	17		
		4	Vcc
NC	16		
		3	Vcc
NC	15		
		2	Vcc Return
Vcc Ret.Sense	14		
		1	Vcc Return

AUX - Male CANNON D-SUB 15 Pins

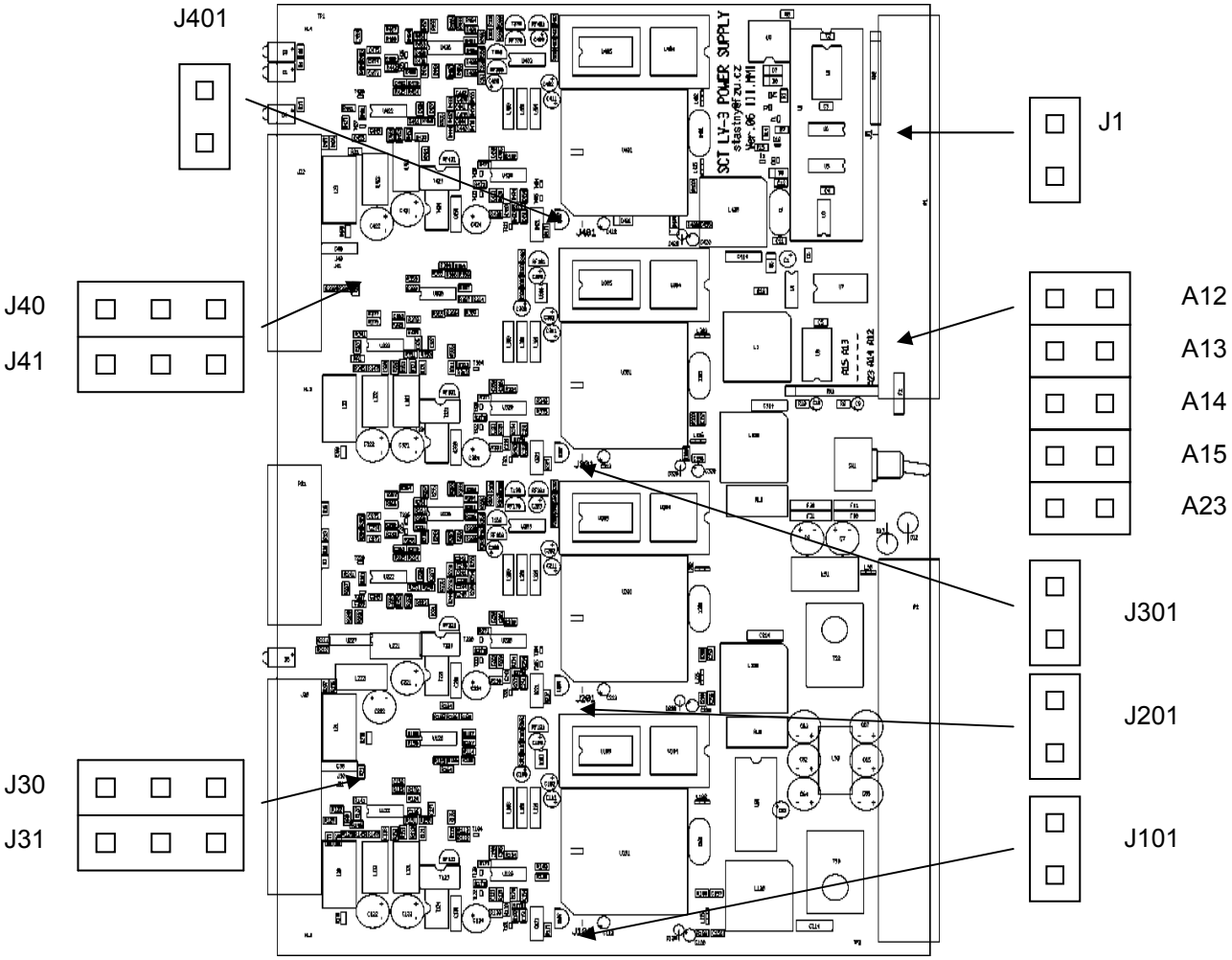
		1	NC
Signal CH1 ON	9		
		2	NC
HV Bias / CH1	10		
		3	NC
HV Ret. / CH1	11		
		4	HW Interlock
NC	12		
		5	HW Interlock Ret.
HV Bias / CH0	13		
		6	NC
HV Ret. / CH0	14		
		7	NC
Signal CH0 ON	15		
		8	NC

I n s t a l l a t i o n

3.1 General Information

Before inserting the VME SCT LV Power Supply into a VME crate, the VME base address must be set. There are five jumpers (A23, A15 - A12) for the base address setting and VME addresses A22 - A16 are hardwired to ones, i.e. 32 base addresses are available (FFF000 to FF0000 and 7FF000 to 7F0000 Hex).

```
          ____                ____
A12   |____| Open = 1    |____|        Example:
A13   |____|             |____|
A14   |____| Close = 0    o—o          Base Address
A15   |____|              o—o          Setting = 0x7F3000
A23   |____|              o—o
```



Screen connections: (J30 / J40) Screen direct - Vdd Return - Screen via cap 10nF
(J31 / J41) Screen direct - VME Gnd - Screen via cap 10nF

3.2 Cables

All cables must be connected correctly before VME SCT LV Power Supply starts up. Take care particularly of right connection of sense and return wires and also of the HW Interlock, if used. There are other jumpers (J30/31, J40/41) for screen connection of the cables to Vdd Returns or VME Gnd. The use of these jumpers may be in conflict with general grounding scheme!

3.3 HW Interlock

The HW Interlock is enabled by a jumper J1. If the jumper J1 is closed, the Start command must be used for switch on the channels. The Interlock Signal Polarity (Bit 7) in the Start command should be set regarding the extern control circuit.

Operating Instruction

4.1 Organization

There are 64 registers (byte width) mapped to the VME address space, i.e. 13 registers for monitoring and 15 registers for setting in each channel and 8 registers for the status and the control.

4.2 VME Address Map

Register Offset:

	CH0			CH1		
Mon. Values	Mon	Set	Scale	Mon	Set	Set. Values
Vc Out	0x00	0x1C	40mV	0x38	0x54	Reserve
Vcc	0x02	0x1E	20mV	0x3A	0x56	Vcc
Reserve	0x04	0x20	Deg C	0x3C	0x58	Reserve
Vd Out	0x06	0x22	40mV	0x3E	0x5A	Reserve
Vdd	0x08	0x24	20mV	0x40	0x5C	Vdd
VCSel0	0x0A	0x26	40mV	0x42	0x5E	VCSel0
VCSel1	0x0C	0x28	40mV	0x44	0x60	VCSel1
VPin Bias	0x0E	0x1A	50mV	0x46	0x52	Vpin Bias
Icc	0x10	0x2A	10mA	0x48	0x62	Icc Warning
Ipin Bias	0x12	0x2C	10μA	0x4A	0x64	Reserve
Idd	0x14	0x2E	10mA	0x4C	0x66	Idd Warning
Temperature0	0x16	0x30	Deg C	0x4E	0x68	Temp. Limit0
Temperature1	0x18	0x32	Deg C	0x50	0x6A	Temp. Limit1
		0x34			0x6C	Selects
		0x36			0x6E	Setting Flag
Ch. Status	0x70			0x74		
Reserve	0x72			0x76		
Module version	0x78		6	0x78		
Board Temp	0x7A		Deg C	0x7A		
Board Status	0x7C			0x7C		
		0x7E			0x7E	HW Restart /Interlock

4.3 Control and Status Registers

Selects:

Bit 0	Channel ON/OFF	1 = Channel ON
Bit 1	CLOCK SEL	1 = High Level
Bit 2	RESET	1 = Low Level
Bit 3 to Bit 7 Not used		

Ch. Status:

Bit 0	Analog Subch.	Parity Error
Bit 1	Digit. Subch.	Parity Error
Bit 2	Analog Subch.	Com. Error
Bit 3	digit. Subch.	Com. Error
Bit 4	Current / Temperature Limit	
Bit 5	Current Trip	
Bit 6	Channel SW ON	
Bit 7	Channel HW ON	

Board Status:

Bit 0	Power Fail
Bit 1	Overheat (T>70 deg C)
Bit 2	HW Interlock
Bit 3	Not used
Bit 4	Power Fail Latch
Bit 5	Overheat Latch
Bit 6	HW Interlock Latch
Bit 7	HW Interlock Enable (J1 close)

HW Restart / Interlock:

Bit 0 Restart	
Bit 1 to Bit 6 Not used	
Bit 7 Interlock Signal Polarity	(1 = Closed Loop)

4.4 Sense wires diagnostic

As an option to diagnose a malfunction around sense wires. It is possible to monitor a difference of the sense wire voltages. For more detail please contact the designer on e-mail (stastny@fzu.cz).