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Design and verification of an FPGA-based bit error rate tester

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Abstract

Bit error rate (BER) is the principle measure of performance of a data transmission link. With the integration of high-speed transceivers inside a field programmable gate array (FPGA), the BER testing can now be handled by transceiver-enabled FPGA hardware. This provides a cheaper alternative to dedicated table-top equipment and offers the flexibility of test customization and data analysis. This paper presents a BER tester implementation based on the Altera Stratix II GX and IV GT development boards. The architecture of the tester is described. Lab test results and field test data analysis are discussed.

The Stratix II GX tester operates at up to 5 Gbps and the Stratix IV GT tester operates at up to 10 Gbps, both in 4 duplex channels. The tester deploys a pseudo random bit sequence (PRBS) generator and detector, a transceiver controller, and an error logger. It also includes a computer interface for data acquisition and user configuration. The tester's functionality was validated and its performance characterized in a point-to-point serial optical link setup. BER vs. optical receiver sensitivity was measured to emulate stressed link conditions. The Stratix II GX tester was also used in a proton test on a custom designed serializer chip to record and analyse radiation-induced errors.

Keywords: Front-end electronics, bit error rate, FPGA, optical link

1. Introduction

High speed links are widely deployed in the data acquisition systems (DAQ) designed for the next generation high energy physics (HEP) experiments. In these links, data generated by the detector front-end are to be transferred to the remote processing stations at high rates with high accuracy and low

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latency. Trigger, timing and control signals are also to be transferred in the reverse direction. Most of these designs involve some form of multi-gigabit serial data transmission over fiber optics. To characterize the components and validate the system, BER tests are always performed in the laboratory and often times in a radiation environment.

As a fundamental and efficient measure of performance, BER tests are routinely carried out on table-top equipment which is dedicated and expensive. When the commercial FPGAs with embedded transceivers emerge, it becomes sensible to implement an FPGA-based BER tester as a low cost and portable alternative to the stand-alone testers. As a reconfigurable device, the FPGA-based BER tester can be easily customized to test various link schemes and system protocols.

The FPGA vendors normally provide users with pre-designed IP cores to reconfigure the embedded hardware. Various common functions and reference designs are also accessible. In terms of data acquisition and error analysis, however, the support is not as developed probably due to the high level of dependence on the specific tasks. We have developed a custom BER tester based on an Altera Stratix II GX transceiver signal integrity development board to demonstrate a point-to-point serial optical link with data rate up to 5 Gbps for the LHC upgrade applications [1,2]. We then updated the tester based on a Stratix IV GT development board and performed tests at up to 10 Gbps. In this tester, an error logging FIFO has been implemented to record both bit error data and link status. The tester's functionality was validated with a stand-alone BER tester. BER vs. receiver sensitivity was measured to emulate stressed signal conditions. The tester was also used in a proton test on a custom serializer chip with irradiation-induced errors recorded and analysed.

The next section presents the FPGA development boards as base platforms for tester implementation. The architecture of the BER tester is specified in section 3 followed by the description of various test setups and measurement results in section 4. Finally a conclusion is given in section 5.

2. FPGA platforms

2.1 FPGA and development board hardware

The Altera FPGA with embedded transceivers was introduced in early 2000 with the Stratix II GX device family. The highest serial data rates increase from 6.375 Gbps in Stratix II GX to 11.3 Gbps in Stratix IV GT and up to 28 Gbps in Stratix V GT. The Stratix II GX FPGA devices are available in production today, but the development board is updated to the Stratix IV edition.

These transceiver-enabled FPGA devices are equipped with dedicated hardware that can be configured to support many serial data communication standards including PCIe, SONET, Gigabit Ethernet, etc. For the targeted data offloading applications, standard communication protocols are neither efficient nor able to meet the timing requirements [3]. Thus the transceivers are configured in the basic mode where the data interfaces are adequate for BER tests at the physical layer and are transparent to custom protocol adaptations. Some mid-layer function blocks, such as 8B/10B encoder/decoder, can be incorporated as options. The 8B/10B coding effect on error distribution was studied in the GX platform. In the GT platform, all mid-layer function blocks need to be disabled for the transceiver to run at data rates of 10 Gbps and higher, in which case functions such as word alignment need to be implemented outside of the transceiver block in the FPGA main logic.

Development boards provide a versatile hardware platform for rapid prototyping projects. We used the Stratix II GX signal integrity development board from Altera to demonstrate the BER testing up to 5 Gbps and the Stratix IV GT PCIe development board from HiTech Global to demonstrate the BER testing up to 10 Gbps. The Stratix II GX board features an EP2SGX90 device. Six full duplex transceiver channels at up to 6.375 Gbps each are wired to the on-board SMA connectors. The USB connection as

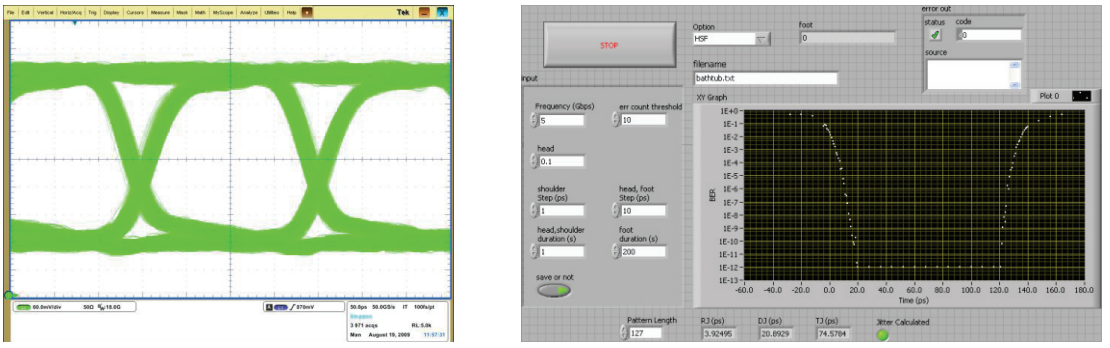
serial port enables communication with the host PC. The Stratix IV GT board features an EP4S100G2 device. Twenty-four full duplex transceiver channels at up to 11.3 Gbps each are wired on board. Four channels go to the SMA connectors and eight channels go to the high speed FMC (field programmable mezzanine card) connector for hosting custom modules. Two gigabit Ethernet ports are present for communication with the host PC. Other interfaces include PCIe edge connector, USB3.0/2.0 hosts and SFP+ connectors.

2.2 Transceiver characterization

To characterize the featured hardware we measured the waveforms and jitters of the transceiver transmitters. The eye diagram in figure 1(a) shows the electrical output of a Stratix II GX transmitter at 5 Gbps with zero pre-emphasis. It was compliant to the industry standards such as 4G Fiber Channel and 10 Gigabit Ethernet scaled to the 5 Gbps operation data rate. This validated the use of the Stratix II GX transmitter to characterize the downstream data link components. The eye diagram of the electrical output of a Stratix IV GT transmitter at 10 Gbps was also wide open. But higher bandwidth oscilloscope probes are needed for the complete characterization.

The transmitter driven by random test patterns was tested by the receiver of a commercial stand-alone BER tester programmed to receive the same pattern. The resulting BER bathtub curve, i.e., BER measured against the sampling time scanned from the left edge to the right edge of a data eye, provided necessary information to calculate the total jitter. The bathtub curve in figure 1(b) shows the electrical output of a Stratix II GX transmitter at 5 Gbps scanned. A total jitter of 0.225 UI (unit interval) or 45ps was measured, which was also standards compliant. The reference clock to the Stratix II GX transceiver was provided by an on board 156.25MHz oscillator and the reference clock to the Stratix IV GT transceiver was provided by an external clock source of 312.5MHz.

We compared the BER results of the Stratix II GX transceiver, the Stratix IV GT transceiver and a commercial stand-alone BER tester over the same optical link at 5 Gbps operation data rate. The link BER vs. received optical modulation amplitude (OMA) test setup will be discussed in detail in section 3. Receiver sensitivities of the same optical link measured by these testers were less than 1dB in difference, which was comparable to the measurement error limit.



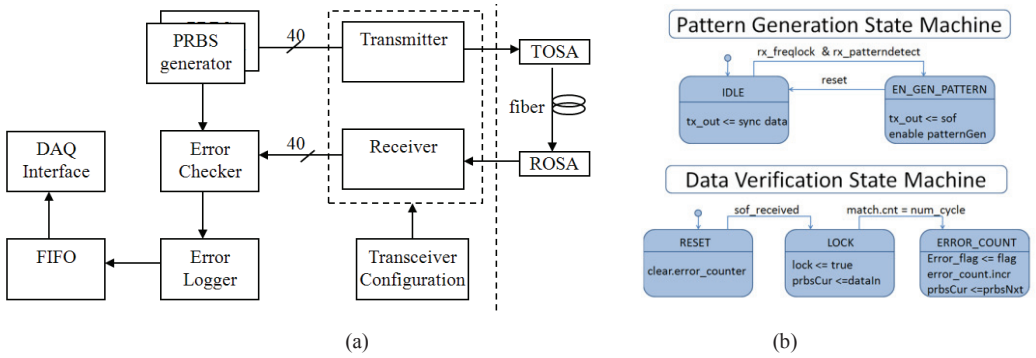
(a) (b)

Fig. 1. (a) Stratix II GX transmitter output waveform at 5 Gbps; (b) Stratix II GX transmitter output scanned by a stand-along BER tester receiver at 5 Gbps.

3. BER tester architecture

The custom BER tester was developed as an open source firmware and software package. The main blocks of the HDL (hardware description language) codes were pattern generator, error checker, transceiver block, error logger and user interface, as shown in figure 2(a). The LabVIEW routines included the library calls to the USB and Ethernet chips, the data acquisition and hardware configuration data flows, as well as the controls for automated measurements.

Pseudo random bit sequence (PRBS) patterns of 2^7-1, 2^{23}-1 and 2^{31}-1 bits were generated using parallel to serial converters for low latency. The internal data bus was 40 bit wide so that the main FPGA logic could keep up with the serial transceiver. One of the benefits of using PRBS was that long and stressed patterns could be produced without using a lot of memory. Another benefit of using PRBS was that the patterns were time correlated, thus the boundary synchronization was not necessary for the BER testing at the physical layer. In the Stratix II GX tester, the word aligner was integrated in the receiver data path as a common practice. Pre-defined training patterns were transmitted and verified for the link to establish word boundary and for the state machine to advance to the link-lock mode, as shown in figure 2(b). The error detector used the incoming data as seeds to generate the expected patterns in the lock state. After a certain number of error-free cycles, it switched to internal seeds so that incoming erroneous bits could not disturb the error checking of the detector. In the Stratix IV GT tester, the word aligner was removed for the transceiver as required by the vendor for the hardware to run at 10 Gbps and above. The training patterns were also dismissed. Since the PRBS patterns could be verified without a set boundary, the tester worked with the rest of the process flow.



(a) (b)

Fig. 2. (a) Block diagram of the custom BER tester function blocks (including connections to an optical link); (b) State machine of the BER tester pattern generator and detector structure.

An error FIFO was instantiated to communicate with the external IO interface. The error logger monitored and recorded five types of events to the FIFO as shown in table 1. When the link-lost events due to loss of signal or loss of clock occurred, they were always logged in a reserved section of the FIFO. During a link-lost event, bit error was not relevant and was no longer recorded. Instead the duration of the link-lost event could be derived when the link re-locked. More information from the error event could be retrieved from the recorded XOR pattern of the received and expected data given the time stamps since the pattern was a known PRBS.

The user interfaces were developed to establish simple communication protocols with the external IO chips. They were the USB in bulk FIFO mode for the Stratix II GX tester and the Ethernet in GMII mode for the Stratix IV GT tester.

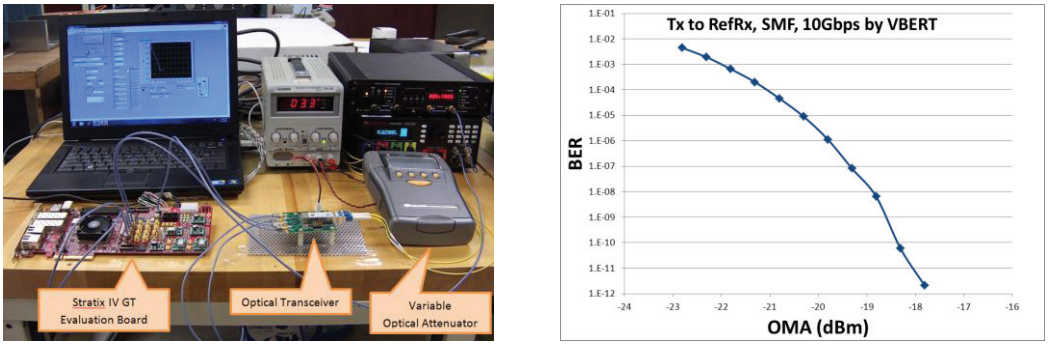
Table 1. Error FIFO data structure

Event	ID	Stamp	Data	Note
Single error event	001	yes, 48bit timer	IN XOR Exp'd	
Link locked	010	yes, 48bit timer	Exp'd	Error checker locked to generator
Link lost	011	yes, 48bit timer	Exp'd	Receiver CDR lost synchronization
FIFO full	100	yes, 48bit timer	Exp'd	Stop recording error events
FIFO ready	101	yes, 48bit timer	Exp'd	Resume recording error events

4. Test setup and results

4.1 In lab verification

The basic BER testing was performed on a point-to-point optical link. The tester's transmitter drove the transmitting side of an optical transceiver and the tester's receiver was connected to the receiving side of the optical transceiver. A variable optical attenuator (VOA) was inserted in the fiber loop to induce stress. The bit error rate was then measured at different attenuation levels. Figure 3(a) shows the setup where a Stratix IV GT board was connected to a PC and an optical transceiver. The optical transceiver was routed to and from an optical loop with a VOA. In figure 3(b) we plotted the BER vs. received optical modulation amplitude with the link operating at 10 Gbps. In the noise dominated region, this curve followed the general trend of the error function of a Gaussian distribution. Receiver sensitivity, the minimum optical modulation power for achieving the bit error rate of 10^{-12} or better, could be derived from the curve. The receiver sensitivity of the reference link was measured at about -17.5 dBm, comparable to the vendor's specification and to the measured result from a table-top tester. The BER testing using the Stratix II GX board, operating the same link at 5 Gbps, resulted in a similar curve with slightly improved sensitivity as expected.



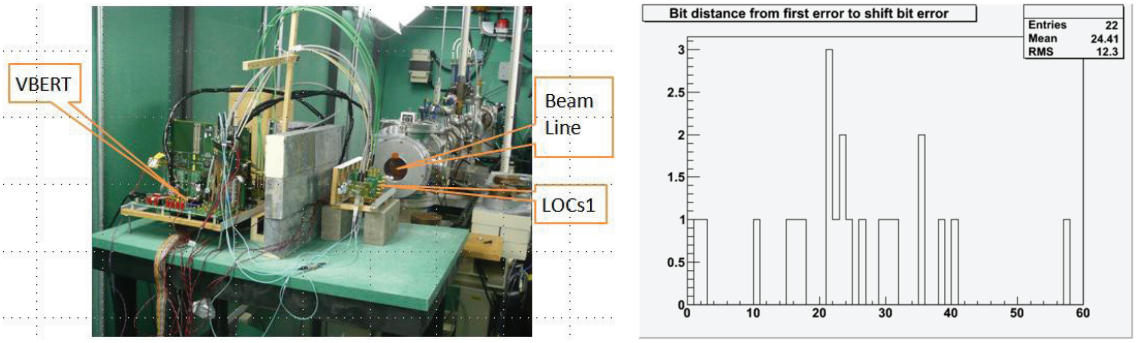
(a) (b)

Fig. 3. (a) Picture of the Stratix IV GT tester routed to a point-to-point optical link; (b) BER vs. OMA measurement of the reference link using the Stratix IV GT tester.

4.2 Radiation test application

The Stratix II GX tester was deployed in a radiation test on a 5 Gbps custom designed serializer chip using a 200 MeV proton beam at the Indiana University Cyclotron Facility. Figure 4(a) shows a picture of the setup where parallel PRBS data generated by a cyclone II FPGA were injected to the serializer and data output were feed to the Stratix II GX receivers. Two serializer boards were placed in the beam and the rest of the system was in the shielded area. When the flux reached the highest rate tested, a few errors occurred in both channels under radiation. We observed two types of single-event errors: single bit errors and synchronization errors. The single bit error events did not affect the link status afterwards, whereas the synchronization error events required a receiver reset.

Post-test analysis of the error logging files showed that the synchronization errors resulted in exactly one bit shift forward or backward, after a period of burst errors. The distribution of burst error lengths is shown in figure 4(b). The bursts were heterogeneous yet constrained within two data frames, i.e., 80 bits of serial transmission. This observation suggested that for devices that may suffer from the synchronization error events, a tester scheme like that of the Stratix IV GT, where the detector does not depend on boundary alignment, can be helpful to avoid the manual resets during testing.



(a) (b)

Fig. 4. (a) Picture of the Stratix II GX tester (VBERT) deployed in a radiation test of a serializer (LOCs1) chip; (b) Distribution of burst error lengths of synchronization error events

5. Conclusions

A custom FPGA-based bit error rate tester was developed to characterize and validate a serial optical link. The hardware platforms were the Stratix II GX development board operating at up to 5 Gbps and the Stratix IV GT development board operating at up to 10 Gbps. In addition to the PRBS generator, detector and transceiver blocks, the error logger and user interface were implemented for data acquisition and targeted test analysis.

The tester was cross validated with stand-alone equipment. BER vs. receiver sensitivity of an optical link was measured. The tester was used in a proton test on a custom serializer chip where two types of radiation-induced errors were recorded and analysed. A number of coding schemes and transmission protocols were explored. These experiments showed the benefits of using the FPGA-based BER tester in system prototyping and test customization. Currently, a single transceiver block supporting four duplex channels was enabled on each of the Stratix II and IV platforms. An additional twelve transceiver channels can be enabled on the Stratix IV GT platform to accommodate module cards with FMC connection, extending its BER testing capability to high channel count and parallel systems.

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