SIMULATION AND CHARACTERIZATION OF THE FRONT-END OF SDD IN ALICE ITS

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Abstract

The front-end of a semiconductor detector usually requires a charge amplifier followed by a shaper and a voltage ADC. This typical solution is not suitable for Silicon Drift Detectors in ALICE. We have performed many realistic simulations concerning the ALICE event, the detector and the front-end electronics to optimise the structure and the parameters of the readout electronics. The solution we propose consists of a transimpedance amplifier followed by a switched capacitor array analog memory and an ADC.

1. INTRODUCTION

The constraints imposed by high-energy physics experiments to the front-end electronics are becoming more and more rigorous. The higher the number of channels, the smaller the size of the electronics, the quantity of matter through the particle tracks and the power consumption. At the same time, the noise has to be as low as possible to allow better resolutions and efficiency.

Clearly, the challenge is offered to technology, but a lot of work is possible designing appropriate solutions for a fixed technology. With the help of an accurate simulation relating to the whole generation chain, signal treatment and reconstruction of the transported information, the values to be assigned to the specific parameters of the electronics project, crucial for the precision and efficiency of the whole measurement, can be defined. This publication presents the preliminary results of our study of the most suitable electronics for the readout of the Silicon Drift Chambers used in the Inner Tracking System (ITS) of ALICE ([1]÷[2]÷[3]).

ALICE is a high-energy physics experiment that will be performed using LHC (Large Hadron Collider) to explore the 'quark gluon plasma'. The six innermost cylindrical layers of high-resolution detectors constitute the Inner Tracker System (ITS), whose basic functions are low-momentum particle identification and tracking, and secondary vertex reconstructions. The third and the fourth layers will be arranged with SDDs (Silicon Drift Detectors).

2. SILICON DRIFT DETECTORS IN ALICE

The SDDs ([4]÷[5]÷[6]) for ALICE will be large-area planar detectors (8.7x7cm) (Fig.1) of a 300 μm high resistivity n-type silicon wafer. An external high voltage applied to an integrated on-board divider fully depletes the volume of the detector and generates a drift field inside towards the edge of the detector where 384x2 n^+ anodes with a pitch of 210 μm are implanted.

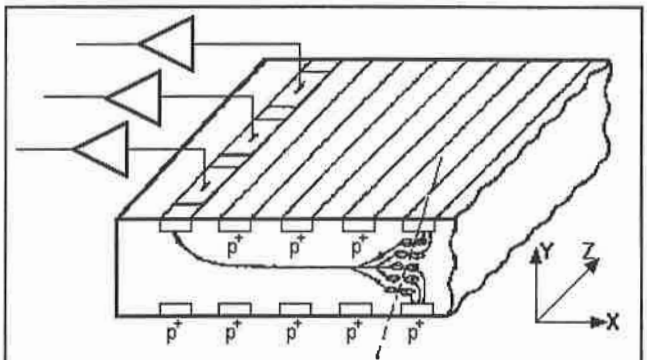

Fig. 1 - Silicon Drift Detector

A charged particle crossing the detector releases energy creating electron-hole pairs along its track. The holes are removed by the nearest electrodes, but the electrons, focused in the middle plane of the detector are collected by the anodes just in front of the impact point by the drift field. During its motion, the electronic cloud diffuses and its gaussian widening depends primarily on the distance of the impact point from the anodes (X - drift coordinate). The drift field foreseen is about 450 V/cm, with an electron velocity of 6 μm/nsec.

The information given by a SDD about an interacting particle, is a collection of signals, suitably sampled, on the anodes in front of the impact point. In ALICE the sampling frequency is 40 MHz.

A conservative proposal for the readout of the SDDs foresees the acquisition and the further analysis of all the signals over the threshold (zero-suppression). The two spatial coordinates will be reconstructed off-line by means of the centre-of-mass method, taking into account the influence of the amplifier response in the signal time developing. Both the resolutions vary with the localisation of the point of impact [7]. In Fig.2 the SDD resolutions in both directions vs. X, the distance of the point of impact from the anodes, are depicted for single tracks.

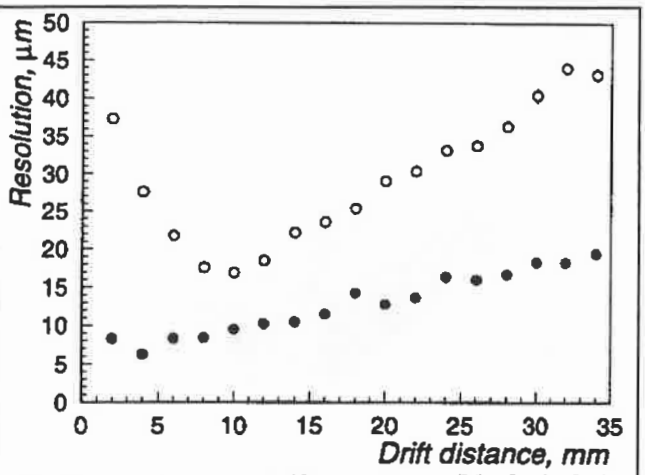

Fig. 2 - Resolution in drift coordinate (black circles) and in anode coordinate (white circles).

A general scheme of the readout is shown in Fig.3 [3]. In this system the signals coming from each anode of the detector are sent to one input of a 32-Input Preamplifer-Shaper (PAS) [8] whose outputs are connected to the inputs of a 32-Input Analog Memory (AM) [9]. The AM must continuously sample the analog signals at 40 MHz and store all the data. When some suitable conditions are detected, a trigger signal stops the write phase. Then a read phase begins the data transfer, at low rate (1÷3 MHz), to an ADC for digitalisation. Finally the data will be sent to the acquisition system.

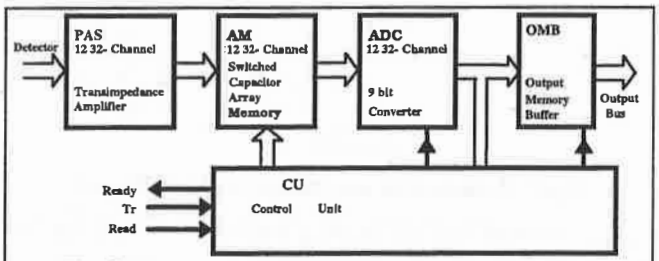

Fig.3 The readout of the Silicon Drift Detector

3. EVENT, SDD AND READOUT SIMULATION

The physical event is the collision between two ions accelerated by the collider, which leads to a shower of charged particles impinging on the detector. These have a realistic distribution both in space and as far as energy loss is concerned. The our set of '*generation data*' comes from three events, i.e. central collisions Pb-Pb generated by the SHAKER code [10] with charged particle rapidity density of dN/dy = 8000 and a pseudo-rapidity region of $-1.3 < \eta < 1.3$ ($30° < \theta < 150°$). Besides, productions of $\pi°$, η and their decays to two γ were included as well, leading to 38000 charged particles and γ per event. The generation data set consists of about 50,000 single charged particles with a uniform distribution in X (1000÷35000 μm) and in Z (-105÷105 μm). Their initial produced charge distribution is shown in Fig.4. In the detail inside the box, it is shown the same distribution up to 10 mips.

The following step of the simulation takes into account the interaction of the charged particle with the detector and the creation of Q hole-electron pairs along the particle path inside the SDD. All the tracks are supposed to be normal to the detector surface. So the generated electronic cloud has an initial δ-distribution centred at the impact point (X,Z) and focused by the field on the middle plane of the detector (half thickness). The detector is realistically biased, therefore the electronic cloud will migrate towards the anodes facing the impact point. At the same time, the cloud will spread in space, according to the diffusion laws for charge carriers in silicon.

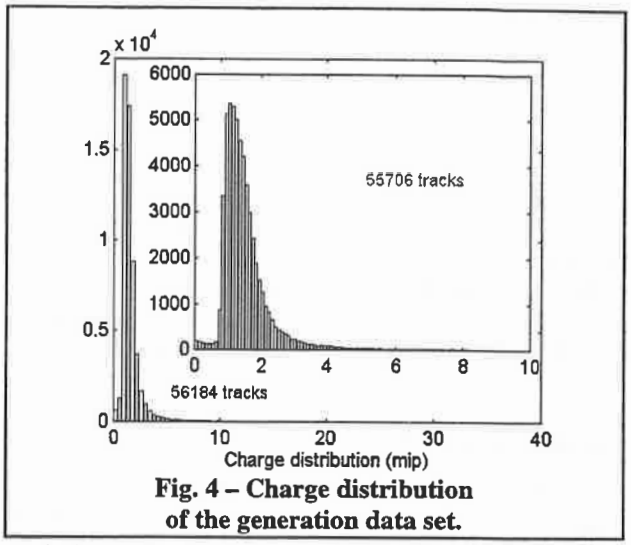

Fig. 4 – Charge distribution of the generation data set.

The current signal feeding the preamplifier is:

$$I_j(t) = \frac{q_j}{\sqrt{2\pi}\sigma_t} \exp\left[-\frac{(t-t_0)^2}{2\sigma_t^2}\right] \qquad (1)$$

$$\sigma_t = \sigma / v = \frac{\sqrt{2 D_e t_0}}{v}$$

where D_e is the diffusion constant for electrons in silicon, t_0 is the drift time, v is the drift speed and q_j the total charge collected by the j-anode.

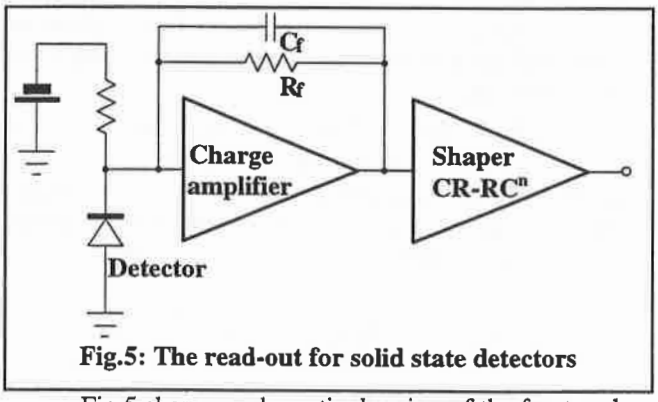

Fig.5: The read-out for solid state detectors

Fig.5 shows a schematic drawing of the front-end for solid state detectors. The preamplifier is used to obtain a voltage step proportional to the charge coming from the detector. A further filter (shaper) reduces noise in order to improve performance in terms of resolutions and efficiency.

The model chosen for the simulation of this device is the one relating to a linear transimpedance amplifier with semi-gaussian shaper RC-CR^n. The delta response is shown in Eq.2 where τ_p is the shaping time and τ the time constant RC=CR:

$$V(t) = k\frac{t^n}{n!}e^{-\frac{t}{\tau}} \qquad (2)$$

$$\tau_p = n\tau$$

For n=4, the correlation efficiency between a gaussian with a spread equal to σ_{ampl} (half of the shaping time) and the CR-RC^4 results in 98.7%. Therefore, in the course of the simulation gaussian output signals were considered, allowing shaping time to vary, so as to establish what effects this had on the resolution and on overall efficiency.

4. NOISE EFFECTS

Noise greatly affects the overall readout characteristics. To avoid ghost tracks, simulated by noise, a threshold must be set. This latter increases with noise decreasing efficiency too. Besides resolution, both for charge and position worsens. It is therefore reasonable to reduce noise as much as possible. Due to the power consumption increase, a more efficient cooling system would lead to an increased physical noise caused by the multiple scattering.

The source of noise is localised in: the detector itself, the preamplifier-shaper, the sampling system, and the ADC. The first one is negligible. We can decrease the preamplifier noise adding a suitable filter. In order to achieve a better noise the signal shapes are changed. This fact, in turn, affects both resolutions, efficiency and power consumption. The sampling system, that is the AM generates a noise too. Since it depends essentially on the matching of capacitors inside the system, we use a suitable value already obtained for a dedicated AM [9]. As regards digitalisation we will introduce it as already mentioned in the previous section. The quantization error will be introduced using three different values: 8, 9 and 10 bit.

The problem we want to solve is to find the best filter, and the minimum number of bits compatible with power dissipation.

Noise depends both on design and process parameters. We have chosen for this work a CMOS .8 μm, double-poly, double-metal process. We have investigated all the contributions of noise: flicker (ENC_f), thermal (ENC_t) and shot (ENC_s). The total noise ENC_{tot}, is given by:

$$ENC_{tot} = \sqrt{ENC_f^2 + ENC_t^2 + ENC_s^2} \quad (3)$$

The first transistor from which the noise essentially depends is a PMOS. The analysis has been performed as in previous papers ([11]]÷[[12]). We have assigned some parameters as, for instance, the leakage current ILk, the capacitance Cd of the detector and the number of integration. The number of integration n was chosen as 4 to have a gaussian response and a better noise.

The first attempt to optimise was made without any limitation for ts ($\tau_s = n\cdot\tau$) τ is the time constant of the filter integrator), ID (the bias current of the first transistor and W (first transistor gate width) ranges. A minimum noise of 38 e$^-$ was achieved. The results are quite paradoxical! Only W = 1218 μm and L = 1 μm are reasonable

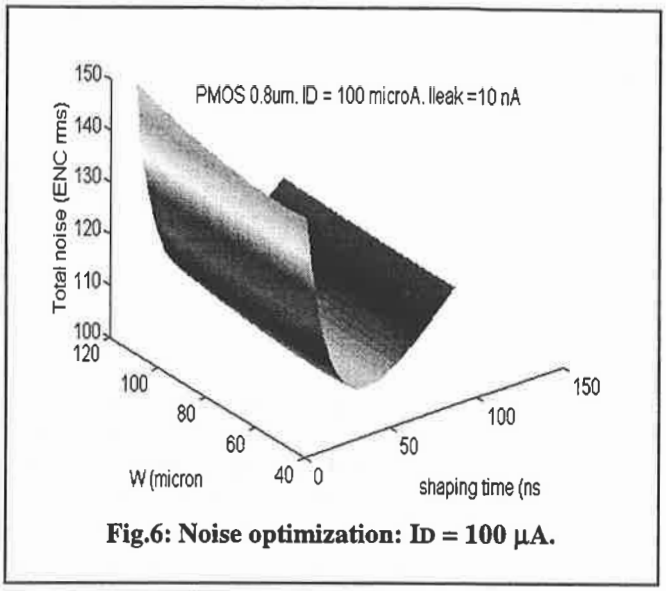

Fig.6: Noise optimization: ID = 100 μA.

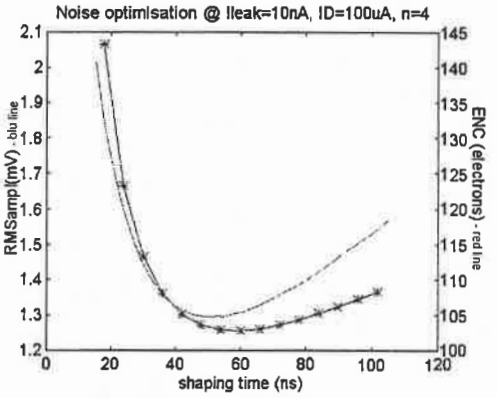

Fig.7: Preamplifer optimization: ID = 100 μA.

values. Nevertheless the shaping time of 3.2 ns and the ID current of 7.6A are values unrealistic!

A limitation for power reasons has to be introduced, so the ID has to be not more than 100 μA. It means that using 2.75 VDC for its supply then about 300 μW is its power need.

A new optimisation has led to the results shown in Fig.5: W ≈ 61 μm is almost independent of ts. With W = 60 μm it is possible to reach a minimum noise of about 115 e rms using ts ≈ 60 ns. (Fig 6).

Taking into account that a filter CR-RC^4 gives a quasi-gaussian response, the noise in volts can be calculated in a fixed dynamic range (in our case 2V) starting from the optimised ENC. Finally, a parallel code [13] has been developed to generate the noise in the time domain.

5. EFFICIENCY AND RESOLUTIONS

One of the problems when we try to analyse the simulated data is the cluster localisation inside a noise matrix. The chosen algorithm detects a cluster if two successive samplings of the same channel exceed an opportune threshold. The inefficiency is the number of 'lost' clusters (not identified) over the total number of simulated tracks.

The impact point and the charge released by the particle are reconstructed by means of centre-of-mass method and opportune integration of samplings.

We fixed the preamplifier input/output dynamics, the noise spectrum, the AM uncorrelated noise, and we varied the ADC bit number and the shaping time. Figs.8-11 show the obtained inefficiency and resolutions.

The results show that 9 or 10 bits give comparable performances, while 8 bits are not indicated. The best shaping time is a compromise between the two opposite behaviours of spatial resolutions with respect to the charge resolution. A shaping time of about 50 ns seems to be a good choice, both for inefficiency and for resolutions. A fast shaper response has to be excluded, because of the efficiency deterioration. With higher shaping times there is a light amelioration of efficiency, but there is a degraded charge resolution, especially in the first centimeter. Figs.12-13 show the X distribution of inefficiency and resolutions. A part from scale factors, spatial resolutions behave as shown in Fig.2.

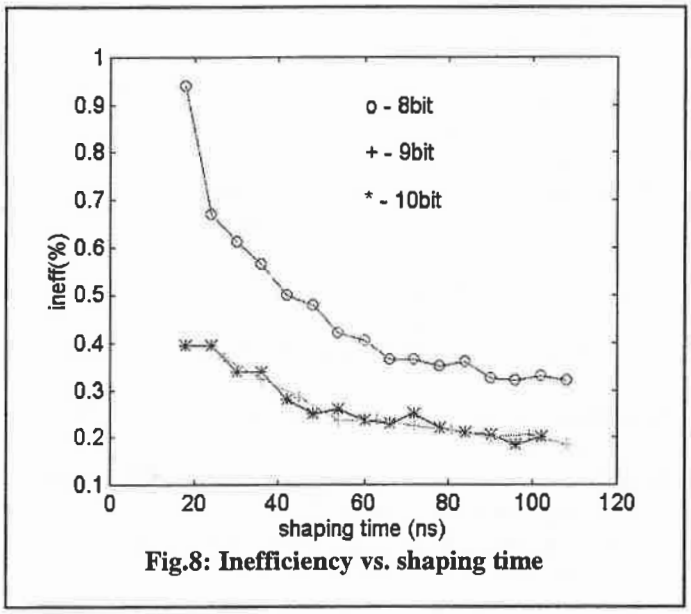

Fig.8: Inefficiency vs. shaping time

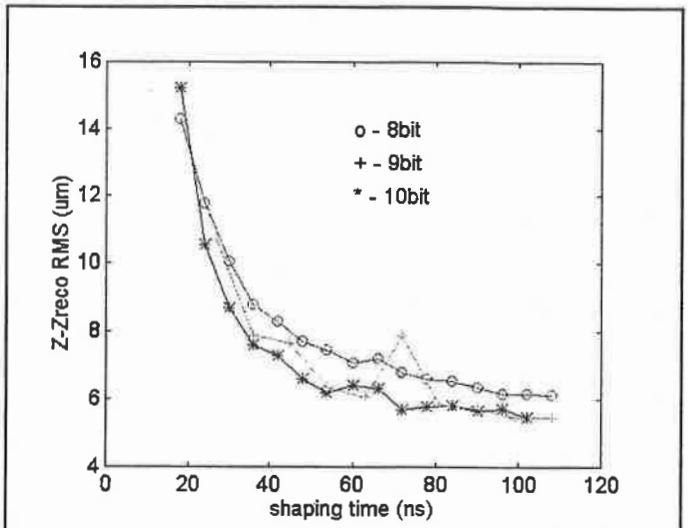

Fig.10: Anode coordinate resolution vs. shaping time

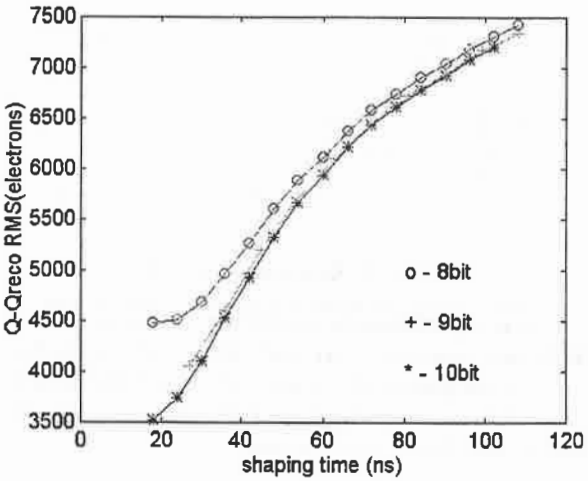

Fig.11: Charge resolution vs. shaping time

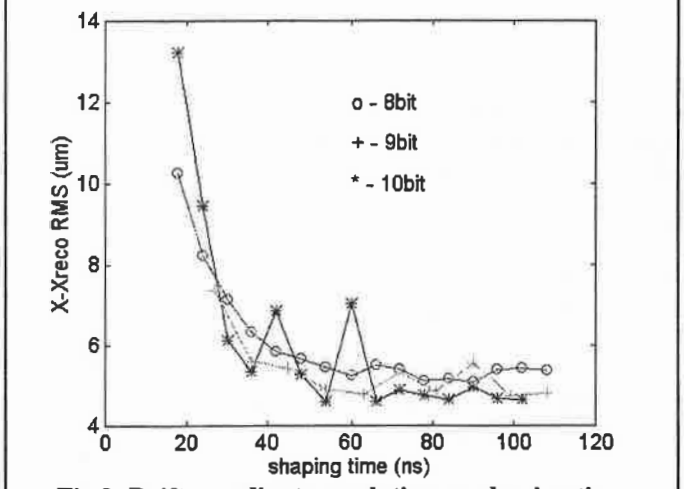

Fig.9: Drift coordinate resolution vs. shaping time

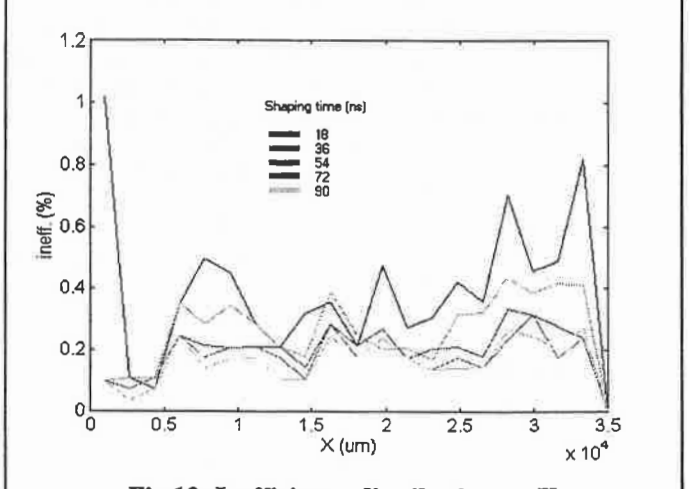

Fig.12: Inefficiency distribution vs. X

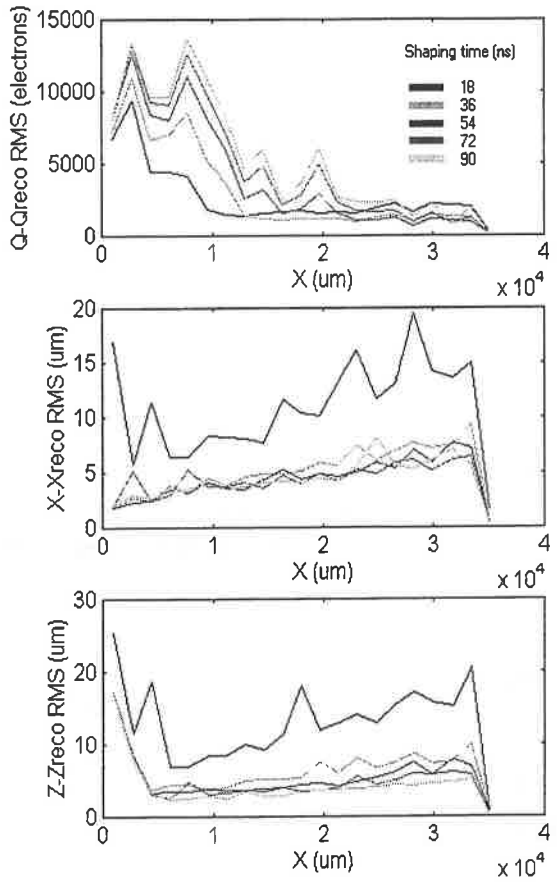

Fig.13: Resolutions vs. X

We also performed a preliminary comparison between OLA performances [14] and other realised and/or designed preamplifiers (Gramegna [15], SUPERSBREX [8], PRELUD [16], ALIAS [17]). Table I resumes the characteristics and the obtained results.

6. CONCLUSIONS

We performed a simulation of the ALICE event, the SDD response and the front-end electronics, designing and coding a software to study the variation of efficiency and resolutions when some crucial parameters (ADC bit number, shaping time, etc...) are modified. We introduced a noise optimisation taking into account the assigned constraint regarding power consumption. The results obtained show that a shaping time of 55 ns and a 9 bit resolution ADC can guarantee good performances, according to the technical proposal requirements.

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	Shaping time (ns)	ENC (electrons)	Q range (fC)	V range (V)	Inefficiency (%)	X resolution (μm)	Z resolution (μm)	Q resolution (fC)
OLA 8bit	55	250	8	0.3	0.37	9.65	10.13	3.28
OLA 9bit	55	250	8	0.3	0.25	13.9	13.7	3.28
Gramegna	50	120	50	2	0.4	6.6	8.0	0.36
SUPERSBREX	20	240	100	0.4	8.85	98.6	98.3	1.42
PRELUD	15		28	2.6	0.4	6.5	8.4	0.92
ALIAS	55	140	28	1	0.6	6.8	9.7	0.56

TAB. I – Comparison between SDD preamplifiers (realised and/or designed)