READOUT AND PRETRIGGER LOGIC OF THE HERA-B HIGH-P_T PRETRIGGER.

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Abstract
The high-p_T pretrigger has been proposed for HERA-B experiment. Dedicated pretrigger logic is needed for selection events out of data streams coming with typical rate of few 10^{12} hits/s. The paper describes concept of pretrigger logic and data processing which provide necessary speed and flexibility for pretrigger selection criteria.

1 Introduction

The high-p_T trigger provides HERA-B experiment with ability to measure CKM unitarity triangle angles α and γ by detection of the $B \to \pi^+\pi^-$ and $B \to K^\pm\pi^\mp$ decays [1]. The expected numbers of reconstructed events are 500 and 750 per year correspondingly. The goal of the high-p_T pretrigger is selection of candidates for particles with the large transverse momentum to initiate the First Level Trigger(FLT) tracks finding process. The high-p_T pretrigger is organized using approximately 19000 pads of different sizes distributed among three layers of chambers located in the magnet. There is a projectivity between position and sizes of correspondent pads in three layers with respect to the vertex position. Pads' sizes are varying in correspondence with their distance from the beam. The basic track selection algorithm of the high-p_T pretrigger is: each pad of the first chamber layer (PT1) maps to three adjacent pads in the second layer PT2, and each pads of the PT2 maps to two adjacent pads of the PT3 (fig.1). The tracks with high-p_T produce signals in the projective or adjacent pads of three chamber layers. Specific pretrigger logic must provide selection and encoding events and distribution the parameters of few 10^7 tracks out of few 10^{12} possible roads per second.

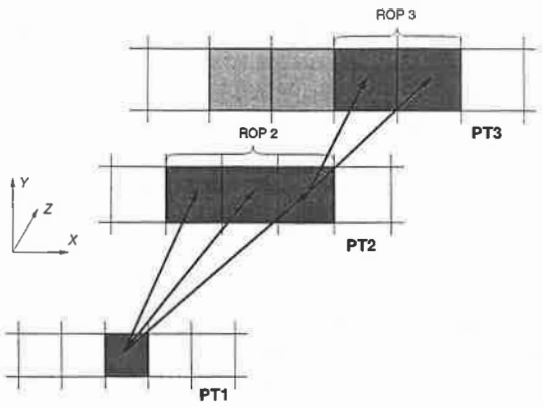

Figure 1: High-p_T pretrigger track selection algorithm.

2 Pretrigger implementation

The main components of the high-p_t pretrigger system are three layers of gaseous pad chambers placed in the magnet, on-chamber front-end electronics, front-end drivers and pretrigger logic. The outer region of detecting layers is covered by straw tube chambers with cathode pad readout. These chambers are developed at Princeton University, Cincinnati [2]. The inner region is covered by gas pads of different sizes assembled in gas pixel chambers developed in ITEP, Moscow [3].

Detailed description of readout and pretrigger logic is given in [5]. The pad signals are routed from the chambers to front-end cards mounted at both sides of the chamber stations' frames outside the detector fiducial volume. It is done by using low-mass flex cables which have been specially developed for that.

Front-End Driver (FED) fulfills the tasks of interface for FE output signals both to the data acquisition system (DAQ) and to the pretrigger logic, and either synchronization function - labels passing data with timing information (bunch crossing number). It is placed close to the detector. Data are being transmitted from FEDs to the pretrigger logic located outside the HERA-B detector area via optical lines.

Every bunch crossing chamber's data together with timing information are being transfered to the pretrigger logic. The main task of the pretrigger logic is to define track candidates by performing coincidences of pads' signals with required topology and transforming the result into streams of initial track parameters coming to the appropriate FLT processors. This task is being carried out in real-time with short delay. Information from chambers is being accepted synchronously with the HERA clock(10.4 MHz), the track parameters are being transmitted to FLT processors at a typical rate of 40 MHz. Some additional facilities to provide monitoring and testing functions, are implemented either.

3 Readout

The geometry of readout signals from pads to the front-end cards is horizontal. Such geometry has been chosen due to two main reasons: to minimize the number of overlapping hits (the hits which involved in coincidence procedures in different boards of the pretrigger logic) and due to arrangement of pads in vertical direction more regular than in horizontal. The ASD8B chip is used in FE cards[4]. It has 8 amplifier-shaper-discriminator channels.

Every bunch crossing each FED reads in synchronously 1024 hit signals coming from FE cards. These data stream are being fan-outed in two paths: transmitted to the pretrigger logic and loaded to pipeline memory to be output then to the DAQ in accordance with the FLT request. To reduce the number of transmition lines data are being transfered in serial form via high-speed optical link lines. Reduction factor is approximately 42. To transfer hits out of 19000 pads to the pretrigger logic 480 optical links are used. Fast link chips MC100SX1451 (Motorola) transmit data in serial form with the speed which allows to transfer two 32-bit words per bunch crossing.

4 Pretrigger Logic

Main tasks of the pretrigger logic are:

1. Receive streams of logical signals from front-end drivers and select data which match to the pretrigger track selection criteria.

2. Translate selected data into streams of track's parameters (messages).

3. Distribute messages among appropriate FLT processors in accordance with their regions of interest.

Besides, pretrigger logic must provide ability for monitoring its performances and performances of input data, and either provide ability for updating of constant in order to cope with unexpectable operating conditions.

Essential requirement is flexibility for coincidence algorithm to provide ability for further optimization of the pretrigger.

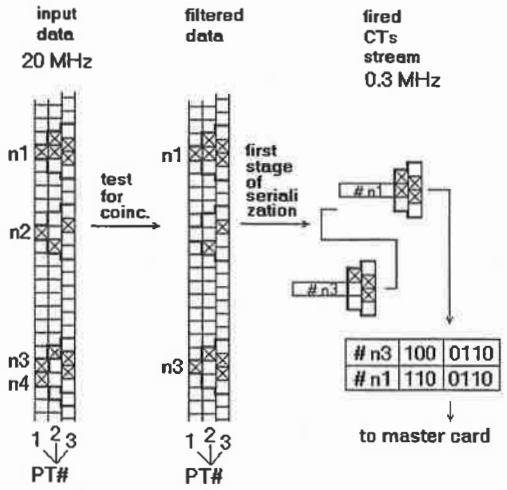

Figure 2: Schematic view of data processing on a pretrigger board. Coincidence trees n1 and n3 have at least one hits' combination which matches to the pretrigger algorithm, while patterns n2 and n4 have no one.

The following concept and data processing algorithm are put into development of pretrigger logic [5]. The pretrigger logic electronics has sectional structure and is composed of boards of two types - the Pretrigger Boards and the Master Cards. Each section consists of one master card and a number of pretrigger boards. Two processes run asynchronously in each section: filtering and serialization procedure at pretrigger boards, and serialization-encoding process at the master card. Output of the first process is the input for the second one. A pretrigger board executes filter procedure for raw data and diminishes output data rate to acceptable level. A pretrigger board serves complete rows of pads of three chamber layers. It receives data from six half-layers of chambers and tests them for coincidence. Data which match to the pretrigger algorithm are stored for necessary time, data items are being extracted from stored data and transmitted in special format to the master card. The master card acquires data items from a group of pretrigger boards, transforms them into a number of messages and distributes messages among FLT processors.

Average rate of messages generated by a master card can not be more than one track candidate per bunch crossing. This restriction determines maximal number of pretrigger boards served by one master card. According to the above restriction and the results of

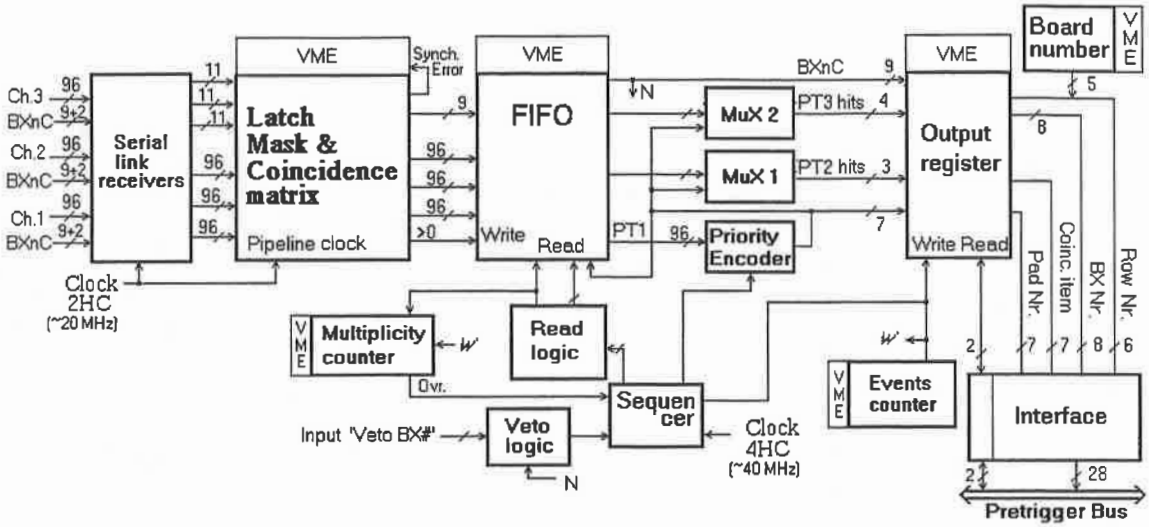

Figure 3: Schematic of a Pretrigger Board.

MC simulation of the pretrigger rate distribution over the detection area the pretrigger logic has been divided into independent sections with one master card in each.

Schematic view of data processing at a pretrigger board is shown at fig.2. Data are being processed in items of 'coincidence trees'(CTs). This term means a set of pads involved in the coincidence procedure together with one pad of the first layer. For the basic pretrigger algorithm (fig.1) a CT consists of eight pads - 1, 3 and 4 pads of the 1st, 2nd and 3rd layers correspondingly. The position of fired pad in the 1st layer defines a point of track, the combination of fired pads in the 2nd and 3rd layers are used to determine the direction of track(s). CTs are being encoded at pretrigger boards in the following way - root hit obtains its individual number and the rest seven bits remain as they are. The stream of CTs is being sent to the master card. One or more track roads can be derived from a fired CT at a master card using more detailed algorithm.

4.1 *Pretrigger board*

The main tasks for a pretrigger board are the following:

Receive 3 streams of logical signals via optical link lines;

The first stage of data selection by performing the coincidence procedure;

Serialization of selected data into a stream of CT items.

Besides, the pretrigger board fulfills the following specific procedures:

Check of synchronization between the data streams coming from different FEDs;

Suppression data with pointed 'VETO-BX' numbers coming from other pretriggers;

Data overflow protection - limitation the number of fired CTs with the same BX# which are being sent to the master card;

Counting average rate of CTs.

The pretrigger board block scheme is shown at fig.3. The numbers given on the picture are related to case when pretrigger board serves 96-pad rows. Every 48 ns three data packs, consists of 96-bit string of chamber's hits and 9-bit timing information each, are coming into a board in serial form. They are being accepted by fast link receivers (MC100SX1451 by Motorola) and arranged into parallel form. Bit-strings are being latched, masked to suppress noisy channels and tested for coincidences. 96-bit string of PT1 is filtered in the following way (illustrated at fig.2). Those bits which match to the coincidence algorithm remain fired, the other bits are cleared. If there is at least one fired road in processed data then the following information are loaded into the FIFO: filtered bit-string of PT1, bit-strings of the PT2 and PT3 as they are, and timing code BXnC. The described procedure can be executed by 7 PLD chips of MACH4 family or 4 PLD chips CYPRESS 7C388A. Two pipeline cycles are necessary to execute it.

BXnC code consists of 8 least significant bits of full Bunch crossing Number and the transmission Cycle bit. The last C-bit is necessary due to the following. Data are being taken from chambers into FEDs every bunch crossing - each 96ns. Two data transmission cycles can be done via optical links to the pretrigger logic during this time interval. C-bit is used as extension of BX# code to identify 1st and 2nd data transmission cycles. The BXnC codes received from chamber stations must be equal, and thus they are tested for equality. An error signal is generated in case of in-

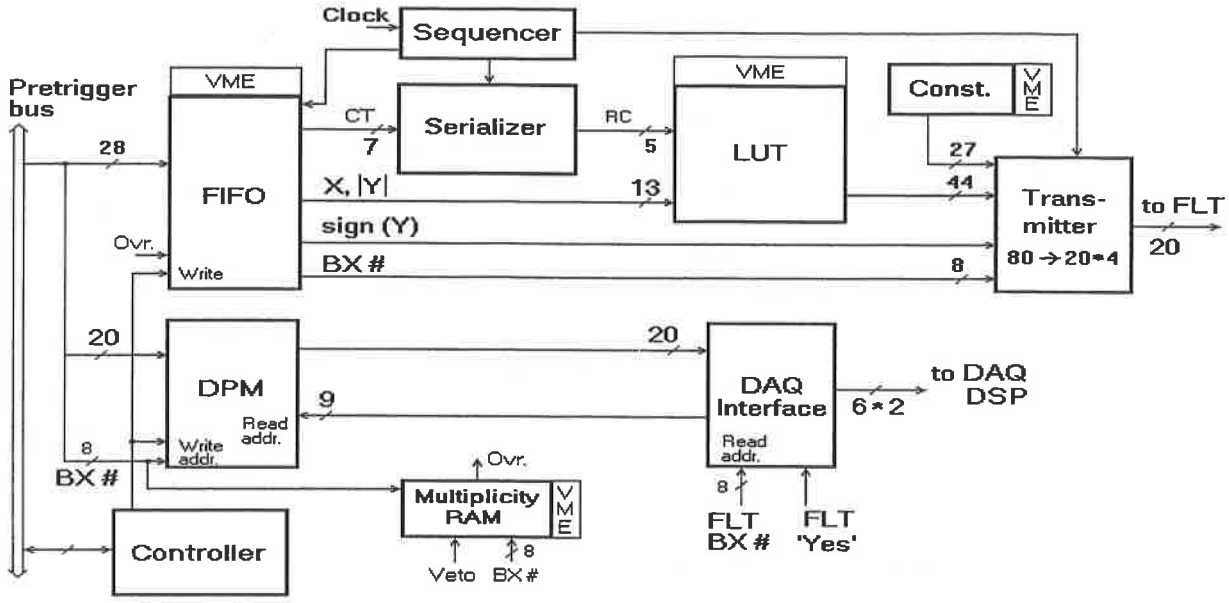

Figure 4: Schematic of a Master Card.

equality.

The next procedure implemented at the pretrigger board is an extraction the fired CTs from the selected data which are stored in the FIFO. Filtered PT1 hit-string is being loaded into priority encoder and tested to find fired bits. The positions of fired bits are consequently appeared at the output of encoder as 7-bit codes and used to retrieve 3 adjacent bits out of PT2 and 4 bits of PT3 bit-strings. This 7-bit code defines X-position (in the row) while board number together with transmission Cycle bit of BXnC code define Y-position (row) of fired pad in the PT1. These codes together with BXnC code are loaded into the output register to be read by the master card. The time needed for deriving one fired CT in this way is about 96 ns (one bunch crossing time). This time is short enough in respect to the average number of tracks which pass through one row of pads per bunch crossing. This number is expected to be less than 0.1 per bunch crossing and no pile-up is expected at pretrigger boards.

Output data overflow protection is implemented in a pretrigger board. The 'Multiplicity counter' counts fired CTs in the same event. It stops the CT finding procedure in case of this number exceeds the limit.

External 'VETO' signal represents the BX# of HERA-B event which must be rejected. In order to monitor the average rate of CTs generated by the pretrigger board, the 'Events counter' is used.

4.2 *Master Card*

A Master Card completes the pretrigger logic process and provides communication between group of pretrigger boards and appropriate FLT processors. It executes the following procedures:

Acquires data out of pretrigger boards;

Completes the serialization procedure - extracts roads out of the CTs using optimized algorithm;

Converts road's code into a set of track parameters;

Transmits messages to the appropriate FLT processors;

Distributes VETO-BX# among pretrigger boards;

Limits the number of track candidates with the same BX# is being sent to the FLT (overflow protection);

Besides, some additional facilities are foreseen at a master card:

Storage of acquired data for necessary time and transmission of data selected by the FLT to the DAQ.

Counting of track candidates.

Optimization of roads finding procedure means minimization the number of roads in fired CT which has several neighbour fired pads (see fig.2, CT #n1).

A master card consists of three parts (fig.4) working asynchronously. The first one ('Controller') acquires data out of pretrigger boards via the bus and loads data to the FIFO and DPM in parallel. 'Multiplicity RAM' counts CTs with the same BX#. It blocks FIFO input in case of overload. The 'Veto BX#' from other subdetectors can be easily implemented at a master card.

The 'messages generation' part defines roads in CT, converts them into tracks parameters and distributes messages among appropriate FLT processors. The row and pad numbers coming from pretrigger boards determine Y and X positions of track in the PT1 plane. The symmetry of chamber layers with respect to horizontal axis allows to reduce the addressing space of the Look-Up-Table (LUT) for one bit. Only 5 last bits out of 6 of Y-code are connected to the address inputs of the LUT (Look-Up Table). The 'Serializer' consequently derives roads from CT and generates road codes (RCs). According to the HERA-B FLT message format LUT transforms X,Y and RC codes into 45-bit code which includes initial track parameters. Some parameters in 80-bit message are constant and are being taken from register 'Const'. The 'Message transmitter' divides 80-bit message into four 20-bit words and transmits them to FLT processors.

The third part of a master card provides communication with the DAQ. Dual Ports Memory (DPM) realizes pipeline function, it keeps acquired data during 256 bunch crossings. BX# determines the data location in memory - both for loading data into and for reading data out in according with FLT request.

4.3 *Flexibility, testability*

The pretrigger logic is implemented in VME standard. Initialization procedure must be done to provide functionality of the pretrigger logic. Initialization of a pretrigger board includes loading mask codes into the PLDs and setting some other necessary codes. The Look-Up Table and some registers on a master card are to be initialized either. Reinitialization can be done at any time to update parameters.

There is either a facility to change coincidence algorithm by reprogramming PLDs at pretrigger boards and master cards. It allows to change basic coincidence scheme 1-3-2 to 1-4-2 or 1-5-2.

Facilities to test the pretrigger logic via VME bus are foreseen. Test data can be loaded into coincidence PLDs on a pretrigger board, the results of data processing can be retrieve out of FIFOs both at the pretrigger board and the master card.

4.4 *Prototype*

The first prototype of the pretrigger logic section has been designed and is being tested in Hamburg University. The pretrigger logic latency is 0.5 μs. In physics run '98 complete test of the prototype with real data is planned to check its performances and study high-p_T pretrigger.

References

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