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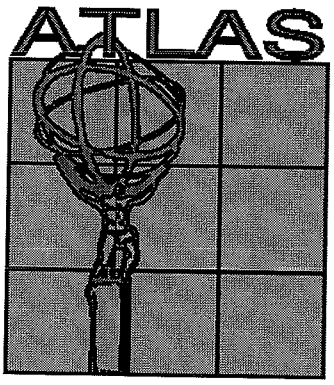
Tests of the SCT Front-end Chip of the ATLAS Detector at the Large Hadron Collider



Thesis for the degree of Master of Science in Physics

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Contents

abstract and acknowledgements to be written... maybe list of figures, and list of tables...

Chapter 1

Introduction

In 1994 the European Organization for Nuclear Research (CERN) approved the construction of the Large Hadron Collider (LHC), a new proton-proton (pp) collider with a center of mass energy of 14 TeV, which is planned to be operational in the year 2005.

Four experiments are currently planned for LHC. Two of them, ATLAS (A Toroidal LHC ApparatuS) and CMS are general purpose pp experiments and are designed to fully exploit the discovery potential of the LHC. The third experiment, LHC-B is dedicated to B-physics. While the fourth one, ALICE will explore heavy ion physics.

The ATLAS detector optimization is guided by physics issues such as sensitivity to the largest possible Higgs mass range. Other important goals are the investigation of CP violation in B-decays, the searches for heavy W- and Z-like objects, for supersymmetric particles, for compositeness of the fundamental fermions, as well as detailed studies of the top quark. The ability to cope well with a broad variety of possible physics processes is expected to maximize the detector's potential for the discovery of new, unexpected physics.

The ATLAS detector consists of several parts. These are the Inner Detector (ID), the different calorimeters (Hadronic Tile, EM Accordion, Forward LAr and Hadronic LAr End Cap Calorimeters), and the Muon Sectrometer. The work presented here concerns the readout of the Silicon Tracker (SCT) of the Inner Detector of ATLAS. As the detector will operate at very high luminosities (10^{34} $cm^{-2}\,s^{-1}$), this puts very serious demands on the performance of the detectors in LHC. In order to fully take advantage of the this high luminosity, new electronics systems have been developed. They must be reliable, accurate and efficient in order to survive in the SCT environement for several years. One of them is the ABCD readout chip. The aim of this paper is to present the tests performed on this chip, in order to see if its performance meets the requirements.

After this introduction chapter 1 will describe the ATLAS detector with emphasis on the ID. It will also introduce the basic elements of particle physics and the physics which will be studied in ATLAS, especially B-physics. Chapter 3 will concentrate on the Silicon Tracker (SCT) of the Inner Detector, its

structure, its modules. The design of the readout chip ABCD will be presented in chapter 4. Chapter 5 is devoted to the measurements carried out to test and better understand the ABCD chip. Finally, chapter 6 gives a conclusion to the work that has been done.

Chapter 2

Physics in ATLAS

2.1 Overview of the experimental apparatus

2.1.1 The Large Hadron Collider (LHC)

The Large Hadron Collider, which is being built at CERN, represents the next generation of colliders. It will be installed in the 27 km tunnel where the LEP collider is located, and should be operational in 2005. It will be a proton-proton collider capable of producing collisions with a total collision energy of 14 TeV and luminosity of 10^{34} $cm^{-2}\,s^{-1}$. The LHC will use the existing accelerators for the injection of the particles. Since the LHC will be colliding beams of particles with identical charge two separate beam-lines are necessary in order to allow the two proton beams to circulate in opposite directions. The frequency of bunch-crossing will be 40 MHz.

There will be 4 interaction points, and as many experiments. Two of them, ATLAS (A Toroidal LHC ApparatuS) and CMS are general purpose pp experiments and are designed to fully exploit the discovery potential of the LHC. The third experiment, LHC-B is dedicated to B-physics. While the fourth one, ALICE will explore heavy ion physics.

2.1.2 ATLAS

The ATLAS[1] Collaboration proposes to build a general-purpose pp detector which is designed to exploit the full discovery potential of the LHC.

The LHC offers a large range of physics opportunities, among which the origin of mass at the electroweak scale is a major focus of interest for ATLAS. The detector optimization is therefore guided by physics issues such as sensitivity to the largest possible Higgs mass range. Other important goals are the investigation of CP violation in B-decays, the searches for heavy W- and Z-like objects, for supersymmetric particles, for compositeness of the fundamental

[1] A Toroidal LHC ApparatuS

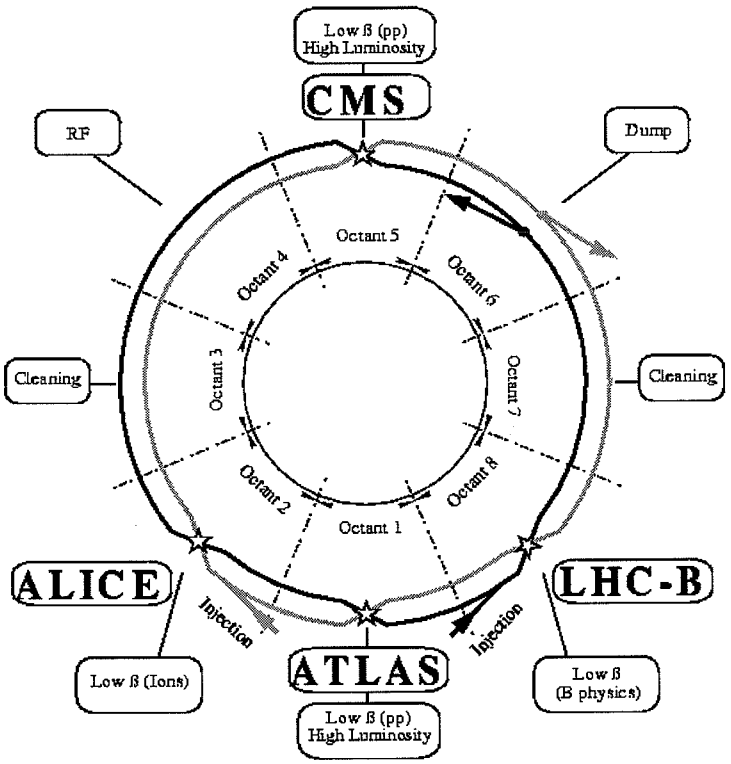


Figure 2.1: Experiments at the LHC

fermions, as well as detailed studies of the top quark. The ability to cope well with a broad variety of possible physics processes is expected to maximize the detector's potential for the discovery of new, unexpected physics.

Many of the interesting physics questions at the LHC require high luminosity, and so the primary goal is to operate at high luminosity (10^{34} cm^{-2} s^{-1}) with a detector that provides as many signatures as possible using electron, gamma, muon, jet, and missing transverse energy measurements, as well as b-quark tagging. The variety of signatures is considered to be important in the high-rate environment of the LHC in order to achieve robust and redundant physics measurements with the ability of internal cross-check.

Emphasis is also put on the performance necessary for the physics accessible during the initial lower luminosity running (10^{33} cm^{-2} s^{-1}), using more complex signatures such as tau-lepton detection and heavy-flavour tags from secondary vertices.

The overall layout of the detector is presented on fig. 2.2. It is approximately 35 m long and its radius is around 10 m. It consists of three sub-systems: muon spectrometer, calorimeters and the Inner Detector. The primary goal of the first one is to identify heavy quark events with prompt muon and produce a trigger essential for all heavy quark studies. The second will provide a good electromagnetic calorimetry for the identification and measurement of photons and electrons, and accurate jet and missing transverse energy measurements. The third sub-system is the theme of the next section.

2.1.3 The Inner Detector

The purpose of the Inner Detector is to make high-precision measurements of the kinematic parameters of charged tracks with maximum capability for pattern recognition, particle identification and triggering. In order to maximise the capability for resolving the inevitable ambiguities caused by overlapping tracks, secondary interactions and detector inefficiencies, it is desirable to make a large number of measurements along the track. A combination of high-precision "discrete" (i.e. few point) and low-precision "continuous" (i.e. many point) tracking will offer the best possible track finding and track fitting capabilities. The discrete tracking will be provided by the silicon pixel and strip detectors at radii close to the beam axis. Silicon strip detectors come in two configurations: barrel silicon tracker and forward silicon tracker. The difference between strips and pixels is mainly geometric, pixels being closely spaced pads capable of good two dimensional reconstruction, while strips give better spatial resolution in one coordinate than the other. Pixels are also more resistant concerning the radiation damage, so they are placed closer to the beam. The continuous tracking will be provided by straw drift tubes situated at higher radii. The Semiconductor Tracker will be described in greater detail in chapter 3.

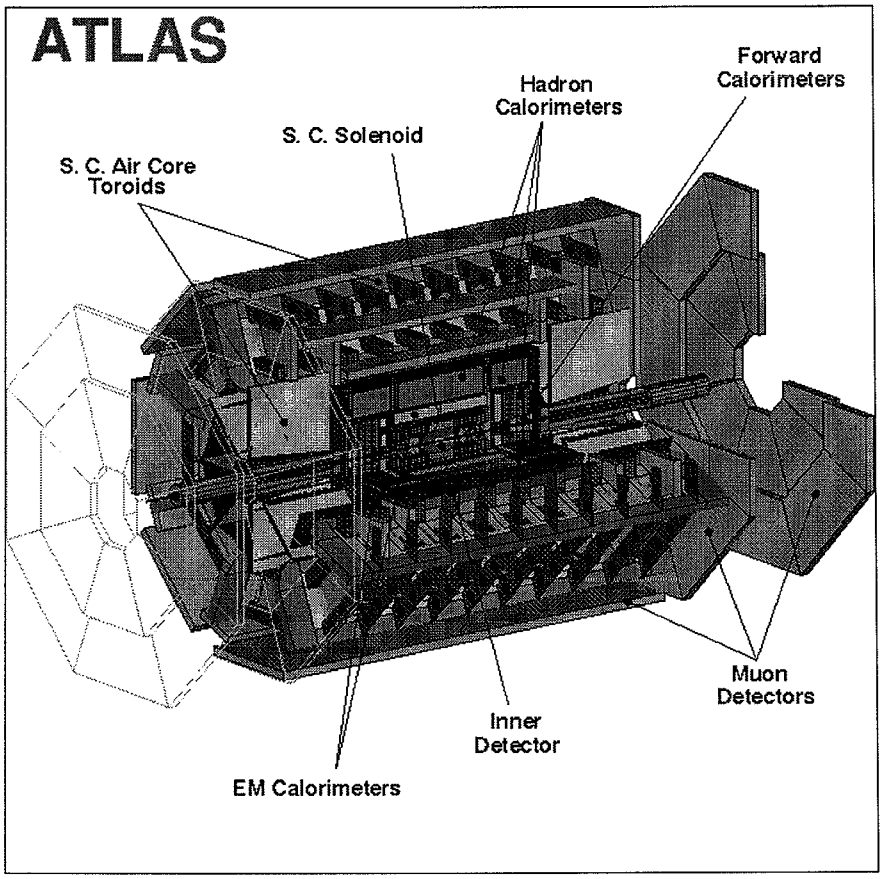


Figure 2.2: Cross-section of the ATLAS detector

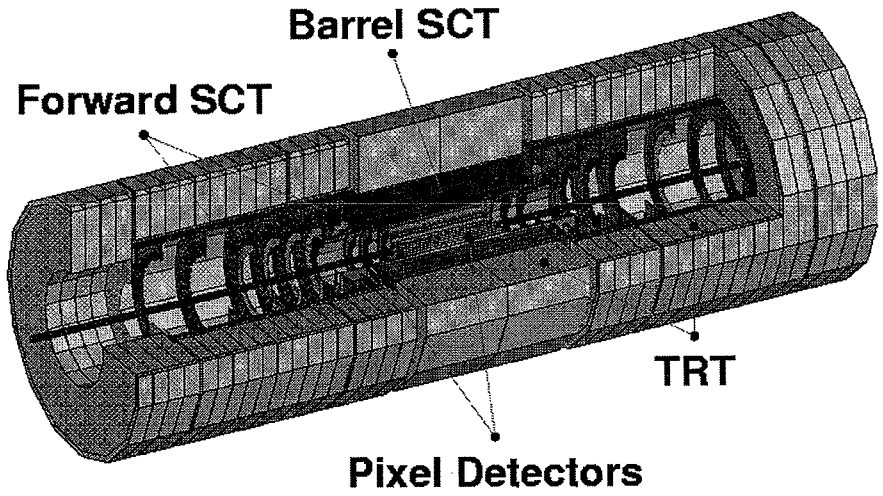


Figure 2.3: The Inner Detector of ATLAS (fig 1-i)

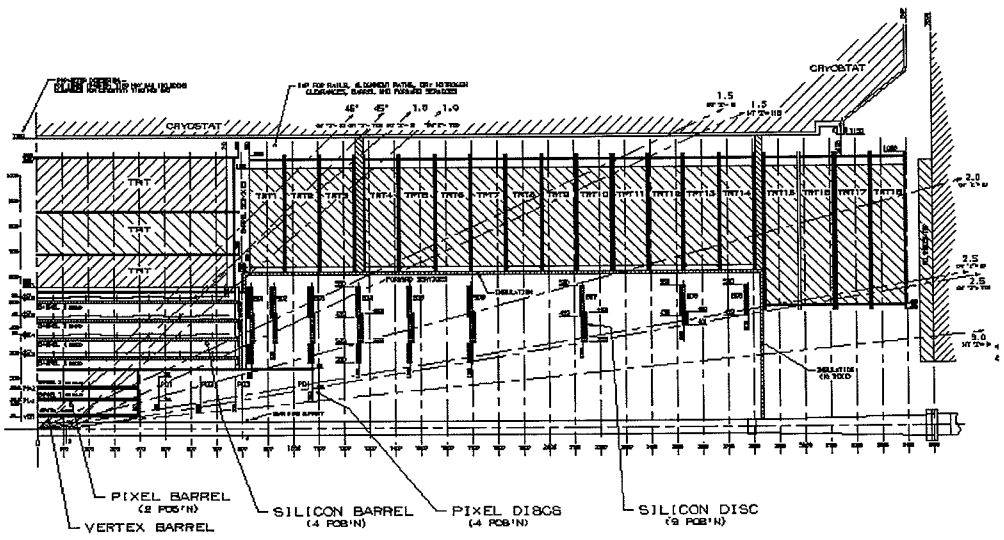


Figure 2.4: Cross section of the Inner Detector along the beam axis (fig1-1)

Quarks	d	u	s	c	b	t
Mass (GeV/c^2)	0.008	0.004	0.15	1.2	4.7	170
Charge	-1/3	+2/3	-1/3	+2/3	-1/3	+2/3
Leptons	e	ν_e	μ	ν_μ	τ	ν_τ
Mass	0.0005	0	0.105	0	1.8	0
Charge	-1	0	-1	0	-1	0

Table 2.1: Main properties of the fermions

2.2 Theoretical overview

2.2.1 The Standard Model

The experimental and theoretical developments of the last 50 years have led to the development of the Standard Model (SM) of particle physics. Since it is described in great detail in many textbooks, the discussion given here will be brief.

The most important concept of the modern fundamental physics is that of symmetry. Noether's theorem states that to every symmetry corresponds a conserved quantity. For example invariance under translations, time displacements, rotations and Lorentz transformations leads to the conservation of momentum, energy, and angular momentum. Apart from the discrete symmetries, like the ones just mentioned, there are also local gauge symmetries: the phase variation permitted by a local symmetry is reconciled by a field which is considered to be the mediator of interactions between matter particles. The Standard Model describes the fundamental particles and their interactions via three of the four known forces: electromagnetic, weak and strong. The gravity is negligeably small at particle level and is not described by the SM.

The SM has three types of particles:

- fermions which are the matter particles and have spin $\frac{1}{2}$
- bosons which represent the interactions between fermions and have spin 1
- Higgs-boson which is a consequence of the spontaneous symmetry breaking, and has spin 0

The main properties of the fermions are summarized in table 2.1

2.2.2 CP-violation

Not all symmetries are conserved by all interactions. The weak interactions are not invariant under the parity transformation P; the cleanest evidence for this is the fact that the antimuon emitted in pion decay

$$\pi^+ \rightarrow \mu^+ + \nu_\mu \tag{2.1}$$

Figure 2.5: Diagram responsible for $K^0 \leftrightarrow \overline{K}^0$ mixing

always is produced left-handed. Nor are the weak interactions invariant under C, for the charge-conjugated version of reaction 2.1 would be

$$\pi^- \rightarrow \mu^- + \overline{\nu}_\mu \tag{2.2}$$

with a left-handed muon, whereas in fact the muon is always produced with a right-handed helicity. However, combining the two operations gives a true picture: CP turns the left-handed anti-muon into a right-handed muon, which is exactly what is observed in nature. The parity transformation was replaced by CP as the one believed to be conserved.

As it turned out to be, once again the intuition was false. The contradiction of this belief came from the neutral K mesons. The K^0 , with strangeness +1, can turn into its antiparticle $\overline{K}_0$, strangeness -1

$$K^0 \leftrightarrow \overline{K}^0 \tag{2.3}$$

through a second-order weak interaction represented by the diagram in figure 2.5 [2]. As a result, the particles that are normally observed in the laboratory are not K^0 and $\overline{K}_0$, but rather some linear combination of the two. In particular, eigenstates of CP can be formed, as follows. Because the K's are pseudoscalars

$$P|K^0> = -|K^0>, \quad P|\overline{K}^0> = -|\overline{K}^0> \tag{2.4}$$

on the other hand, from

$$C|p> = |\overline{p}> \tag{2.5}$$

$$C|K^0> = |\overline{K}^0>, \quad C|\overline{K}^0> = |K^0> \tag{2.6}$$

Accordingly

$$CP|K^0> = -|\overline{K}^0>, \quad CP|\overline{K}^0> = -|K^0> \tag{2.7}$$

and hence the normalized eigenstates of CP are

$$|K_1> = (1/\sqrt{2})(|K^0> - |\overline{K}^0>) \quad and \quad |K_2> = (1/\sqrt{2})(|K^0> + |\overline{K}^0>) \tag{2.8}$$

with

$$CP|K_1> = |K_1> \quad and \quad CP|K_2> = -|K_2> \tag{2.9}$$

Assuming CP is conserved in the weak interactions, K_1 can only decay into a state with $CP = +1$, whereas K_2 must go to a state with $CP = -1$. Typically, neutral kaons decay into two or three pions. The two-pion configuration carries

[2] ????see griffiths

a parity of +1, and three pion system has $P = -1$; both have $C = +1$. So the K_1 decays into two pions (never three); K_2 decays into three pions (never two):

$$K_1 \to 2\pi, \quad K_2 \to 3\pi \tag{2.10}$$

Now, the 2π decay is much faster, because the energy released is greater. So if initially the beam consists of K^0's

$$|K^0 >= (1/\sqrt{2})(|K_1 > +|K_2 >) \tag{2.11}$$

the K_1 component will quickly decay away, and down the line the beam should contain only K_2's. Near the source there should be a lot of 2π events, but farther along only 3π decays are expected.

Experimentally the two lifetimes are

$$\tau_1 = 0.89 \times 10^{-10} sec \tag{2.12}$$

$$\tau_2 = 5.2 \times 10^{-8} sec \tag{2.13}$$

so the K_1 's are mostly decayed after a few centimeters, whereas the K_2's can travel many meters.

The neutral kaons provide a perfect experimental system for testing CP invariance. By using a sufficiently long beam, it is possible to produce an arbitrarily pure sample of the long-lived species. If at this point a 2π decay is observed, CP has been violated. Such an experiment was reported by Cronin and Fitch in 1964. At the end of a beam 57 feet long, they found 45 two-pion events in a total of 22700 decays. That's a tiny fraction, but unmistakable evidence of CP violation. Evidently the long-lived neutral kaon is not a perfect eigenstate of CP after all, but contains a small admixture of K_1:

$$|K_L >= \frac{1}{\sqrt{1+|\epsilon|^2}}(|K_2 > +\epsilon|K_1 >) \tag{2.14}$$

The coefficient ϵ is a measure of nature's departure from perfect CP invariance; experimentally its magnitude is about 2.3×10^{-3}.

2.2.3 The Cabibbo Angle

CP violation can be parametrised (though not explained) by means of a phase in the Cabbibo-Kobayashi-Maskawa (CKM) matrix. In the following the CKM formalism is introduced. Leptons and quarks participate in weak interactions through charged $V - A$ currents constructed from the following pairs of (left-handed) fermion states:

$$\begin{pmatrix} \nu_e \\ e^- \end{pmatrix}, \quad \begin{pmatrix} \nu_\mu \\ \mu^- \end{pmatrix}, \quad and \quad \begin{pmatrix} u \\ d \end{pmatrix} \tag{2.15}$$

All these charged currents couple with a universal coupling constant G. It is natural to extend this uiversality to embrace the doublet

$$\begin{pmatrix} c \\ s \end{pmatrix} \tag{2.16}$$

Figure 2.6: The decay $K^+ \to \mu^+\nu_\mu$ HAL12.16

formed from heavier quark states. However this cannot be quite correct. For instance, the decay $K^+ \to \mu^+\nu_\mu$ occurs, so there must be a weak current which couples a u to an $\overline{s}$ quark (see fig. 2.6). This contradicts the above scheme which only allows weak transition between $u \leftrightarrow d$ and $c \leftrightarrow s$.

Instead of introducing new couplings to accomodate observations like $K^+ \to \mu^+\nu_\mu$, it is more elegant to keep universality but modify the quark doublets. Assuming that the charged current couples "roated" quark states

$$\begin{pmatrix} u \\ d' \end{pmatrix}, \quad \begin{pmatrix} c \\ s' \end{pmatrix}, ..., \tag{2.17}$$

where

$$d' = d\cos\theta_c + s\sin\theta_c \tag{2.18}$$

$$s' = -d\sin\theta_c + s\cos\theta_c \tag{2.19}$$

This introduces an arbitrary parameter θ_c, the quark mixing angle, known as he Cabibbo angle. Cabibbo first introduced the doublet u,d' to account for the weak decays of strange particles. Indeed, the mixing of the d and s quark can be determined by comparing $\Delta S = 1$ and $\Delta S = 0$ decays. For example

$$\frac{\Gamma(K^+ \to \mu^+\nu_\mu)}{\Gamma(\pi^+ \to \mu^+\nu_\mu)} \sim \sin^2\theta_c \tag{2.20}$$

After taking into account the kinematic factors arising from the different particle masses, the data show that the $\Delta S = 1$ transiions are suppressed by a factor of about 20 as compared to the $\Delta S = 0$ transitions. This corresponds to a Cabibbo angle $\theta_c \approx 13^o$

So instead of the simplistic charged current now there are "Cabibbo favored" transitions (proportional to $\cos\theta_c$) and "Cabibbo suppressed" ones and similar diagrams for the charge-lowering transitions.

It is possible to summarize the above scheme as follows. The charged (or flavor-changing) current couples $u \leftrightarrow d'$ states or $c \leftrightarrow s'$ (left-handed) quark states, where d' and s' are orthogonal combinations of the physical (i.e., mass) eigensttates of quarks of definite flavor d, s:

$$\begin{pmatrix} d' \\ s' \end{pmatrix} = \begin{pmatrix} \cos\theta_c & \sin\theta_c \\ -\sin\theta_c & \cos\theta_c \end{pmatrix} \begin{pmatrix} d \\ s \end{pmatrix} \tag{2.21}$$

The quark mixing is described by a single parameter, the Cabibbo angle.

2.2.4 Generalization to three doublets

Now consider the generalization of the Cabibbo-GIM ideas to more than four quark flavors. Imagine for a moment that weak ineractions operate on N doublets of left-handed quarks,

$$\begin{pmatrix} u_i \\ d_i' \end{pmatrix} \quad with \;\; i = 1, 2, ..., N \tag{2.22}$$

where d_i' are mixtures of he mass eigenstates d_i:

$$d_i' = \sum_{j=1}^{N} U_{ij} d_j \tag{2.23}$$

U is a unitary $N \times N$ matrix to be determined by the flavor-changing weak process. How many observable parameters does U contain? We can change the phase of each of the $2N$ quark states independently without altering the physics. Therefore U contains

$$N^2 - (2N - 1) \tag{2.24}$$

real parameters. One phase is omitted as an overall phase change still leaves U invariant. On the other hand, an orthogonal $N \times N$ matrix has only $\frac{1}{2}N(N-1)$ real parameters. Therefore, by redefining the quark phases, itt is not possible, in general, to make U real. U must contain

$$N^2 - (2N - 1) - \frac{1}{2}N(N - 1) = \frac{1}{2}(N - 1)(N - 2) \tag{2.25}$$

residual phase factors. Thus, for wo doublets ($N = 2$), there is one real parameter (θ_c), whereas for three doublets, there are three real parameters and one phase factor, $e^{i\delta}$. This phase leading to an imaginary part of the CKM matrix is a necessary ingredient to describe CP violation within the framework of the Standard Model.

The matrix that connects the weak eigenstates (d', s', b') and the corresponding mass eigenstates d, s, b is

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{2.26}$$

Let us introduce the notation $c_{ij} = \cos\theta_{ij}$ and $s_{ij} = \sin\theta_{ij}$ with i and j being generation labels ($i, j = 1, 2, 3$). The standard parametrization is then given as follows [8]:

$$V = \begin{pmatrix} c_{12}c_{13} & s_{12}c_{13} & s_{13}e^{-i\delta} \\ -s_{12}c_{23} - c_{12}s_{23}s_{13}e^{i\delta} & c_{12}c_{23} - s_{12}s_{23}s_{13}e^{i\delta} & s_{23}c_{13} \\ s_{12}s_{23} - c_{12}c_{23}s_{13}e^{i\delta} & -s_{23}c_{12} - s_{12}c_{23}s_{13}e^{i\delta} & c_{23}c_{13} \end{pmatrix}, \tag{2.27}$$

where δ is the phase necessary for CP violation. c_{ij} and s_{ij} can all be chosen to be positive and δ may vary in the range $0 \leq \delta \leq 2\pi$. However, the measurements of CP violation in K decays force δ to be in the range $0 < \delta < \pi$.

The extensive phenomenology of the last years has shown that s_{13} and s_{23} are small numbers: $\mathcal{O}(10^{-3})$ and $\mathcal{O}(10^{-2})$, respectively. Consequently to an excellent accuracy $c_{13} = c_{23} = 1$ and the four independent parameters are given as

$$s_{12} = |V_{us}|, \quad s_{13} = |V_{ub}|, \quad s_{23} = |V_{cb}|, \quad \delta \tag{2.28}$$

with the phase δ extracted from CP violating transitions or loop processes sensitive to $|V_{td}|$. The latter fact is based on the observation that for $0 \leq \delta \leq \pi$, as required by the analysis of CP violation in the K system, there is a one–to–one correspondence between δ and $|V_{td}|$.

For numerical evaluations the use of the standard parametrization is strongly recommended. However once the four parameters in (2.28) have been determined it is often useful to make a change of basic parameters in order to see the structure of the result more transparently. This brings us to the Wolfenstein parametrization.

The original Wolfenstein parametrization is an approximate parametrization of the CKM matrix in which each element is expanded as a power series in the small parameter $\lambda = |V_{us}| = 0.22$,

$$V = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3(\varrho - i\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3(1 - \varrho - i\eta) & -A\lambda^2 & 1 \end{pmatrix} + \mathcal{O}(\lambda^4)\,, \tag{2.29}$$

and the set (2.28) is replaced by

$$\lambda, \qquad A, \qquad \varrho, \qquad \eta\,. \tag{2.30}$$

The Wolfenstein parameterization has several nice features. In particular it offers in conjunction with the unitarity triangle a very transparent geometrical representation of the structure of the CKM matrix and allows the derivation of several analytic results to be discussed below. This turns out to be very useful in the phenomenology of rare decays and of CP violation.

When using the Wolfenstein parametrization one should keep in mind that it is an approximation and that in certain situations neglecting $\mathcal{O}(\lambda^4)$ terms may give wrong results. The question then arises how to find $\mathcal{O}(\lambda^4)$ and higher order terms. The point is that since (2.29) is only an approximation the *exact* definiton of the parameters in (2.30) is not unique by terms of the neglected order $\mathcal{O}(\lambda^4)$. This is the reason why in different papers in the literature different $\mathcal{O}(\lambda^4)$ terms can be found. They simply correspond to different definitions of the parameters in (2.30). Obviously the physics does not depend on this choice. Here we will follow a definition which allows for simple relations between the parameters (2.28) and (2.30). This will also restore the unitarity of the CKM matrix which in the Wolfenstein parametrization as given in (2.29) is not satisfied exactly.

To this end we go back to (2.27) and we impose the relations

$$s_{12} = \lambda\,, \qquad s_{23} = A\lambda^2\,, \qquad s_{13}e^{-i\delta} = A\lambda^3(\varrho - i\eta) \tag{2.31}$$

to *all orders* in λ. It follows then that

$$\varrho = \frac{s_{13}}{s_{12}s_{23}}\cos\delta, \qquad \eta = \frac{s_{13}}{s_{12}s_{23}}\sin\delta. \tag{2.32}$$

We observe that (2.31) and (2.32) represent simply the change of variables from (2.28) to (2.30). Making this change of variables in the standard parametrization (2.27) we find the CKM matrix as a function of $(\lambda, A, \varrho, \eta)$ which satisfies unitarity exactly! We also note that in view of $c_{13} = 1 - \mathcal{O}(\lambda^6)$ the relations between s_{ij} and $|V_{ij}|$ in (2.28) are satisfied to high accuracy.

In order to improve the accuracy of the unitarity triangle discussed below one includes also the $\mathcal{O}(\lambda^5)$ correction to V_{td}. In summary then V_{us}, V_{cb}, V_{ub}, V_{td} and V_{ts} are given to an excellent approximation as follows:

$$V_{us} = \lambda, \qquad V_{cb} = A\lambda^2 \tag{2.33}$$

$$V_{ub} = A\lambda^3(\varrho - i\eta), \qquad V_{td} = A\lambda^3(1 - \bar{\varrho} - i\bar{\eta}) \tag{2.34}$$

$$V_{ts} = -A\lambda^2 + \frac{1}{2}A(1 - 2\varrho)\lambda^4 - i\eta A\lambda^4 \tag{2.35}$$

with

$$\bar{\varrho} = \varrho(1 - \frac{\lambda^2}{2}), \qquad \bar{\eta} = \eta(1 - \frac{\lambda^2}{2}). \tag{2.36}$$

The advantage of this generalization of the Wolfenstein parametrization over other generalizations found in the literature is the absence of relevant corrections to V_{us}, V_{cb} and V_{ub} and an elegant change in V_{td} which allows a simple generalization of the unitarity triangle.

2.2.5 The unitarity triangle

The unitarity of the CKM-matrix leads to the following set of equations:

$$|V_{ud}|^2 + |V_{cd}|^2 + |V_{td}|^2 = 1 \tag{2.37}$$
$$|V_{us}|^2 + |V_{cs}|^2 + |V_{ts}|^2 = 1 \tag{2.38}$$
$$|V_{ub}|^2 + |V_{cb}|^2 + |V_{tb}|^2 = 1 \tag{2.39}$$

$$|V_{ud}|^2 + |V_{us}|^2 + |V_{ub}|^2 = 1 \tag{2.40}$$
$$|V_{cd}|^2 + |V_{cs}|^2 + |V_{cb}|^2 = 1 \tag{2.41}$$
$$|V_{td}|^2 + |V_{ts}|^2 + |V_{tb}|^2 = 1 \tag{2.42}$$

$$V_{ud}V_{us}^* + V_{cd}V_{cs}^* + V_{td}V_{ts}^* = 0 \tag{2.43}$$
$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0 \tag{2.44}$$
$$V_{us}V_{ub}^* + V_{cs}V_{cb}^* + V_{ts}V_{tb}^* = 0 \tag{2.45}$$

$$V_{ud}V_{cd}^{*} + V_{us}V_{cs}^{*} + V_{ub}V_{cb}^{*} = 0 \quad (2.46)$$
$$V_{ud}V_{ld}^{*} + V_{us}V_{ls}^{*} + V_{ub}V_{lb}^{*} = 0 \quad (2.47)$$
$$V_{cd}V_{td}^{*} + V_{cs}V_{ts}^{*} + V_{cb}V_{tb}^{*} = 0. \quad (2.48)$$

Whereas (2.37)-(2.39) and (2.40)-(2.42) describe the normalization of the columns and rows of the CKM-matrix, respectively, (2.43)-(2.45) and (2.46)-(2.48) originate from the orthogonality of different columns and rows, respectively. The orthogonality relations (2.43)-(2.48) are of particular interest since they can be represented as six "unitarity" triangles in the complex plane . Note that the set of equations (2.37)-(2.48) is invariant under the CKM phase-transformations specified in (ref?? maybe explain it??). If one performs such transformations, the triangles corresponding to (2.43)-(2.48) are rotated in the complex plane. Since the angles and the sides (given by the moduli of the elements of the mixing matrix) in these triangles remain unchanged and do therefore not depend on the CKM-phase convention, these quantities are physical observables.

It can be shown that all six triangles have the same area which is related to the measure of CP violation $J_{\rm CP}$:

$$| J_{\rm CP} | = 2 \cdot A_{\Delta}, \quad (2.49)$$

where A_{Δ} denotes the area of the unitarity triangles.

Let us briefly analyze the shape of the six unitarity triangles by using the original Wolfenstein parametrization. Then we find that most of these triangles are very squashed ones, since the Wolfenstein-structure both of eqs. (2.43)-(2.45) and (2.46)-(2.48), respectively, is given as follows:

$$\mathcal{O}(\lambda) + \mathcal{O}(\lambda) + \mathcal{O}(\lambda^5) = 0 \quad (2.50)$$
$$\mathcal{O}(\lambda^3) + \mathcal{O}(\lambda^3) + \mathcal{O}(\lambda^3) = 0 \quad (2.51)$$
$$\mathcal{O}(\lambda^4) + \mathcal{O}(\lambda^2) + \mathcal{O}(\lambda^2) = 0. \quad (2.52)$$

Consequently, only in the unitarity triangles corresponding to (2.44) and (2.47), all three sides are of comparable magnitude ($\mathcal{O}(\lambda^3)$), while in those described by (2.43), (2.46) and (2.45), (2.48) one side is suppressed relative to the remaining ones by $\mathcal{O}(\lambda^4)$ and $\mathcal{O}(\lambda^2)$, respectively. The triangles related to (2.44) and (2.47) agree at the $\mathcal{O}(\lambda^3)$ level and differ only through $\mathcal{O}(\lambda^5)$ corrections. Neglecting the latter subleading contributions they describe *the* unitarity triangle that appears usually in the literature.

Let us next concentrate on the most interesting unitarity triangle described by

$$V_{ud}V_{ub}^{*} + V_{cd}V_{cb}^{*} + V_{td}V_{tb}^{*} = 0. \quad (2.53)$$

Phenomenologically this triangle is very interesting as it involves simultaneously the elements V_{ub}, V_{cb} and V_{td}.

In most analyses of the unitarity triangle present in the literature only terms $\mathcal{O}(\lambda^3)$ are kept in (2.53). It is, however, straightforward to include the next-to-leading $\mathcal{O}(\lambda^5)$ terms. We note first that

$$V_{cd}V_{cb}^{*} = -A\lambda^3 + \mathcal{O}(\lambda^7). \quad (2.54)$$

Thus to an excellent accuracy $V_{cd}V_{cb}^*$ is real with $|V_{cd}V_{cb}^*| - A\lambda^3$. Keeping $\mathcal{O}(\lambda^5)$ corrections and rescaling all terms in (2.53) by $A\lambda^3$ we find

$$\frac{1}{A\lambda^3}V_{ud}V_{ub}^* = \bar{\varrho} + i\bar{\eta}, \qquad \frac{1}{A\lambda^3}V_{td}V_{tb}^* = 1 - (\bar{\varrho} + i\bar{\eta}) \tag{2.55}$$

with $\bar{\varrho}$ and $\bar{\eta}$ defined in (2.36). Thus we can represent (2.53) as the unitarity triangle in the complex $(\bar{\varrho}, \bar{\eta})$ plane. This is shown in fig. 2.7. The length of the side CB which lies on the real axis equals unity when eq. (2.53) is rescaled by $V_{cd}V_{cb}^*$. We observe that beyond the leading order in λ the point A *does not* correspond to (ϱ, η) but to $(\bar{\varrho}, \bar{\eta})$. Clearly within 3% accuracy $\bar{\varrho} = \varrho$ and $\bar{\eta} = \eta$. Yet in the distant future the accuracy of experimental results and theoretical calculations may improve considerably so that the more accurate formulation will be appropriate.

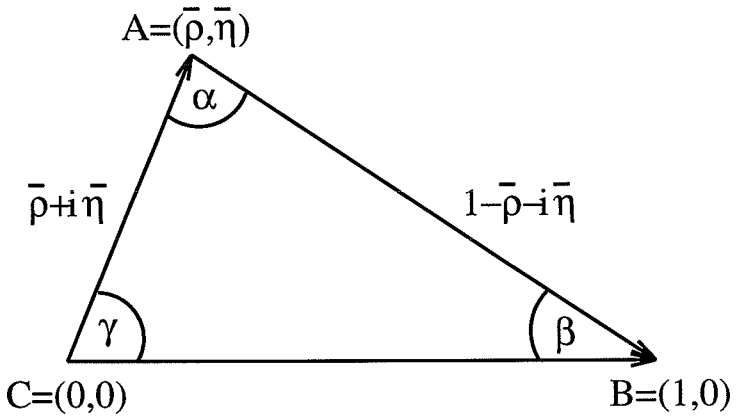


Figure 2.7: Unitarity Triangle.

For numerical calculations the following procedure for the construction of the unitarity triangle should be recommended:

- Use the standard parametrization in phenomenological applications to find s_{12}, s_{13}, s_{23} and δ.
- Translate to the set (λ, A, ϱ, η) using (2.31) and (2.32).
- Calculate $\bar{\varrho}$ and $\bar{\eta}$ using (2.36).

Using simple trigonometry one can express $\sin(2\phi_i)$, $\phi_i = \alpha, \beta, \gamma$, in terms of $(\bar{\varrho}, \bar{\eta})$ as follows:

$$\sin(2\alpha) = \frac{2\bar{\eta}(\bar{\eta}^2 + \bar{\varrho}^2 - \bar{\varrho})}{(\bar{\varrho}^2 + \bar{\eta}^2)((1-\bar{\varrho})^2 + \bar{\eta}^2)} \tag{2.56}$$

$$\sin(2\beta) = \frac{2\bar{\eta}(1-\bar{\varrho})}{(1-\bar{\varrho})^2 + \bar{\eta}^2} \tag{2.57}$$

$$\sin(2\gamma) = \frac{2\bar{\varrho}\bar{\eta}}{\bar{\varrho}^2 + \bar{\eta}^2} = \frac{2\varrho\eta}{\varrho^2 + \eta^2}. \tag{2.58}$$

The lengths CA and BA in the rescaled triangle of fig. 12 to be denoted by R_b and R_t, respectively, are given by

$$R_b \equiv \frac{|V_{ud}V_{ub}^*|}{|V_{cd}V_{cb}^*|} = \sqrt{\bar{\varrho}^2 + \bar{\eta}^2} = (1 - \frac{\lambda^2}{2})\frac{1}{\lambda}\left|\frac{V_{ub}}{V_{cb}}\right| \tag{2.59}$$

$$R_t \equiv \frac{|V_{td}V_{tb}^*|}{|V_{cd}V_{cb}^*|} = \sqrt{(1-\bar{\varrho})^2 + \bar{\eta}^2} = \frac{1}{\lambda}\left|\frac{V_{td}}{V_{cb}}\right|. \tag{2.60}$$

The expressions for R_b and R_t given here in terms of $(\bar{\varrho}, \bar{\eta})$ are excellent approximations. Clearly R_b and R_t can also be determined by measuring two of the angles ϕ_i:

$$R_b = \frac{\sin(\beta)}{\sin(\alpha)} = \frac{\sin(\alpha+\gamma)}{\sin(\alpha)} = \frac{\sin(\beta)}{\sin(\gamma+\beta)} \tag{2.61}$$

$$R_t = \frac{\sin(\gamma)}{\sin(\alpha)} = \frac{\sin(\alpha+\beta)}{\sin(\alpha)} = \frac{\sin(\gamma)}{\sin(\gamma+\beta)}. \tag{2.62}$$

The angles β and γ of the unitarity triangle are related directly to the complex phases of the CKM-elements V_{td} and V_{ub}, respectively, through

$$V_{td} = |V_{td}|e^{-i\beta}, \quad V_{ub} = |V_{ub}|e^{-i\gamma}. \tag{2.63}$$

The angle α can be obtained through the relation

$$\alpha + \beta + \gamma = 180^\circ \tag{2.64}$$

expressing the unitarity of the CKM-matrix.

The triangle depicted in fig. 12 together with $|V_{us}|$ and $|V_{cb}|$ gives a full description of the CKM matrix. Looking at the expressions for R_b and R_t, we observe that within the Standard Model the measurements of four CP *conserving* decays sensitive to $|\ V_{us}\ |$, $|\ V_{ub}\ |$, $|\ V_{cb}\ |$ and $|\ V_{td}\ |$ can tell us whether CP violation ($\eta \neq 0$) is predicted in the Standard Model. This is a very remarkable property of the Kobayashi-Maskawa picture of CP violation: quark mixing and CP violation are closely related to each other.

There is of course the very important question whether the KM picture of CP violation is correct and more generally whether the Standard Model offers a correct description of weak decays of hadrons. In order to answer these important questions it is essential to calculate as many branching ratios as possible, measure them experimentally and check whether they all can be described by the same set of the parameters $(\lambda, A, \varrho, \eta)$. In the language of the unitarity triangle this means that the various curves in the $(\bar{\varrho}, \bar{\eta})$ plane extracted from different decays should cross each other at a single point. Moreover the angles (α, β, γ) in the resulting triangle should agree with those extracted one day from CP-asymmetries in B-decays.

2.3 B physics in ATLAS

An important chapter of LHC physics will be the study of heavy-quark systems. In fact, already at initial lower luminosities the LHC will be a high-rate beauty- and top-quark factory. A particularly rich field will be available in B-physics, the main emphasis being on the precise measurement of CP-violation in the B_d^0 system and the determination of the angles in the Cabibbo-Kobayashi-Maskawa unitarity triangle. In addition, investigations of $B\overline{B}$ mixing in the B_s^0 system, rare B decays, and general spectroscopy of states with b-quarks will be of great interest. The goal of the ATLAS Collaboration to address also these physics topics has had an important impact on the detector design. Precise secondary vertex determination, full reconstruction of final states with relatively low-p_T particles, an example being $B_d^0 \to J/\psi K_S^0$ followed by $J/\psi \to \ell^+\ell^-$ and $K_S^0 \to \pi^+\pi^-$, and low-p_T lepton first-level trigger thresholds as well as second-level track triggering capability are all necessary requirements for the experiment.

2.3.1 *CP*-violation in ATLAS

The neutral kaon system discussed in section??? is the only evidence of the *CP*-violation that was measured up till now, so scientists were looking for another ecxperiment that would confirm it. They were seeking also for a bigger effect than that of 2.3×10^{-3} of the neutral kaon system. In fact, the Standard Model predicts a much bigger effect in the case of B-mesons. Of course, to produce B-mesons one has to have a much bigger energy, because of the large mass of the *b*-quark, and that's where the Large Hadron Collider comes into the picture. With the LHC it will be possible to reach energies, that have never been reached before resulting in a very high number of *b*-quarks. The ATLAS Collaboration aims to perform a wide programme of B-physics studies. These include the search for and measurement of CP-violation through the decays $B_d^0 \to J/\psi K_S^0$, $B_d^0 \to \pi^+\pi^-$, and $B_s^0 \to J/\psi\phi$. Other topics are the measurement of B_s^0 mixing, searches for rare decays such as $B_d^0 \to \mu^+\mu^-$, $B_s^0 \to \mu^+\mu^-$, the study of B-baryon decay dynamics, and spectroscopy of rare B hadrons.

B-physics studies will be experimentally easiest at the initial luminosity $\mathcal{L} \approx 10^{33}\ \mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, where pile-up effects are small and vertex detectors very close to the beam pipe are expected to survive for several years. Much of the B physics will thus be performed during the first few years of LHC operation. It is assumed in the ATLAS Technical Proposal that the total $b\overline{b}$ production cross-section is $\sim 500\ \mu$b.

Strong features of the ATLAS detector for the B-physics programme are a powerful and flexible trigger system, high-resolution secondary-vertex measurement, and efficient track reconstruction and electron identification down to low p_T. These have been studied in detail using full simulation of the inner detector and applying global pattern-recognition, bremsstrahlung-recovery and vertex-fitting algorithms (see for example a $B_d^0 \to J/\psi K_S^0$ simulation on figure 2.8).

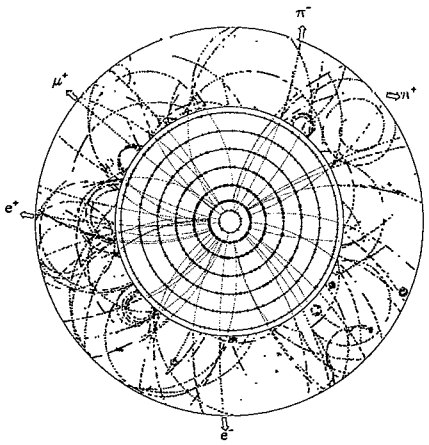


Figure 2.8: $B_d^0 \to J/\psi K_S^0$ event display at the inner detector

Figure 2.9: $B_d^0 \to J/\psi K_S^0$ decay (tagging...)

$B_d^0 \to J/\psi K_S^0$ decays

The decay mode $B_d^0 \to J/\psi K_S^0$ is a clean channel for measuring $\sin 2\beta$, where β is one of the angles in the unitarity triangle. The reconstructed B meson is tagged as having been produced as a B_d^0 or a $\bar{B}_d^0$ using the charge of the accompanying 'tag' muon (see fig. 2.9), which is assumed to come from the semileptonic decay of the other b-quark in the event.

In the decay mode $B_d^0 \to J/\psi K_S^0$, the quark subprocess is dominated by the single tree-level transition $b \to c\bar{c}s$. The time-dependent decay rates of B_d^0, $\bar{B}_d^0 \to J/\psi K_S^0$ are [3]

$$N(B_d^0(t) \to J/\psi K_S^0) \propto \exp^{-\Gamma t}(1 - \sin 2\beta \sin \Delta m t)$$
$$N(\bar{B}_d^0(t) \to J/\psi K_S^0) \propto \exp^{-\Gamma t}(1 + \sin 2\beta \sin \Delta m t) \qquad (2.65)$$

where $\Gamma = 1/\tau$ is the average of the widths Γ_1 and Γ_2 of the B-meson mass eigenstates, Δm is the mass difference between the eigenstates, and β is one of the angles of the unitarity triangle. The asymmetry in the decay $B_d^0 \to J/\psi K_S^0$, when integrating starting from time t_0, is:

$$A = \frac{N(B_d^0 \to J/\psi K_S^0) - N(\bar{B}_d^0 \to J\psi/K_S^0)}{N(B_d^0 \to J/\psi K_S^0) + N(\bar{B}_d^0 \to J\psi/K_S^0)}$$
$$= 1/(1 + x_d^2) \sin 2\beta (\sin \Delta m t_0 + x_d \cos \Delta m t_0)$$
$$= D_{int} \sin 2\beta \qquad (2.66)$$

The factor multiplying $\sin 2\beta$ comes from the time-integration. For $t_0 = 0$, $D_{int} = x_d/(1+x_d) = 0.47$, with $x_d = \Delta m/\Gamma \approx 0.69 \pm 0.07$ [6]. The observed asymmetry is

$$A^{obs} = \frac{N_{total}(J/\psi K_S^0 l^+) - N_{total}(J/\psi K_S^0 l^-)}{N_{total}(J/\psi K_S^0 l^+) + N_{total}(J/\psi K_S^0 l^-)}$$
$$\simeq D_{tag} D_{back}(D_{int} \sin 2\beta + A^p) \quad (2.67)$$

where A^p is the production asymmetry of B_d^0 and $\overline{B}_d^0$, estimated to be at the percent level [4].The statistical significance of the signal is reduced by wrong-sign tags ($D_{tag} = 1 - 2W$, where W is the fraction of wrong-sign tags over the total number of tags). Wrong assignements of the tag-lepton are caused by

1. cascade decays of the b
2. $B^0 - \overline{B}^0$ mixing
3. additional c- and b-quarks created in the parton shower
4. hadron background
5. top decays

They are dominated by cascade decays and mixing. Fig. 2.10 illustrates the wrong-tag fraction as a function of the transverse-momentum threshold of the trigger muon. With the $p_T > 6$ *GeV* used at ATLAS $D_{tag} = 0.52$. $D_{\rm back} = N_{\rm S}/N_{\rm total}$ is the dilution factor from background, where $N_{\rm S}$ and $N_{\rm total}$ are the number of signal events and the total number of events respectively; the background is assumed to be asymmetry-free.

Reconstruction of $K_S^0 \to \pi^+\pi^-$ decays has been studied using a full detector simulation [2]. The K_S^0 mass resolution was in the range 3–8 MeV for transverse decay lengths of 1–50 cm, depending on the K_S^0 decay position. The average efficiency was 91% and the background under the K_S^0 peak was 6% at $\mathcal{L} = \infty \cdot 10^{33}\ {\rm cm}^{-2}\,{\rm s}^{-1}$. At $\mathcal{L} = \bigtriangledown \cdot 10^{33}\ {\rm cm}^{-2}\,{\rm s}^{-1}$, the efficiency was 88% while the background rose to 11%.

The signal and background analyses were performed using a particle-level simulation [5]. The signal search started from the J/ψ reconstruction. For μ-tagged $J/\psi \to e^+e^-$ decays, a tag muon with $p_{\rm T} > 6$ GeV and $|\eta| < 2.2$, and two electrons with $p_{\rm T} > 1$ GeV were required. For μ-tagged $J/\psi \to \mu^+\mu^-$ decays, a tag muon with $p_{\rm T} > 5$ GeV, and two other muons with $p_{\rm T}(\mu^1) > 5$ GeV, $p_{\rm T}(\mu^2) > 3$ GeV were required; in addition, one of the three muons was required to satisfy the trigger, having $p_{\rm T} > 6$ GeV, $|\eta| < 2.2$. For electron-tagged $J/\psi \to \mu^+\mu^-$ events, a tag electron with $p_{\rm T} > 5$ GeV, and two muons with $p_{\rm T}(\mu^1) > 6$ GeV, $|\eta(\mu^1)| < 2.2$, and $p_{\rm T}(\mu^2) > 3$ GeV were required.

The distance of closest approach between the two lepton candidates forming the J/ψ was required to be < 100 μm. The distance of the J/ψ decay vertex from the primary vertex in the transverse plane was required to be > 250 μm.

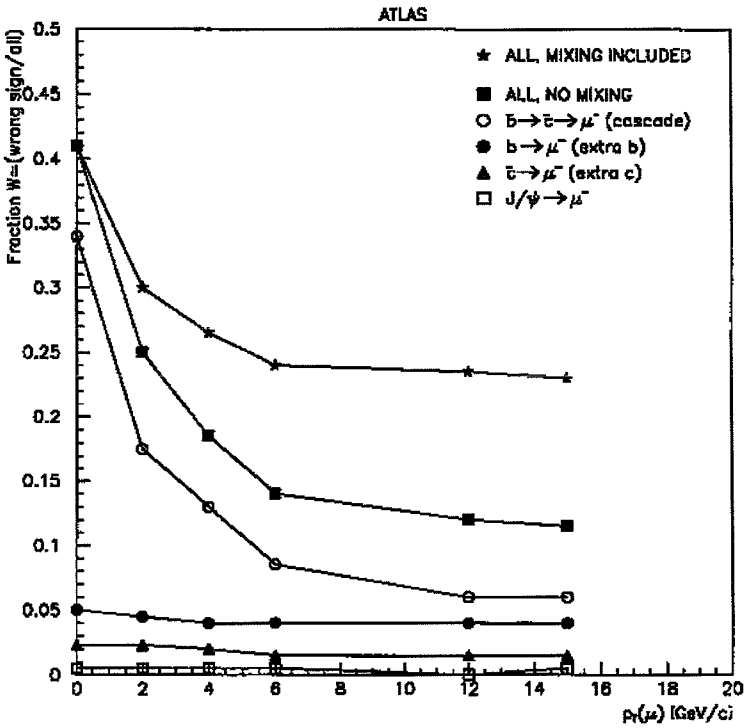


Figure 2.10: The sources of wrong-sign trigger muons and their fractions, as a function of the trigger threshold

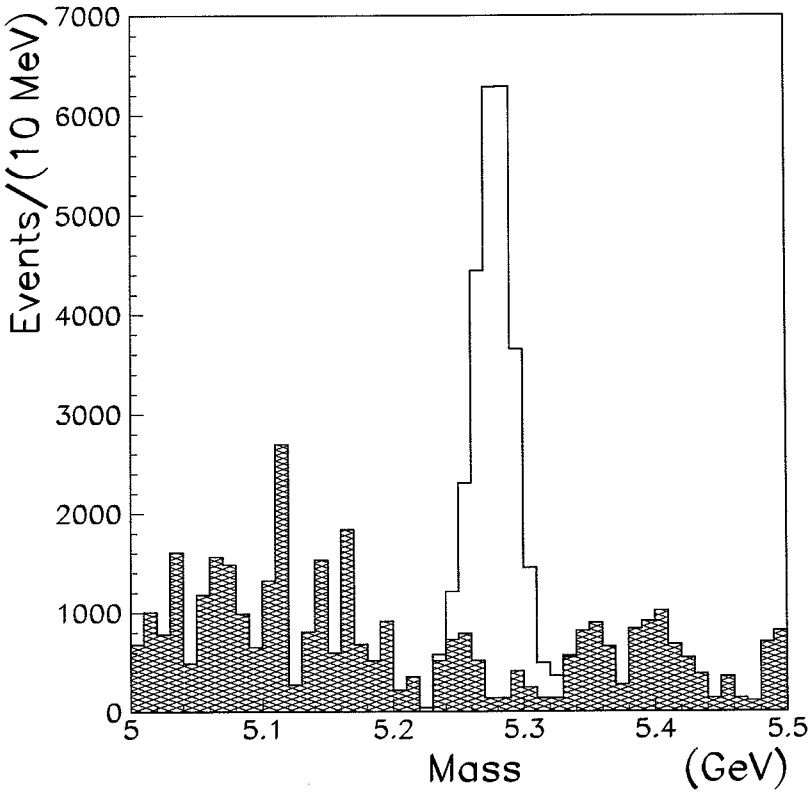


Figure 2.11: Reconstructed ($J/\psi K^0_S$) mass. The white histogram shows the signal and the hatched histogram shows the background.

In the $\mu^+\mu^-$ channel, the reconstructed J/ψ mass was required to be within two standard deviations of the nominal one. In the e^+e^- channel, the mass window was [-400,+200] MeV around the J/ψ mass. After the above cuts, the fake-J/ψ fraction was $\sim$ 45% in the μ-tagged $\mu^+\mu^-$ channel, 95% in the μ-tagged e^+e^- channel, and 24% in the electron-tagged $\mu^+\mu^-$ channel.

Finally, the J/ψ and the K^0_S candidates were used to search for the B^0_d. The proper time of the B decay, measured from the distance of the J/ψ decay vertex from the primary vertex in the transverse plane, and from the reconstructed p_T of the B, was required to be > 0.5 ps. Such a cut on the proper time corresponds to $D_{int} = 0.63$. Constraining the K^0_S and the J/ψ masses to their nominal values, a B^0_d mass resolution of 16 MeV was obtained. The reconstructed $J/\psi K^0_S$ mass distributions for the signal and background are shown in Fig. 2.11 after all the cuts except for the final two-standard-deviation cut on

the reconstructed B_d^0 mass. The dominant background comes from a real J/ψ from a B decay combined with a K_S^0 from the fragmentation. Fake J/ψ's and K_S^0's were also included in the background estimate. Cuts on the decay length of the J/ψ candidate suppress background from real J/ψ coming directly from hadronization.

The value of $\sin 2\beta$ was obtained from a fit to the proper time distributions for the positive and negative tags. The statistical precision for $\sin 2\beta$, including the effect of the secondary-vertex resolution, was $\delta(\sin 2\beta) = 0.018$.

Theoretical uncertainties in the measurement of $\sin 2\beta$ via the decay channel $J/\psi K_S^0$ are expected to be less than 1%. The experimental sources of systematic error can be controlled with comparable accuracy. The background is relatively small and dominated by accidental background with a rather flat mass distribution.

$B_d^0 \to \pi^+\pi^-$ decays

The CP-asymmetry in the decay mode $B_d^0 \to \pi^+\pi^-$ is sensitive to the angle α in the unitarity triangle. The branching fraction of this decay has not yet been measured, and was assumed to be $2 \cdot 10^{-5}$.

The largest experimental uncertainties in this decay mode are due to the background. Systematic errors may arise from uncertainties in the branching fractions and shapes of mass distributions of the B decays which constitute the background, since it is possible that not all these decays will have been studied before the LHC becomes operational.

In spite of the large systematic uncertainties associated with the measurement of $\sin 2\alpha$, it will be interesting to establish CP-violation in the $B_d^0 \to \pi^+\pi^-$ channel, and a measurement of the asymmetry will constrain the CP-violation parameters.

$B_s^0 \to J/\psi\phi$ decays

The decay $B_s^0 \to J/\psi\phi$ is related to the third angle γ of the unitarity triangle. The CP-asymmetry is, however, suppressed by a small factor D_{CKM} and the maximum asymmetry is expected to be only $\sim 3\%$ in the Standard Model. A large observed asymmetry would thus be an indication of new physics.

Chapter 3

The Semiconductor Tracker (SCT)

The SCT is a sub-detector of the ATLAS Inner Detector (ID). The SCT works with the other elements of the ID, the Transition Radiation Tracker (TRT) and the Pixel Tracker to provide the necessary tracking functions to meet the performance requirements discussed in the previous chapter. The SCT is based upon silicon microstrip detector technology, which has been used with success over the past 8 years in experiments at LEP and at the Fermilab Tevatron. Consequently there is substantial experience in the high energy physics community with the construction and operation of these devices.

The ATLAS SCT aims to operate reliably according to performance specifications over a 10-year period of high luminosity LHC operation. The design LHC luminosity aims for an average peak value of $10^{34}\ cm^{-2}s^{-2}$ over 10^{7} secs per year, giving an annual integrated luminosity of $10^{41}\ cm^{-2}$. Instantaneous rates may exceed this value. These luminosities are achieved using bunch-bunch crossings separated by 25 nsec (40 MHz) to result in a particle interaction rate 10^{9} Hz.

The SCT radial envelope is defined internally by the tolerance of silicon sensors and their electronics to charged and neutral radiation, and externally by the TRT, to an active radius $r < 52\ cm$ in the barrel region and $r < 56\ cm$ for the forward silicon disks. Silicon has been chosen as the detector medium because of its fast signal speed, and excellent spatial segmentation.

The layout consists of 4 'central' barrel layers in the radial range $30 < R < 52\ cm$, and 9 disks in each of the forward and backward directions in the radial range $26 < R < 56\ cm$.

In the barrel region, each layer consists of silicon strip modules of 4 single-sided silicon detectors with active area 61.6 x 62.0 mm^2, and geometric area 63.6 x 64.0 mm^2. Within the module , two detectors are daisy-chained for each side of a module . On one side 768 strips of 80 μm pitch and active length 123.2 mm are aligned precisely along the beam direction. The back-side detector pair

Figure 3.1: p^+n binary detectors, the effective bulk doping changes from n- to p type after irradiation(strip width 22um, pitch80 um, tthickness 300 um)

is identical, but rotated by 40 *mrad*, to provide a z-measurement capability. The use of small-angle stereo rather than orthogonal strips is motivated by the need to reduce the number of ghost hits near a real track in high-multiplicity events. A second motivation is to retain an $r - \phi$ measurement capability in the case of detector inefficiencies. In order to minimise the signal spread during operation in a 2 Tesla solenoidal field, the modules are mounted at an angle of 10^o to the tangent. Modules are overlapped in a tile arrangement to minimise dead areas in the barrel region. The silicon detector signals will be read out by binary front-end electronics. Within the barrel region, all detectors have the same pitch, and all modules are identical.

In the forward direction, the geometrical layout no longer allows the use of identical detector designs; nevertheless, the module construction is similar. Modules of daisy-chained singel-sided detectorpairs with strip length $\approx 12\ cm$ and mean pitch $\approx 80\ \mu m$, are arranged back-to-back with a 40 *mrad* stereo orientation.

The technical solutions for the SCT consist of a choice of silicon detector design and technology, a choice of front-end, readout, and monitoring electronics, a detector module design, a data transmission and cabling technology, a mounting scheme, and a cooling system.

3.0.2 Detectors

The principal structure of the option chosen for ATLAS is shown on Figure 3.1

The effects of heavy particle irradiation on silicon detectors include an increase in leakage current, a change in effective doping [1], and a decrease in charge collection efficiency. The change in effective doping implies a change in the voltage necessary to deplete the detector and for detectors which are built on n-type bulk, the doping change will result in an effective type inversion. Projections for the SCT after 10 years of operation indicate depletion voltages of up to $\approx 450\ V$ and type inversion for all sensors. Significant uncertainities exist which may imply even higher voltages.

By constructing n-in-n detectors (n+ strips on an n-type substrate) it has been demonstrated that efficient partially depleted operation is possible after type inversion, with fast signal collection and limited charge diffusion. Because of the consequent safety margin, single-sided n-in-n sensors have been chosen. The detectors will be AC-coupled, and will be negativ-biaised from the backside to maintain only a small voltage across the capacitor oxide.

[1] The radiation gives rise to the creation of deep level acceptor type defects.

3.0.3 Electronics

The front end electronics is based upon a one-bit digital (binary) readout architecture. This choice is supported by test-beam and bench prototype studies, and is the most cost-effective implementation meeting the performance requirements. Any strip that collects charge above an externally adjustable threshold fires a per strip discriminator. The binary output is stored in a pipeline until an ATLAS trigger initiates readout for the beam crossing. A consequence for this architecture is significant data reduction in the front end chips, meaning that the discriminator performance, thresholds, noise, and pickup must be well controlled.

The hybrid design uses a thick film technology on a Berillium Oxide (BeO) substrate. The substrate choice is motivated by the high thermal conductivity and long radiation length of this material.

An optical communication scheme is chosen, because of its low mass and lack of electrical pick-up. It is required, however, to be radiation resistant. Each pair of hybrids is connected to a pair of light-diode (LED) drivers which share the output data. In case of failure, one driver can be used for the pair. The clock and control data are received optically by a PIN diode near the hybrid. The SCT cable design for low voltages and detector bias uses a thin aluminium on kapton technology. This is chosen to minimise mass while maintaining an acceptable voltage drop.

Power supplies for the SCT are segmented to provide self contained low and high voltage channel separately to each module . This minimises pick-up and potential ground loops. High impedance DC connections are included to prevent excessive baseline drift between components.

3.0.4 Modules

A module is the basic readout unit of the SCT. The module layout is described in the next section. Two pairs of daisy-chained detectors are glued back-to-back with one pair rotated by 40 mrad. The readout of 12-cm strips was motivated by cost, while maintaining adequate signal-to-noise (S/N) performance. To minimise the effect of strip resistance and fan-out capacitance on the S/N, a 'centre-tapped $r-\phi$' design, where the front end IC's are bonded at the middle of the module, is chosen for the barrel. Mechanical assembly is more complex for the forward modules, and an 'end tapped' design is chose, at the expense of a modest increase in noise.

Cooling considerations significantly constrain the module design. In order to avoid the thermal runaway of damaged silicon detectors , a thermal base board is required to increase the effective in-plane thermal conductivity. There must also be good thermal contact to the cooling pipes.

3.1 Modules

3.1.1 Introduction

A module is the basic functional sub-unit of the ATLAS SCT. It consists of a set of single sided silicon mocro-strip detectors glued back to back, an electronics package (the 'hybrid') and an interface to the cooling and mechanical support structure of the tracker.

There are four main issues which arise from the requirements of the SCT and LHC operating environment and affect significantly the design of the module . The first issue concerns the general event topology at the LHC and affects the division of the tracker into a barrel and forward region. The second issue concerns tracking performance and translates into constraints on the mechanical precision and stability of the module and its electrical performance. The third issue concerns radiation levels and the thermal design of the module . This is because radiation effects are strongly temperature dependent. The fourth issue concerns the effect of material within the module on the performance of the tracker and the other outside elements of the ATLAS detector. This leads to serious constraints on materials to be used in the construction of modules .

3.1.2 Event topology

For the event configurations at LHC, the requirements of rapidity coverage ($|\eta| < 2.5$) and an effective use of silicon area lead naturally to a division of the tracker into a central barrel region and a forward disk region. Effective overlap along z and a minimization of dead regions leads to a barrel module configuration with the hybrid electronics package mounted over the active region of the silicon , rather than off the end as was common in small vertex detectors . The physical limitations of available silicon leads to a barrel module length of 12.8 cm. In the forward region, the natural disk geometry and a restriction of the length of a module to around 12 cm or less leads to the concept of using three rings of detectors to provide the necessary radial coverage. The forward modules are supported at the outer end which is then the natural location of the hybrid.

3.1.3 Tracking

The precision that will be achieved is determined by the readout pitch of the strip detectors , by the assembly and survey precision of the module , and the tilt angle and mounting and survey precision of the module on the support structure. The mechanical tolerance for positioning wafers within the back-to-back pair must be $\approx 5\ \mu m$ in lateral strip position, 25 μm in module thickness, and 25 μm in z.

The forward region measures the longitudinal momentum and the track dip angle. The requirements are very similar to the barrel after allowing for interchange of r and z.

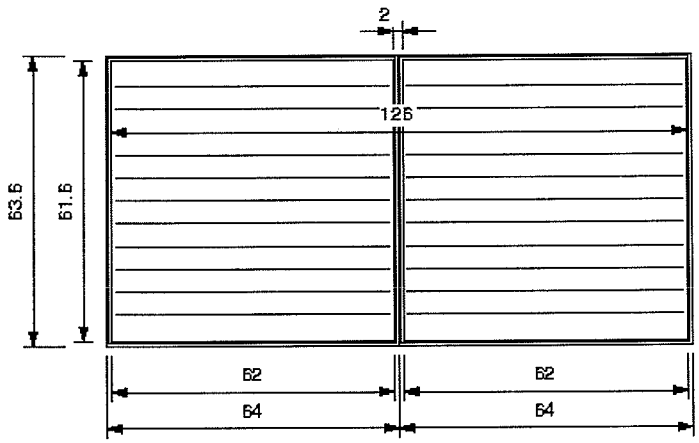


Figure 3.2: Geometry of barrel module detectors (11-50)

For pattern recognition, noise occupancy must be kept low. Electronic noise analysis for the shaping times used in SCT show that a centre tapped configuration will have the minimum noise contribution from the series resistance of the readout strip. The improvement over an end tapped configuration is about 150 electrons.

Within the SCT structure the barrel modules are intrinsically suitable to benefit from the centre-tap scheme, while in the forward region other considerations become relevant. In particular, the radial dependance of the background radiation enhances the need to place active electronic components at the largest possible radii, and hence makes an end-tap readout more attractive.

3.1.4 Mechanical configuration

In the barrel region, one module is made of four 6.4 cm x 6.36 cm single-sided silicon microstrip detectors . Geometrical dimensions are shown in Figure 3.2 for two detectors butt joined to form a 12.8 cm long mechanical unit. Strips of two of the detectors are electrically connected to form 12.6 cm long active strips. The detectors will be positioned to have a 2 mm gap at their join. In order to form a double-sided readout module , two 12.8 cm long mechanical units are back-to-back aligned and glued with a stereo angle of 40 mrad. One side of the module measures the $r-\phi$ coordinates ('axial strips') while the other side measures the 40 mrad rotated coordinate (the 'stereo strips'). The pitch of the strips is 80 μm and there are 768 readout strips.

In the forward region, each module is formed from two measuring planes. In the first plane, the azimuthal angle, ϕ, is measured directly via strips of a radial geometry in which the strip pitch varies along the module length. The

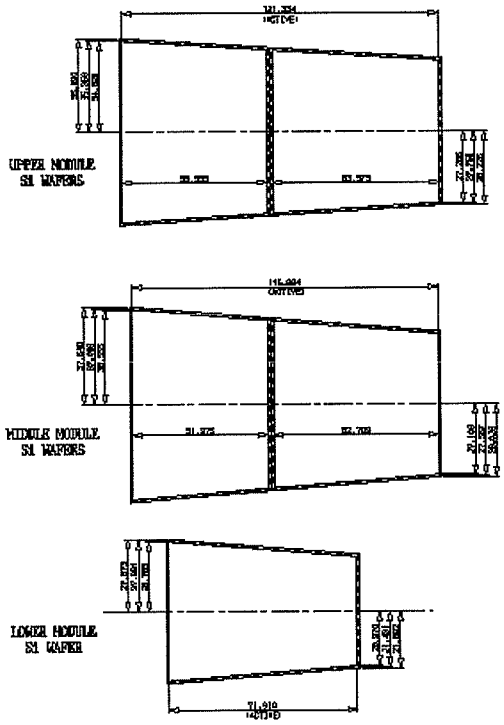


Figure 3.3: Geometry of forward silicon detectors (11-51)

second measuring plane, identical to the ϕ plane, is mounted such that there is a 40 mrad rotation with respect to the ϕ plane. The second plane provides a measure of the radial position of a particle when used in conjunction with the ϕ plane.

There are 770 strips per measuring plane, with the first and the last being used for field shaping and not connected to the readout. Each module subtends an angle larger than that required, to allow for a reasonable number of overlapping strips to ensure hermicity and to facilitate module-to-module alignement using physics tracks. The nominal ϕ angle of a module is covered by strips 10 to 759 where strips 0 and 770 are the field shaping strips. Figure 3.3 shows a schematic of the wafer dimensions and relative positioning for each of the three module types used in the forward region. Each wheel is covered by one to three rings depending on its z position in the tracker.

The outer ring is covered by 52 modules and has an active strip length of 121.1 mm formed from two wafers butted end-to-end. The outer ring module subtends an angle of 7.117 degrees to allow for overlaps. The rotation point for the u/v stereo plane is at the intersection of the wafer break and the module centre-line.

The middle ring, covered by 40 modules is, with the exception of those modules on wheel 8, also formed from two butt-joined wafers and as an active length of 116.7 mm. The middle ring modules on wheel 8 are formed from the upper wafer only and consequently have an active length of 52 mm. Middle ring modules subtend an angle of 9.252 degrees and the rotation point for the u/v plane is at the intersection of the wafer break and the module centre-line.

The inner ring is covered by 40 modules , each having an active strip length of 72 mm formed from a single wafer, subtending an angle of 9.252 degrees.

3.1.5 The barrel module

Figure 3.4 is a schematic of the barrel module showing the key features in the design. Figure 3.5 shows an expanded view of all the components. The measuring planes, each formed of a pair of wafers, are glued to a central beryllia baseboard and a pyrolytic graphite (TPG) heat spreader. The composite baseboard serves as a mechanical support for the wafers and increases the thermal conductivity in the plane of the module . Beryllia has been chosen for the hybrid baseboard frame due to its mechanical rigidity, its high thermal conductivity and long radiation length. The TPG, with a thermal conductivity of 1100 W/mK, significantly increases the in-plane thermal conductivity of the module .

3.1.6 The forward module

Figure 3.6 is a schematic of the forward middle ring module showing the key features in the design. Figure 3.7 is an expanded view of the forward module . The two measuring planes, each formed of a pair of wafers, are sandwiched around a double sided readout hybrid and a central spine. The spine serves as a mechanical support for the wafers and increases the thermal conductivity along

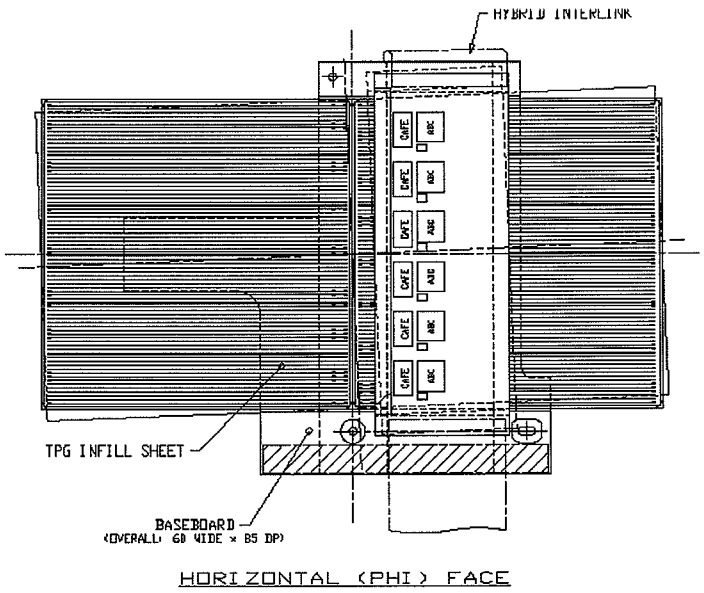


Figure 3.4: Configuration of the barrel module (11-52)

the length of the module . The same double sided hybrid is used for all modules and is formed on a support board into which two slots have been made. The slots act as a thermal break to prevent heat from the front-end electronics from entering into the silicon wafers. The electrical connections from the silicon strips to the readout electronics are made via fan-in structures mounted on either side of the hybrid bridging the thermal break.

The front-end electronics chip-sets are separated into two groups by the primary cooling contact which also serves as the module mounting point. Additional cooling may be provided by a contact to the far end of the spine.

3.2 Readout electronics

3.2.1 Introduction

The SCT readout electronics is responsible for supplying strip hit information to the ATLAS second level trigger and the data acquisition system. No information will be supplied to the first level trigger. The nature of silicon micro-strip detectors necessitates that the front-end electronics be mounted immediately at the silicon strip electrodes to ensure the low noise operation required. The electronics , therefore, must be in the active volume of the detector. This dictates that front-end electronics must be of low mass. Since heat removal requires material, low power consumption is required. The electronics must also

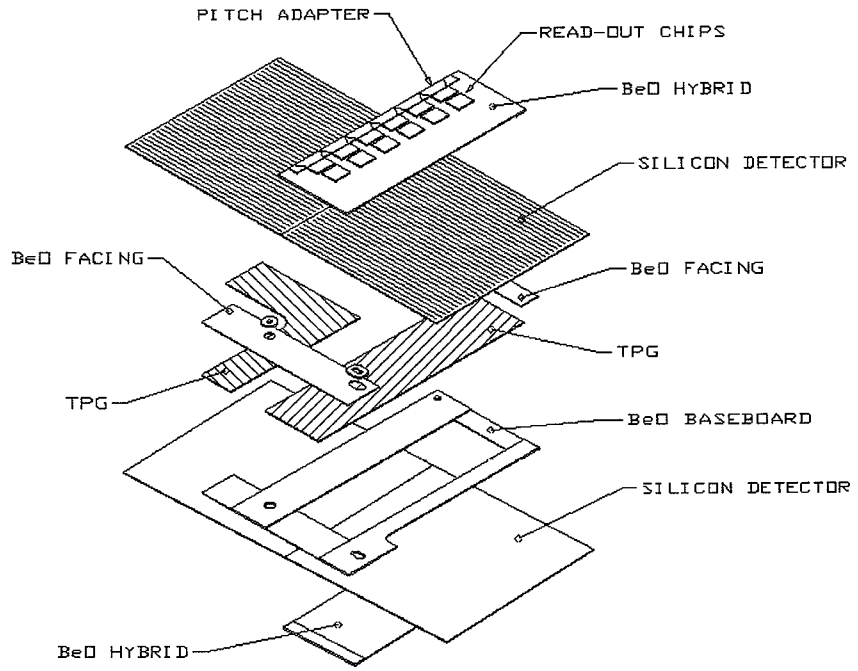


Figure 3.5: Expanded view of barrel module (11-53)

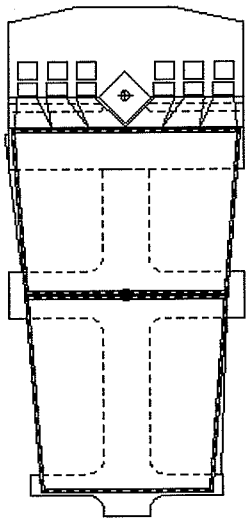


Figure 3.6: Forward module layout (11-55)

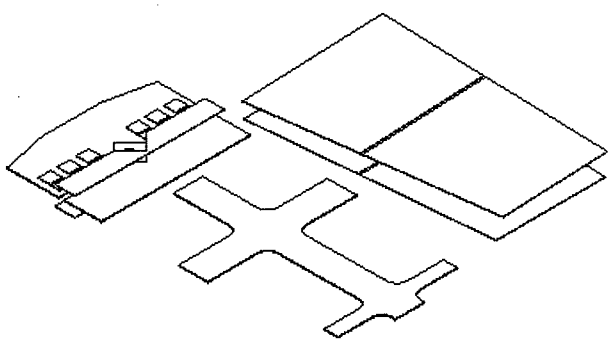


Figure 3.7: Expanded view of a forward module (11-56)

control the operation of the SCT, provide the necessary power for the electronics and detector bias, provide means for calibration and provide monitors of all aspects of the SCT operation.

The LHC operating conditions also present several challenges to the electronics for the SCT. The most obvious is the radiaton environment. The beam bunch crossing rate of 40 MHz and the high luminosity result in expected occupancies in the SCT up to 0.6 % every 25 ns caused by real tracks. In order to simplify track reconstruction, it is important to associate each hit to a specific beam crossing. The limit on noise hits has been set so as make them a negligible addition to the expected occupancy.

The combination of occupancy and crossing frequency also dictate the bandwidth needed to transmit the data off the detector. In order to minimise material and cost, data compression is required on the detector and the readout architecture is event driven. That is, data is only transmitted off detector in response to a Level 1 Accept signal for a specific beam crossing. Data is held in on-detectorbuffers for the duration of the Level 1 latency ($< 2.5\ \mu s$) waiting for the decision to transmit the data or discard it.

Another aspect of the SCT which greatly affects the electronics design is its inaccessibility. To minimise the need for repair access, the system is designed to be highly reliable, with redundancy where possible and a small loss of data from any single failure where is not. The electronics are also designed to provide sufficient monitors and modularity of controls so that problems can be detected and corrective action taken before extensive damage is done to the SCT.

3.2.2 System design

The front end electronics include all the integrated circuits and other components that are mounted onto hybrid assemblies which become part of each detector module . These ICs perform the initial amplification of signals, discrimination, pipeline buffering, data compression and formatting data for transmission. Diagnostic and test capability is provided in the front end ICs (such as variable charge injection into front end pre-amps) but these are kept to a minimum to keep chip size and power to minimum.

Data links transmit the data off detector. Other links transmit clock and control signals to the detector. The system is highly distributed with individual links going to each module. This multiplicity matches the necessary bandwidth with a highly parallel architecture to enhance the reliability of the SCT. Standard commercial links are not practical for this application, therefore the design employs 40 MHz links developed specifically for this application.

The cable system provides all power and DC control signals to (and from) the detector modules from power supplies located off the detector. Individual cable paths are provided for each detector module . Segmenting the power distribution to each module offers a more robust system in that any single failure will disable only a small fraction of the SCT. It allows silicon bias to be adjusted for variations in radiation dose and monitoring of currents and control of voltages to each module . Inside the detector volume, the cables are made of

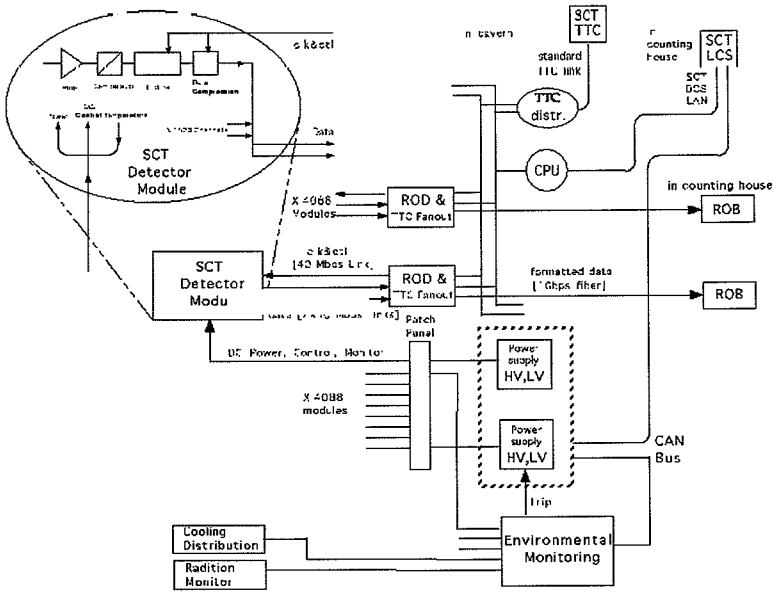


Figure 3.8: Schematic of SCT Electronics sub-systems (11-33)

low mass aluminium on Kapton. Outside the detector they are of conventional twisted pair construction.

The off detector readout and control system is the interface between the SCT detector modules and the ATLAS Data Acquisition (DAQ) Sasytem and the ATLAS Trigger, Timing and Control (TTC) System. There are two main functional blocks; The Readout Driver (ROD) and the SCT-TTC distribution. The RODs reeive data from the detector modules, interpret the SCT protocol, monitor for errors, reformat, buffer the data and feed it to the ATLAS standard Readout Buffers (ROB). The SCT-TTC interfaces to the ATLAS standard TTC. It receives clock and control information from the TTC, decodes the subset required, reformats and distributes it to the SCT-TTC links using the SCT protocol.

3.2.3 Specification

- Noise: The front end system must provide a sufficient signal-to-noise ratio to ensure a good efficiency and low noise occupancy. The equivalent noise charge (ENC) for the front end system is defined including the silicon strip detector parameters. The ENC defined this way is substantially larger than the pure electronic requirement on a single front end channel.

- Occupancy due to noise: The noise occupancy is required to be significantly less than the real hit occupancy to ensure that the noise hit rate

does not affect the data transmission rate or track reconstruction. A noise occupancy of $5x10^{-4}$ requires that the discrimination level in the front end electronics is set to 3.3 times the rms noise.

- Timing resolution: To minimise the data to be read out and to simplify tracking, unique crossing identification is required. The silicon charge collection time of 10 ns then mandates edge-sensing discriminators, with a maximum time walk of 16 ns for the nominal threshold setting and full range of input signals. The fraction of outputs shifted to the wrong beam crossing is required to be less than 1 %.

- Double pulse resolution: In an edge sensing system, double pulse resolution affects efficiency. It is required to be 50 ns to ensure $< 1\%$ data loss at the highest design occupancies.

- Large charge recovery time: A low rate of events resulting in large charge deposition due to slow particles is expected. Therefore, although not very critical, it is desirable that the recovery time after large overloads is limited.

- Trigger: The front end electronics operates at an average trigger rate of 100 kHz. The ATLAS requirement is for a 75 kHz trigger rate upgraded to 100 kHz, but because of its highly integrated nature, the full SCT electronics chain is designed for 100 kHz. The minimum spacing between consecutive triggers is 2 bunch crossings; statistical variations in trigger arrival beyond this must introduce $< 1\%$ data losses for 1% occupancy. This drives the specification for the bandwidth of data links and the depth of the derandomising buffer.

- Pipeline length: The pipeline length must correspond to the maximum trigger latency specified by the trigger system. With contingency, this is 3.2 μs which corresponds to 128 locations of the pipeline.

- Voltage compliance: Significant voltage drops along the power distribution cables are incurred to reduce the amount of material in the sensitive area of the tracker. This requires the front end electronics to be insensitive to a bias voltage variation of $+-5\%$ of the nominal values.

- Temperature: The electronics must operate without recalibration within $+-2.5^{o}C$ of its nominal value. In order to allow testing at room temperature it is required that overall readout system has full functionality in the temperature range between $-15^{o}C$ and $30^{o}C$.

- Power consumption: The actual power consumption is estimated to be between 3.0 mW and 3.2 mW per channel, including the optical interface.

- Radiation: The total radiation levels are specified separately for the displacement damage as a fluence of 1 MeV equivalent neutrons and for ionising radiation as a dose absorbed in SiO_2.

The chosen architecture is 'binary', in which the signal from the silicon strip is amplified, shaped and discriminated yielding only hit/no-hit information for each bunch crossing. The next chapter will describe more in detail this chip in order to better understand the experimental results presented in the last part of this paper.

Chapter 4

Description of the ABCD front-end chip

4.1 Introduction

One of the most important parts of the modules that form the silicon tracker is the front-end electronics. Currently there are two kinds of front-end chips under study:

1. CAFE-M + ABC, where CAFE-M is an analogue chip which performs the task of amplification and discrimination of the signal, while ABC manages the control of the readout

2. ABCD incorporates both tasks (amplification-discrimination and readout control) in a single chip

Both ideas have their advantages and disadvantages. Having two separate chips helps to avoid the interference of the digital and analogue part of the signal processing. On the other side, having one chip saves place, material, simplifies production. In the collaboration Geneva University-CERN the ABCD front-end chip was chosen to be studied. All the measurements presented later in this paper were carried out on these chips. In this chapter an overview of the design of the ABCD is presented in order to better understand the results described in the following chapter.

The ABCD chip designed for the DMILL techology comprises all functions required for the binary readout architecture in a single chip. The functionality of the ABCD chip is fully compatible with the other technological option considered for the ATLAS SCT front-end ASIC[1], although the circuit implementations of various functional blocks in the ABCD design are different. The ABCD design is based upon the SCT128B prototype chip, i.e. the analogue front-end,

[1]Application specific Integrated Circuit

the binary pipeline and the readout buffer is implemented in the ABCD design with some minor modifications. The back-end readout and control blocks use mostly the same circuit implementations as in the ABC design.

The chip must provide all functions required for processing of signal from 128 strips of a silicon strip detector in the ATLAS experiment employing the binary readout architecture. The chip must contain the following functions:

- Charge integration
- Pulse shaping
- Threshold discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage either from internal programmable DAC or from an external source.
- The outputs of the discriminators must be latched either in the edge sensing mode or in the level sensing mode.
- At the start of each clock cycle the chip must sample the outputs from the discriminators and store these values in a pipeline until a decision can be made whether to keep the data.
- Upon receipt of a Level 1 trigger signal the corresponding set of values together with its neighbours are to be copied into the readout buffer serving as a derandomizing buffer.
- The data written into the readout buffer is to be compressed before being transmitted off the chip.
- Transmission of data from the chip will be by means of token passing and must be compatible with the ATLAS protocol.
- The chip is required to provide reporting of some of the errors that occur

  a) Attempt to readout data from the chip when no data is available

  b) Readout Buffer Overflow: the readout buffer is full and data from the oldest event/s has been overwritten.

  c) Readout Buffer Error: the readout buffer is no longer able to keep track of the data held in it (chip reset required).

  d) Configuration error (ChipID sent).

- The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure.
- It is a system requirement that the fraction of data which is lost due to the readout buffer on the chip is being full is less than 1 % . This assumes that on the average only 1 % of the silicon strip detectors are hit during any particular beam crossing.

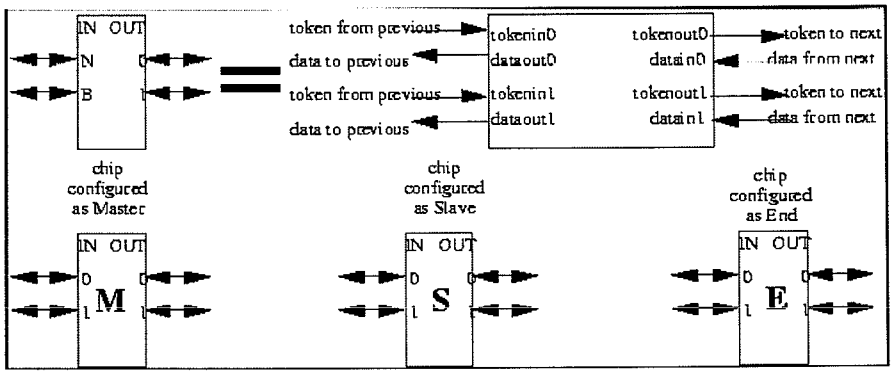


Figure 4.1: Key to symbols used in the following diagrams (3.17a)

The gain at the discriminator output should be 160 mV/fC for nominal shaper current of 15 μA and the nominal process parameters. The maximum rms noise must be < 1400 electrons for unirradiated module, and < 1500 electrons for an irradiated one. The timewalk should not exceed 16 ns [2].

Each channel will have an internal calibration capacitor connected to its input for purposes of simulating a hit strip. The calibration capacitors will be charged by a chopper circuit which is triggered by an independent differential input Calibration Strobe (CALSP, CALSN) [3]. Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). These strobe and selection signals are delivered from the control circuitry. The voltage applied to the calibration capacitors by the chopper is determined by an internal DAC. The four calibration bus lines, each of which connects the calibration capacitors of every fourth cahnnel, are also brought out to pads which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods must be provided.

4.1.1 Data readout and Redundancy

The figure 4.2 shows the data and token interconnections on a typical silicon detector module. The module has 6 ABCD chips on each side (see section 3.1.5). Two of these chips are configured as masters and control the readout of the data from the corresponding side of the module. Their LED outputs are connected to a fibre-optic interface. On the diagrams the master chips are denoted by an "M" and all the other chips are configured to act as slaves as denoted by "S", or "E" for a slave that acts also as an end chip.

[2]The timewalk is the maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC.

[3]See the pinout of the ABCD chip in appendix .1

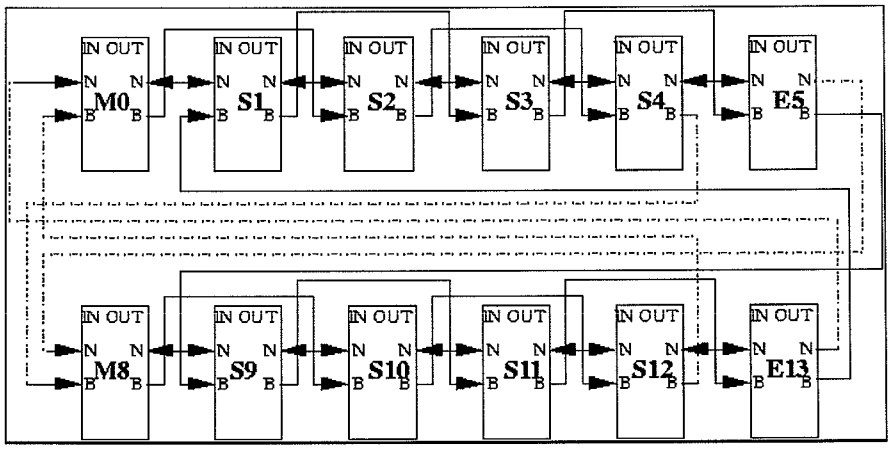


Figure 4.2: Interconnection of ABCD chips on a silicon detector module (3.17b)

After the receipt of a Level 1 Trigger, the master chip initiates a readout cycle by sending the preamble bits at the start of each data block to the LED driver. It then appends its data bits to the output stream sent to the LED driver. A few clock cycles before the last bit has been sent, it sends a token to the slave chip on its right. The slave chip on the right responds by sending its data packet to the master which in turn is appended to the preamble and data bits from the master already sent to the LED driver [4].

Once this slave has finished sending its data, it passes on the token to the next chip on the right. The next chip on the right passes its data to the previous chip on the left which in turn passes it back to the Master chip for transmission to the LED driver. This process continues until the last chip in the chain has sent its data.

A bit is set in the last chip in the chain to inform it that it is the last chip. When this chip has sent its data, it appends a trailer to the end of the data stream. While the master chip is outputting data, it is constantly looking for the trailer pattern which has been carefully chosen to be distinct from the data. Once it finds the trailer pattern, it knows that all the data from the event has been sent and it can start processing the next event (fig. 4.3).

In the event of the failure of one of the slave chips (fig. 4.4), the previous and next slave chips in the chain are programmed to route their data and tokens around the failed chip. Should the last chip in the chain fail, the penultimate chip in the chain will be programmed to perform the operation of the end chip.

When one of the master chips fails, the data and tokens from the chain with the failed master chip are routed to the working master chip as showed on fig. 4.5. Chip E5 has to be reconfigured to set it as a normal slave instead of

[4]Each chip always sends at least 3 bits of data even if it hasn't found any hit channels in the event being read out (No Hit Data Packet <001>).

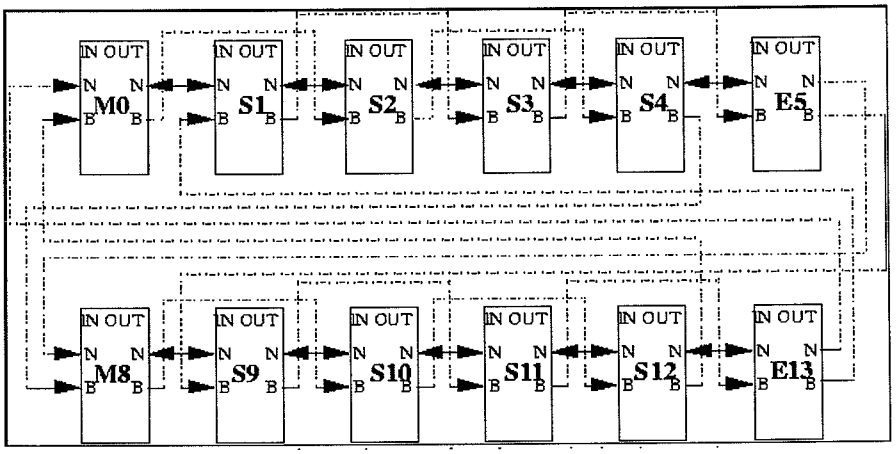


Figure 4.3: Diagram showing the normal flow of data and tokens between chips (active links are highlighted with solid links)

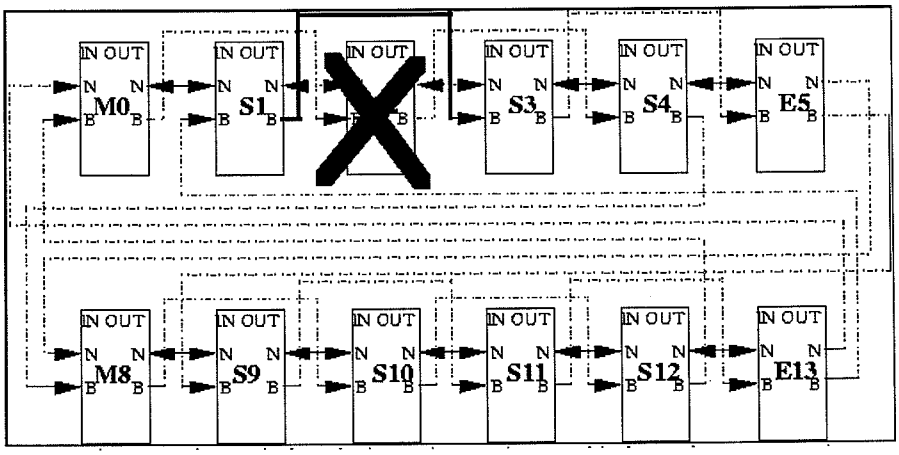


Figure 4.4: Flow of tokens and data in the event of the failure of a slave

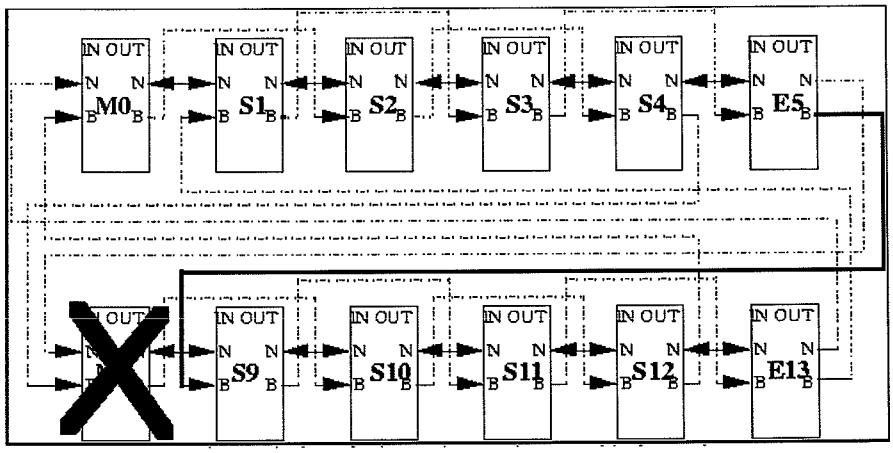


Figure 4.5: Flow of tokens and data in the event of the failure of a master

being an end chip.

The default state of the chip on powerup is determined by the state on the masterB input pin. If this pin has been left unconnected or tied high, the chip will power-up as a slave. If this pin has been tied to ground, the chip will power up as a master. If the chip has been configured as a master on powerup it may be reconfigured as a slave. However if the chip has been configured as a slave on powerup it may not be reconfigured as a master.

4.2 The road of the data

After having seen how the data are transmitted from chip to chip it is time to see the path the data follows through the chip (see fig. 4.6). First the signals coming from the detector are amplified and discriminated. That means the analogue data (current from the strips) coming from the detector is converted to digital data (binary values: 1 for a hit, 0 otherwise). Then the data are transferred to the *input register* which latches the incoming data, delivering a well defined pulse width to the *pipeline*. In the *input register* is incorporated the edge detection circuitry, which detects a high to low transition [5] in the data entering the *pipeline*, and for each of such transition found the circuit outputs a pulse of duration of 1 clock cycle irrespective of the length of the incoming pulse. This circuitry can be turned on or off by setting the appropriate bit in the *configuration register*[6]. There is also a *channel mask register* in the *input register*, which serves a dual purpose. First, it enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate to a level

[5] In the experiment p-on-n detectors were used, so the signal coming from the strips is a negative one (electrons).

[6] See section 4.2.1.

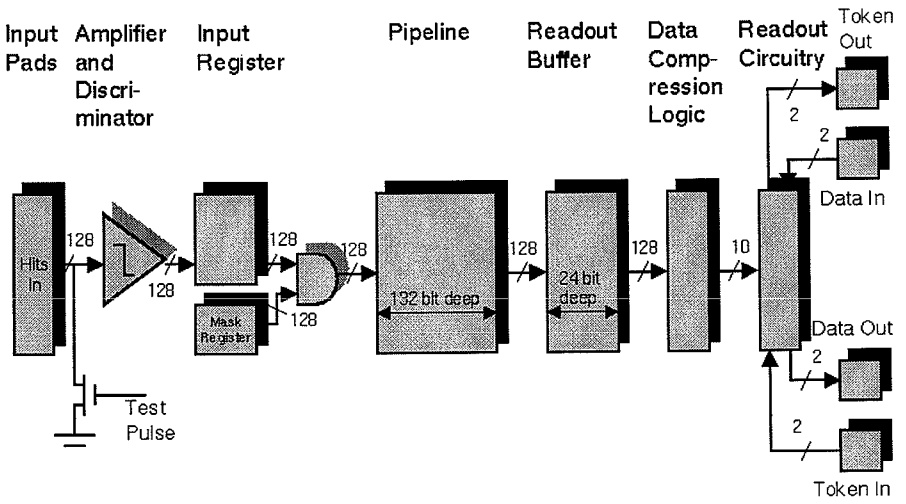


Figure 4.6: The flow of the data inside the ABCD chip

which would create dead-time from false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the *pipeline*. In test mode the inverted test pattern appears at the output of the *pipeline*. The contents of this register can be changed by sending the appropriate control command to the chip. The test pulse is masked by the *mask register* as well.

Then the data enters the binary *pipeline* which is realised as a multiplexed FIFO circuit. The pipeline block comprises 128 channels, each 132 bit deep. The hit pattern from the *input register* is shifted through the *pipeline* during 132 clock cycles. When a level one trigger arrives the pattern from the *pipeline* output is written to the *readout buffer*.

Three bits of data will be stored in the *readout buffer* for each channel per L1 trigger. These bits represent the three beam crossings centered on the L1 trigger time and are set if the input was above threshold during the corresponding crossings. In the case when the accumulator register has been enabled, the contents of this register will be copied into the *readout buffer* three times. This buffer will be 128 bits wide by 24 locations deep. This is sufficient to hold the data from eight L1 triggers. This satisfies the ATLAS specification of maintaining $< 1\%$ data loss at a L1 trigger rate of 100 kHz and a strip occupancy of up to 1% . The accumulator register is implemented in the *readout buffer*. This register marks all channels that have been hit since it was last cleared. If the accumulator mode is selected in the *configuration register*, a L1 trigger results in the transfer of the contents of this accumulator into the *readout buffer* instead of the appropriate time bin of the *pipeline*.

It is anticipated that on any event very few channels will contain hits. This

Mode	Name of selection criteria	Hit pattern	Usage
00	hit	1XX or X1X or XX1	detector alignement
01	level	X1X	normal data taking
10	edge	01X	normal data taking
11	test	XXX	test mode

Table 4.1: Hit patterns

fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The *data compression logic* works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each group of three bits is compared against one of four selectable criteria (see table 4.1). If the pattern meets the criteria, then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This process is repeated until the hit patterns from all 128 channels have been examined.

The *readout circuitry* will be responsible for capture and release of the token and outputting data from the chip. The *readout circuitry* always waits until the token arrives. On arrival of the token, it checks if any hits have been found by the *data compression logic*. If so, it then outputs the appropriate header information. It then proceeds to output the address of the hit channel together with the data from that channel. Once the *readout circuitry* has finished sending the data from one channel, it proceeds to output the data from the next channel. In the situation where one or more neighbouring channels are to be read out, only the address of the first channel is output, but the data from all hit channels is sent. The process continues until the *data compression logic* indicates that all channels have been examined. Once all the data corresponding to a single event has been read out, a token is sent out to the next chip in the readout chain. If the chip has no data to be read out, the circuitry sends out a "no hit data" code and passes the token on to the next chip in the chain. In the case of an error condition occurring, e.g. attempt to readout data and no data available, the appropriate error code will be sent by the readout logic. If the chip is in the send_id mode of operation, no data or error codes are output from the chip but instead a special packet of data containing information about the chips current configuration is sent.

The *readout controller block* is to control the readout of data from several ABCD chips connected together in a token chain. This block is enabled by placing the chip in Master Mode. This block has to detect when a L1 trigger has been received, issue a token to all the ABCD chips connected to it, collect all the data from the chips and tag the data with the beam crossing number from which it came and the number of level 1 trigger. This block then has to transmit this data serially to the LED driver chip.

The purpose of the token generation logic is to detect when the chip has

Type	Field 1	Field 2	Field 3	Description
Level 1	110	-	-	Level one trigger
Fast	101	0100 or 0010	- -	Soft reset BC reset
Slow	101	0111	command	see appendix .2 for more details

Table 4.2: Main types of commands

received an L1 trigger. This logic waits until the event FIFO[7] becomes not empty and it then issues a token. It then monitors the data passing through it from all the chips in the chain looking for the trailer bit pattern. It waits until this trailer is detected before checking to see if the event FIFO is empty. If the event FIFO is still not empty it repeats the cycle.

4.2.1 Commands

The command and control information all comes into the chip in the command input pins. There are two main classes of information which arrive here, level 1 trigger commands and control commands. These are distinguished by a 3-bit code. Furthermore two types of control commands are possible, fast control commands and slow control commands. Depending on which class arrives, further information may follow. This further information will also need decoding, formatting and sending to the appropriate functional blocks of the chip.

The Level 1 Trigger command is the most frequently issued packet and hence the smallest. All ABCD chips that receive this packet act on it. There is no addressing. If this command is received 3 samples are read out of the *pipeline* and written into the *readout buffer*.

There are two fast control commands:

Soft reset Its purpose is to clear all he buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset will be issued to the chip periodically during data taking to eliminate synchronization errors. Upon the receipt of the reset command, the ABCD chip resets all internal counters, clears tokens and sets itself to the no-data state.

BC reset it zeroes the beam crossing number. It has no effect on the operation of any other part of the chip.

To be complete, the third type of reset is the powerup reset. It is asyncronous, and it sets the value of the chip's *configuration register* to zero, and clears all the buffers in the chip, thus placing the chip into a well defined state.

[7]The event FIFO is loaded with the outputs of the L1-counter and the beam crossing counter, and then this information is appended to the data sent by the chip

If the second field of the command is decoded to be a slow control command, then he third, fourh, fifth, and possibly sixh fields are also decoded to determine the action required, and send the relevant instruction and data to other parts of the chip. While a slow control command is being sent, it is not possible to send a Level 1 Trigger. These commands enable to control the operation of the chip, like setting the configuration, threshold, and other registers, loading DACs, issuing calibration pulses and so on [8].

Two sets of clock and command inputs will be provided in order to make the system in which the ABCDs will be used fault tolerant and to provide an additional method of setting up the timing of the system. Each chip will be supplied with two independent sources of clock and commands. In the event of the fallout of one of these sources, the alternative source can be used. An external input to the chip "select" will be used to determine which pair of inputs will be used by the chip.

The *configuration register* is a 16-bit register which is used to hold information about the chip's current configuration. The powerup value of this register will be zero. The contents of the *configuration register* are listed in the table 4.3 . Its contents are not affected by a software reset.

4.2.2 The calibration logic

The calibration logic produces a calibration strobe signal for the front-end calibration circuit. This strobe is produced in response to a control command when the *cal enable* bit is also set in the *configuration register*. A two-bit calibration code is also sent to the calibration circuit which selects one of the four possible patterns in the front-end. The calibration strobe signal must be sent to the front-end a fixed number of clock pulses after the receipt of the control command. The delay from the rising edge of the clock signal to the rising edge of the strobe signal is determined by the value loaded into the *strobe delay register*. This delay can be adjusted in 64 equal steps over a range of 50 ns.

There are two 16 bit registers which hold 2 8-bit values each. The threshold/calibration register holds a threshold value and a calibration value. The threshold value is held in the most significant byte of this register and the calibration amplitude value is held in the least significant byte of this register. The outputs of this register control 2 separate 8-bit DACs. The outputs from these DACs supply two independent DC current levels to the threshold generation circuit and the calibration circuit. The reference current for these DACs is generated internally in the chip. This reference current will be scaled at the output of the DAC by a value of 0 to 255 depending on the setting of the DAC register. The threshold variation should be 4% channel to channel within one chip, and 20% including all process variations. The calibration capacitors should be of 100 fF +-20% over full production skew, and +-2% within one chip. The absolute accuracy of amplitude is supposed to be 5% (full process skew). The relative accuracy of amplitude should be less than 2% for known values of the

[8] For more details see appendix .2.

Bit	Name	Function
0-1	Readout Mode	Selects the data compression criteria (table 4.1)
2-3	Cal_Mode< 1 : 0 >	The state of these two bits determines which channels are tested when Test Mode is enabled
4	not used	
5	not used	
6	Edge_Detect	When this bit is set the edge detection circuitry in the input stage is enabled
7	Mask	When this bit is set the input register is disabled and the contents of the mask register are routed into the *pipeline*.
8	Acuumulate	This bit enables the accumulate function.
9	Input_Bypass	This bit determines which set of token/data inputs are active
10	Output_Bypass	This bit determines which set of token/data outputs are active
11	Master	When cleared the chip acts as a Master providing the masterB input pin is tied to 0
12	End	When set this bit configures the chip as the end of the readout chain
13	Feed_Through	When clear the chip outputs a 20 MHz clock signal but only if the chip has been configured as a Master.
14	not used	
15	Self Destruct	When set this bit prevents data getting into the hands of the bad guys.

Table 4.3: Configuration register contents

	Range	Resolution
Calibration signal amplitude	$0 - 160\ mV$	$0.625\ mV/step$
Calibration charge injected via $100\ pF$ capacitor	$0 - 16\ fC$	$0.0625\ fC/step$
Threshold voltage	$0 - 640\ mV$	$2.5\ mV/step$

Table 4.4: Threshold and calibration DACs - range and resolution

	Range	Resolution
Input transistor current	$0 - 294.4\ \mu A$	$9.2\ \mu A/step$
Shaper current	$0 - 38.4\ \mu A$	$1.2\ \mu A/step$

Table 4.5: Granularity of the current settings

calibration capacitors, amplitude range 0.8 to 4 fC, across one chip. The noise is expected to be lower than 1400 e^- for an unirradiated module.

The bias register holds a bias current value in the input transistor and a shaper bias current value. Bits 12:8 are used to set the DAC which controls the bias current in the input transistor. Bits 4:0 of the register are used to set the DAC which controls the shaper bias current. These bit ranges have been chosen to align the data for both DACs on byte boundaries. The reference current is generated internally as before, and will be scaled by a value between 0 and 31 (5 bits instead of 8).

The values contained in these two registers will play a very important role in the measurements which are presented in the following chapter.

Chapter 5

Testing

5.1 Introduction

5.1.1 What was measured

Strobe delay scans

The first type of measurements was the strobe delay scan. Normally, it was used to check that the calibration strobe signal arrives at the right time, i.e. the right timeslot in the pipeline is used to gather the data. On fig. 5.21 channel 385 shows the result of a typical strobe delay scan[1]. The x axis represents the delay of the calibration signal in nanoseconds, and the y axis represents efficiency. Ideally, it should be a rectangle, but the noise rounds off the corners. A delay value with an efficiency of 1 (=100%) for every channel and every chip has to be chosen in order to read out all the events in the threshold scans.

Threshold scans

A threshold scan is a measurement where the injected charge is fixed, and the threshold value is varied (see for example the first plot of fig. 5.17). Ideally, when the corresponding threshold is lower than the injected charge, the resulting efficiency should be 1 (=100%). When the corresponding threshold is higher than the injected charge, the efficiency should drop to 0. So the curve corresponding to a threshold scan should be ideally a step. Unfortunately there is the noise, which rounds off the corners of this step. This curve is called an S-curve (it resembles to an inverted S).

Important quantities

One of the most important quantities is the gain which is the mapping between the injected charge and the threshold that corresponds to this charge, so it is

[1] On this figure there are other anomalious strobe delay scans with queues, low efficiencies, that do not present any interest for the moment.

an indication of the amplification of the signal coming from the detector. The higher it is the better is the chip. In order to calculate the gain, measurements with different injected charges has to be taken. The 50%-points of the S-curves must be plotted as function of the injected charge. Then these points must be fitted with a straight line. Its slope gives the gain, while the intersection with the y axis gives the offset. The expected gain is $\approx 160\ mV/fC$ and its spread should not exceed 2% in a chip between the different channels. The offset values of the different channels should be centered around 0, and the spread should stay below 4% [2]. The ENC (Equivalent Noise Charge) is expected to be lower than 1400 e^-. The noise can be deducted from the "width" of the S-curve: the bigger the deviation from the step, the bigger the noise. This noise will be given in millivolts, which can be translated to electrons using the value of the gain: $ENC = \frac{noise}{gain}\frac{1}{e}$.

5.1.2 Overview of the measurements

Different tests were carried out in order to test the chip. First, the tests involving single chips on a PCB will be described. Then the configuration will include also a baby-detector. The next step will be to fully populate a hybrid with 6 chips and see how it works. Finally the measurements using a fully populated hybrid and a full-size detector will be described.

5.2 Tests involving a single chip on a PCB-board

5.2.1 The setup

The setup for the single chip testing is presented on fig. 5.1. The setup is based on a VME-crate where the devices that control the chip (SEQSI and DRAFT) are stacked. The VME memory can be accessed from a PC that controls the measurements. The PCB is a board that was specially designed to test single ABCD chips. In the tests described here, 4 PCB boards were used.

The SEQSI

The SEQSI stands for SEQuencer for use in Silicon readout Investigation. It is essentially a programmable multi-channel pulse generator, which may be used to provide control signals for driving silicon detector front-end readout chips.

The basic schematic describing the SEQSI is shown on fig. 5.2. The data memory is 32 bits wide, 64 k deep. This memory is loaded from the VME backplane with the required data. The address is provided by a counter, which is incremented by the clock. A clock also latches the data from the memory. The 20 least significant bits of the latch (B(0:19)) are output to a 50-way front panel connector. When the most significant bit (B31) is asserted the address

[2] In this case the spread is calculated as the spread at the threshold corresponding to 1 fC, that means $spread\ of\ offsets = \frac{sigma\ of\ offsets}{gain}$.

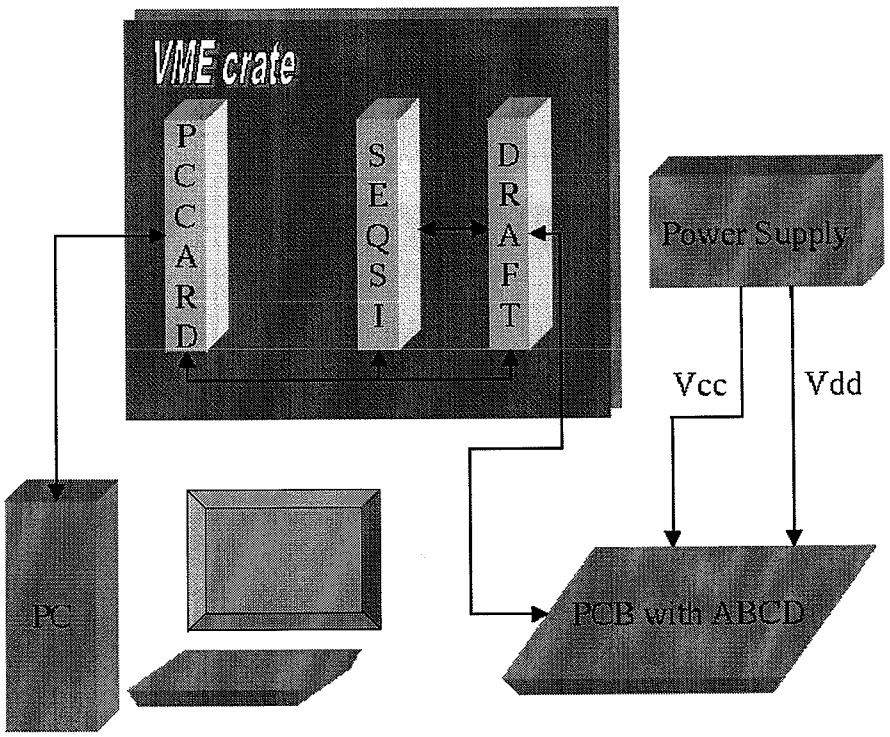


Figure 5.1: The setup for single chip tesing

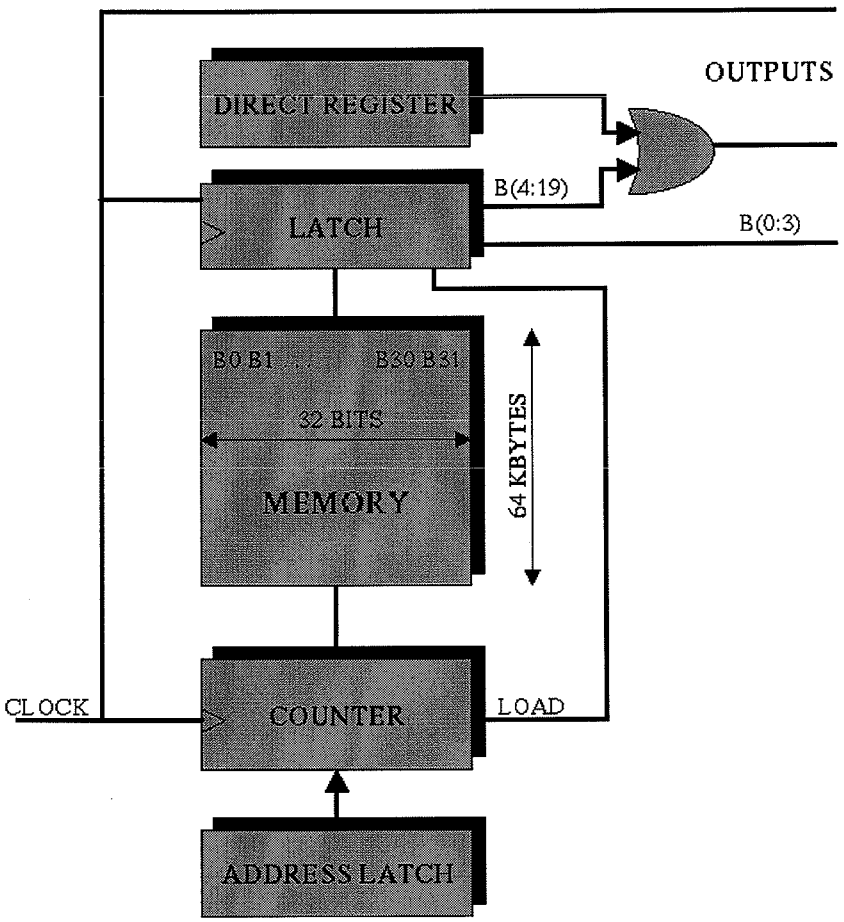


Figure 5.2: The heart of the SEQSI

counter is loaded with an address contained in the address latch (pre-loadable from VME) and the sequence continues until B31 is again asserted (that is why it is called a jump bit). B(4:19) bits of the output are OR-ed with the DIRECT register, thus they can be driven directly from the VME. B(29:30) are output directly and can be used to trigger the oscilloscope.

The sequencer was designed to be capable of responding to random external triggers. There are two registers which can provide an address to be loaded into the memory address counter. One is called the jump address register, and the other is the interrupt address register. When a trigger pulse is fed to the trigger input of the front panel the contents of the interrupt address register are loaded into the memory address counter. The sequence then jumps to the location specified in the interrupt address register and continues until the jump bit, B31 is asserted, when the sequence returns to the location specified in the jump address register.

A way in which a sequence with random triggers might be used is illustrated in fig. 5.3. The sequence starts at a, which is the number loaded into the address counter before starting the sequence (i.e. turning the clock on). Typically the sequence resets the front-end chip. From b to c it will be an idle loop, in which the sequence would stay until the receipt of a trigger. After receipt of trigger the sequence goes to d (the number loaded into the interrupt address register). From d to e is the readout sequence. At the end of it the sequence returns to the idle loop.

A threshold scan, where data are gathered using several thresholds, and for every threshold five events are read out can serve as an example to better understand the programming of the SEQSI (see fig. 5.4). First the chip has to be initialized (*Initialization Sequence*, from a to b). Then the sequence enters the idle loop(*Idle Loop*, from b to c), where it stays until the receipt of the trigger. In this measurement the triggering is performed by software: the trigger signal is written in the DIRECT register to B10 which is connected to the trigger input. First the chip must be read out five times, so the interrupt address register is loaded with the address of the beginning of the readout sequence, and five triggers are sent (*Readout Sequence*, from d to e is executed five times). After reading out the planned amount of data the threshold has to be changed, so the interrupt address register is loaded with the address of the beginning of the sequence that sends the corresponding command to the chip (in the present example *SET THRESHOLD 1*). A trigger is sent to load the address counter. At the end of this sequence the jump bit will be asserted, so the SEQSI will return to the idle loop. Now the interrupt address register can be loaded again with the address of the readout sequence, and five triggers can be sent to get the data for the new threshold, and so on.

The DRAFT

DRAFT stands for Data Receiver for Atlas Front-end Testing. It was designed to receive, decode and store the data from the ABC and ABCD test systems. It also provides the control signals needed by the test system, and can receive data

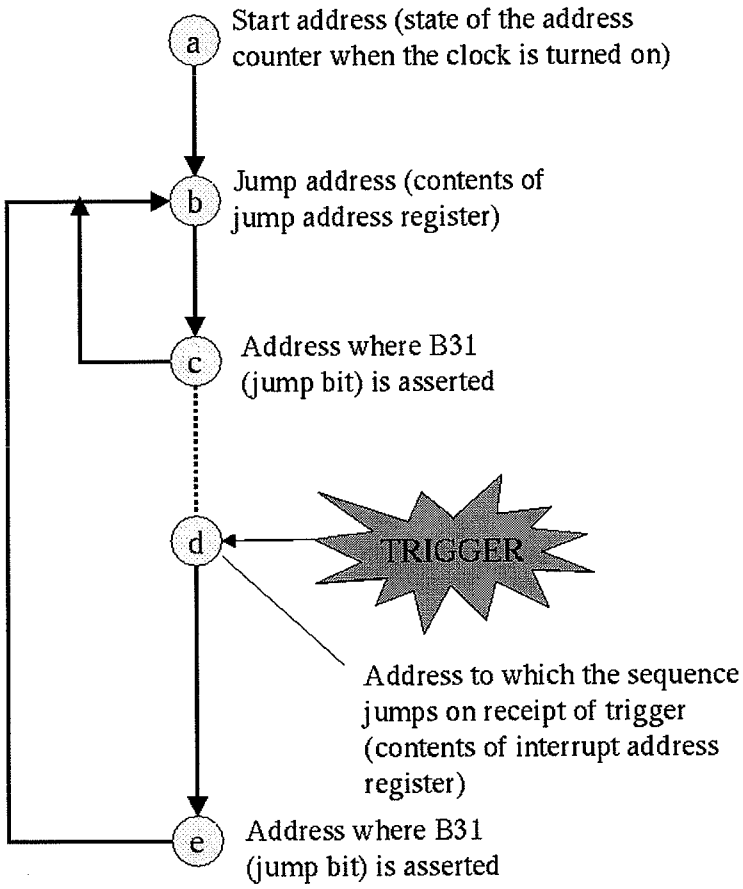


Figure 5.3: Typical SEQSI sequence

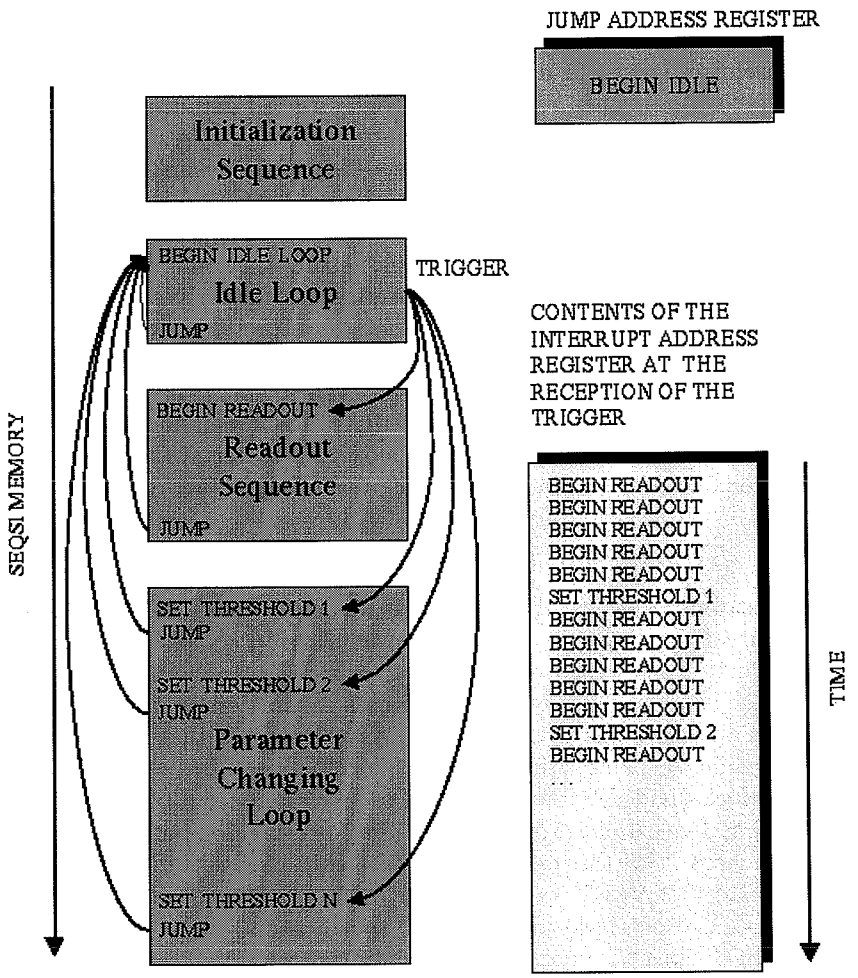


Figure 5.4: The sequence used to test the chip

from up to 8 chips directly. It has the capability to fix the mark/space ratio and the polarity of the clock. All signals are provided at ECL levels (however $clk0$, $clk1$, $com0$ and $com1$ are available also in LVDS in order to connect them directly to the chip but the PCB was designed to receive ECL signals, and then convert them to LVDS). DRAFT has a memory of 64 Kbytes, arranged as 32K 16-bit words. Data can be stored in two ways, either raw or decoded. In the measurements the decoded mode was used in order to to get rid of the headers, trailers and other control sequences. There is only one case when raw mode was useful (apart from debugging, but even then it is more adequate to use the oscilloscope), when reading back configuration data from the chip, because the DRAFT doesn't decode it. The data is then written to the VME memory, from where it is read by the computer. The DRAFT must know the mode the chip is operating in, slave/master and/or end-chip, in order to decode correctly, otherwise it will signal an error . One of the problems that can occur is that while sending a command – for example setting the configuration register – the SEQSI or the DRAFT transmit the sequence incorrectly and one of the bits is either missing or incorrect. The chip may interpret it or not, but weird things will happen, and it's very improbable that the chip will send back something meaningful. In the DRAFT there is an event counter, and if the chip doesn't send anything decodeable, then the DRAFT will wait forever for the results. This limits the time of the runs, because after a certain amount of time it is very probable that an error will occur preventing further data taking.

5.2.2 Testing the basic functionalities of the chip

The first wafer was already cut when it was received at CERN, but without the mapping of the chips (it is not known which chip comes from which region of the wafer). That wasn't a good thing, especially as the manufacturer warned that there were problems with the process parameters in one part of the wafer.

The first task was to see if the chip works at all, that means to turn it on and provide the clock. After startup the chip should be in *Feed_Through* mode, so the clock divided by two should be seen at the output of the chip. The clock divided by two came out of the chip after powerup as expected. Next on the list was to check if the current drawn by the chip is within the specifications. For $V_{DD} = 3.5\ V$ it was 50 mA in master mode and 30 mA in slave mode (40 mA and 20 mA respectively in the ABCD specification).

Then the basic commands of the chip were executed to see if the digital part works as expected. The following plan was carried out:

1. Initial tests
   - Feed_through test: trying to change bit 13 of the configuration register, in order to see the clock divided by two disappear
   - Reading configuration data after chip initialization (sending L1 trigger and looking at what comes back)
2. SendID mode

- Loading the configuration register with different values, and checking if the change has taken place, trying sending commands and clock on both lines

3. Testing the DACs
   - Looking at the threshold generation circuit (pins VTHP, VTHN accessible on the PCB) if the measured voltage agrees with the values set via the DAC register
4. Data Taking Mode: input from mask register, accumulate function disabled, edge detection circuitry off, hit mode
   - No data test – see if the No Hit Data Packet arrives
   - Single channel test
     - First channel hit
     - Last channel hit
     - Some random single channel readouts
   - Multiple channel tests
     - 128 channels hit
     - Random patterns
5. Accumulator and mask register tests (masked input register for accumulator testing)
   - No hit accumulator test
   - All hit accumulator test
   - Using several masks to see whether the accumulator register really accumulates the data

Then the first threshold scans were made using external calibration charge. Right after the results were compared with those obtained using internal calibration, and they were coherent [3]. So for the sake of simplicity in the following measurements mostly internal charge was used, because it can be set by software.

Until now signals were sent on both command and clock lines. It was interesting to see if having both lines has an effect on overall performance. Apparently (see fig. 5.5) having only one set of lines improves qualiy a little bit. That must be the result of not having two interfering signals in the digital part.

The functionality of the edge-detection circuitry was checked next. A serie of measurements was taken using edge-sensing mode, and level sensing mode, and as expected with edge sensing mode a little bit less events were obtained (fig. 5.6). When setting the edge sensing bit, but turning the edge-detection circuitry off the chip automatically puts itself in level sensing mode as expected.

[3] !!! inverted calstrobe!!!

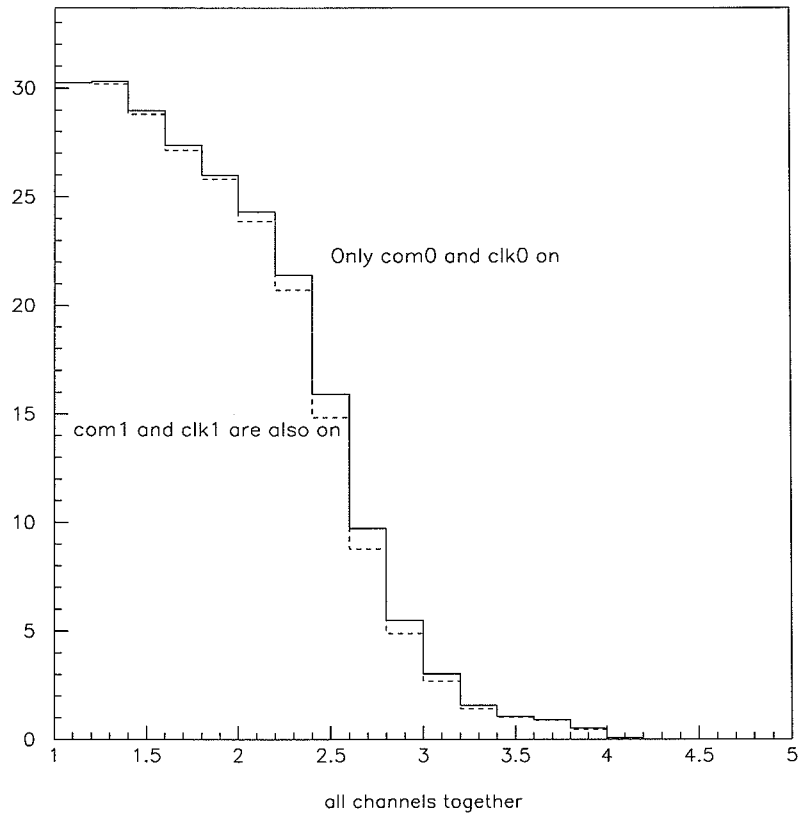


Figure 5.5: Two sets of command and clock lines vs. one (2.5 fC)

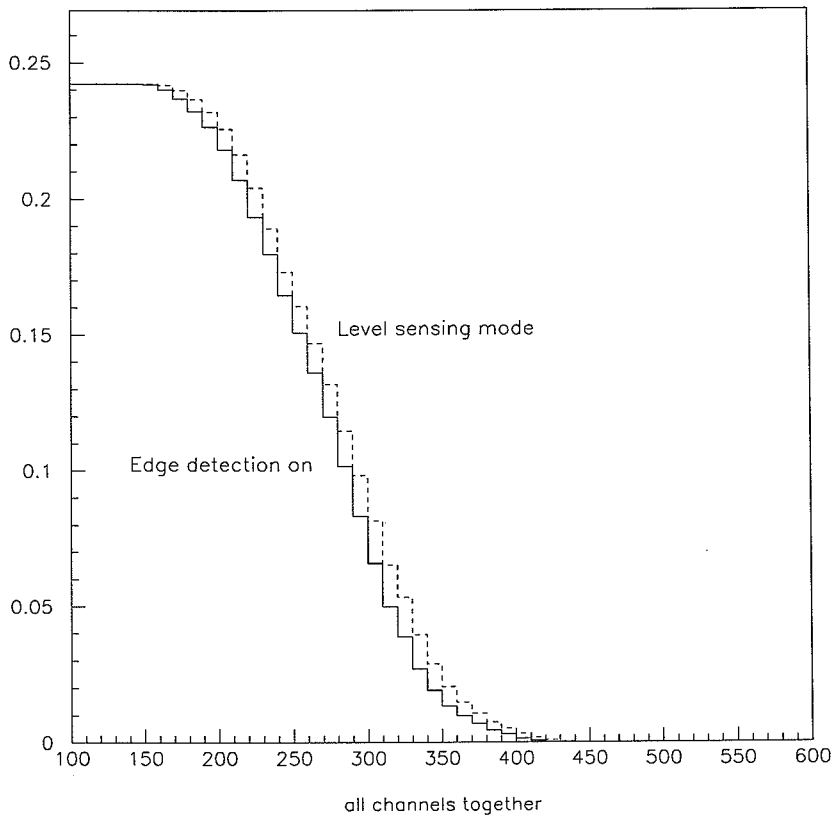


Figure 5.6: Edge sensing and level sensing modes

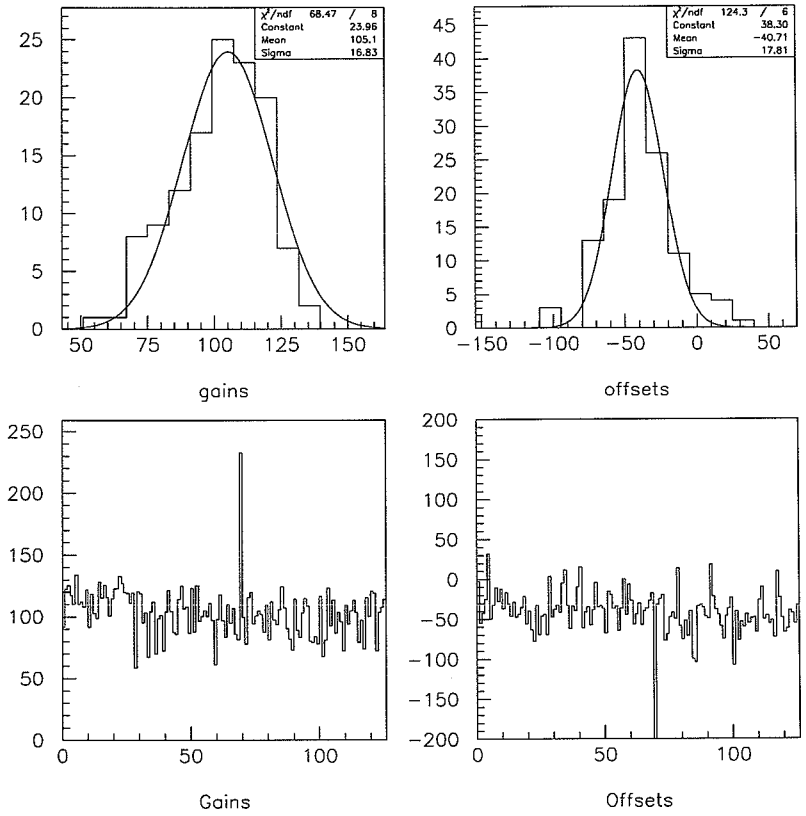


Figure 5.7: Gains and offsets for $I_{shaper} = 20\mu A$ and $I_{preamp} = 200\mu A$

Another interesting thing was to see if the communication between chips worked well. As on the PCB there was only one chip, the other chip was faked by software. That means the chip on the PCB was configured as master, but not as end chip. To the *datain* line of the chip the software sent an "event" (a sequence of bits), and the aim was to see the master append the "data" coming from the faked slave chip. The experience showed that it was true if the delay between the sending out the token and receiving the data didn't exceed a few μs[4].

The next step was to calculate the gains and offsets of different channels. What we can see from fig. 5.7 is that there is a big dispersion between channels,

[4]For example if the delay equals the longest possible data packet $\approx 17\ \mu s$, then the master doesn't detect the data of the slave.

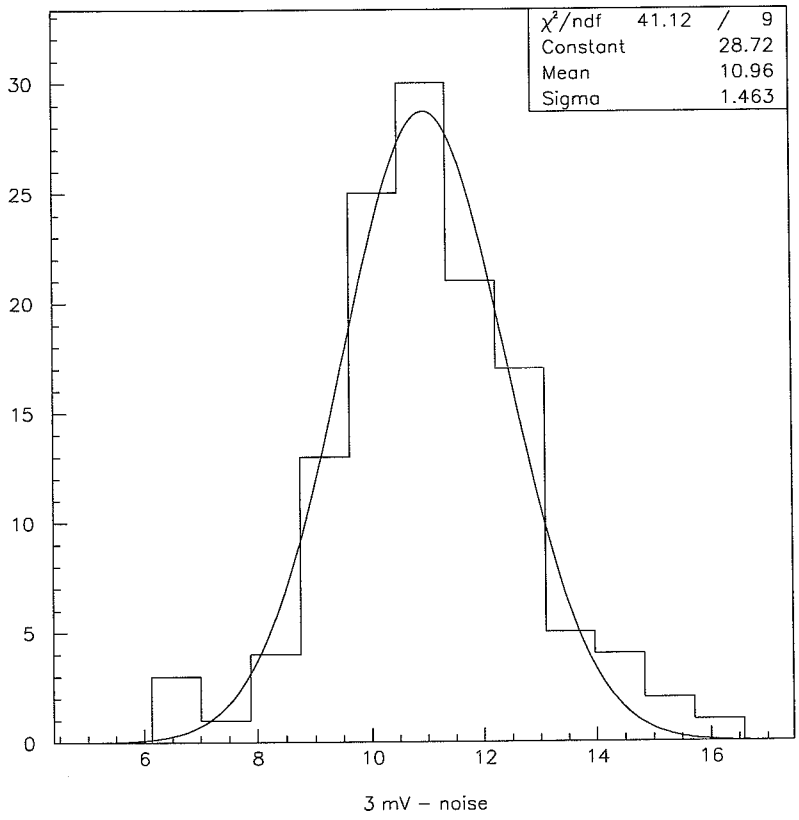


Figure 5.8: Noise for $I_{shaper} = 20\mu A$, $I_{preamp} = 200\mu A$, and 3 fC

Analogue supply (V)	3.2	3 35	3.5	3.7
Optimal I_{preamp} (μA)	193.2	202.4	211.6	220.8-230

Table 5.1: Optimal input transistor current for different analogue supplies

much bigger than what was projected: 16% instead of 2% for the gains and 17% instead of 4% for the offsets. The gain is also lower than the 160 mV/fC expected. The offsets were expected to be centered around 0, instead the mean of the offsets is -41. The value of the noise is $\approx 650\ e^-$, than can be reagarded as normal.

5.2.3 Preamplifier and shaper bias dependance – what went wrong

A measure that revealed something interesting (and alarming) was the determination of the S-curve dependance on the preamplifier bias, shaper bias and the V_{cc}. Measures were taken in the range of $V_{cc} = 3.2 - 3.7\ V$, $I_{preamp} = 184 - 230\ \mu A$ and $I_{shaper} = 9.6 - 21.6\ \mu A$ (the nominal values are $V_{cc} = 3.5\ V$, $I_{preamp} = 200\ \mu A$ and $I_{shaper} = 15\ \mu A$). The external charge injected in the chip was 4 fC.

The first noticeable thing was that the quality of the threshold scans depended very heavily on the preamplifier current [5] (fig. 5.9). Practically there was only one value of I_{preamp} which gave rise to normal S-curves.

Another observation is that the optimal input transistor current depends on V_{cc}. This dependance is expected from the input cicuit characteristics. In the table 5.1 are presented the optimal values found for the different analogue supplies.

That means the optimal premplifier bias shifts roughly 10 μA every 0.15 V.

The narrowness of the I_{preamp} range gives rise to a serious problem demonstrated on fig. 5.10. There are two values that look approximately equally good 220.8 μA and 230 μA, but in spite of a higher analogue supply they don't give better results than what is presented on fig. 5.9. The likely reason is that the optimal value is somewhere between the two $\approx 225\ \mu A$. However the problem is that the input transistor current is set via internal DACs, so it can take on only discret values. More precisely one can set it using a 9.2 μA step[6]. In these measurements the best possible granularity was used, and even that wasn't enough. An idea than can come into mind is to fix the preamp current and adjust V_{cc}. This way it would be possible to have optimal results. But there is a big problem with this approach: on a hybrid every chip must have the same analogue supply, so it's impossible to adjust it on a per chip basis (on the contrary one can adjust the bias values individually).

[5] Throughout this work I_{preamp}, preamplifier bias/current and input transistor current are used interchangeably. The same goes for analogue supply and V_{cc}.

[6] See section 4.2.2.

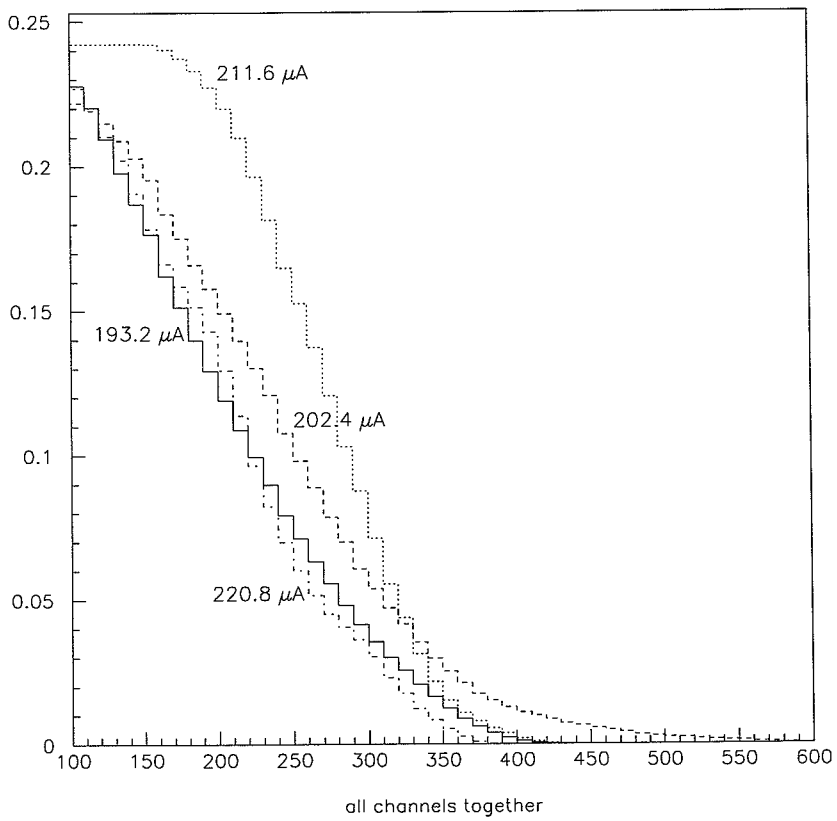


Figure 5.9: Sharp dependance of the S-curve on the input transistor current

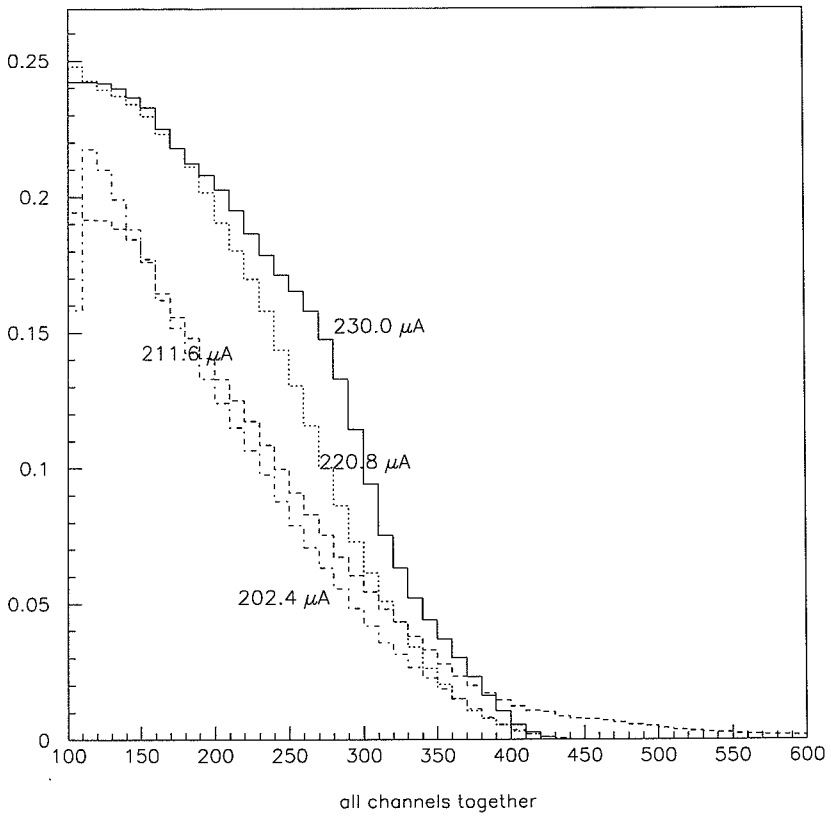


Figure 5.10: S-curves for different values of I_{preamp} for $V_{cc} = 3.7\,V$

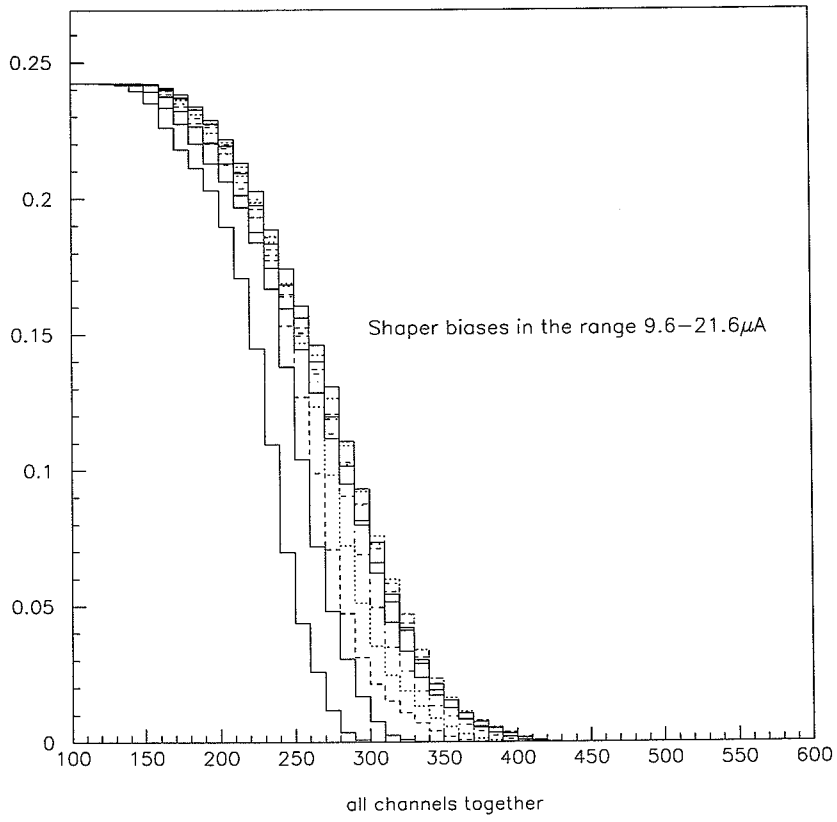


Figure 5.11: Different shaper bias values for fixed $V_{cc} = 3.5\ V$ and $I_{preamp} = 211.6\ \mu A$

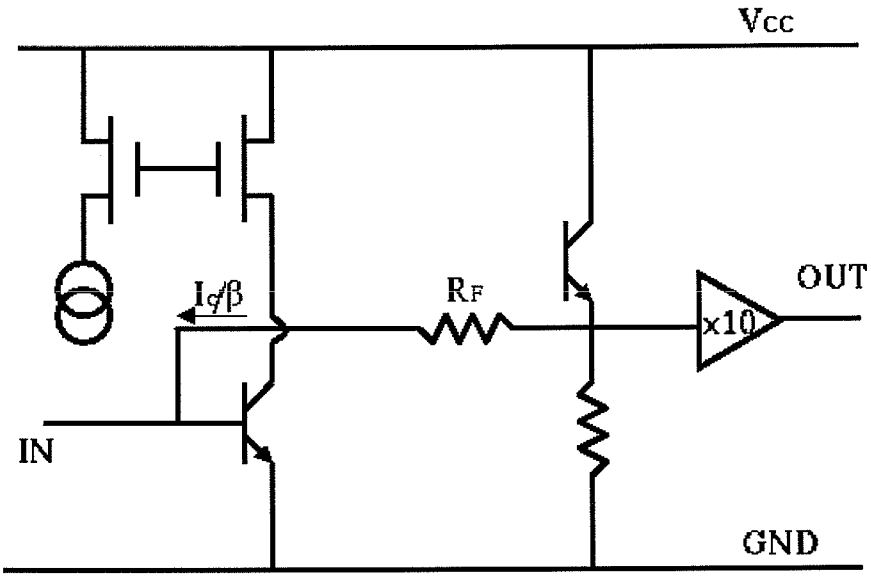


Figure 5.12: Internal structure of the amplifier

Fortunately the chip seems to be much less sensible to the variations of the shaper bias (fig. 5.11). There are usually 4-5 values which give rise to reasonable S-curves.

These results show that the quality of the S-curve depends a lot on the preamplifier bias (or V_{cc}). They were later confirmed by the wafer probing which involved testing all the chips which were on uncut wafers. [7]

As it was found out, the problem was that the manufacturer didn't respect the processing parameters agreed. In fact, the β[8] was lower than the value of the specification, and the resistors were at the high end of the specifications. Apart from that, the wafer probing showed that the yield was also quite low, about 20-30%.

To better understand the problem it is useful to look at the internal structure of the amplifier circuit in the chip (fig. 5.12) [9]. It can be seen that the lower than agreed β implies bigger current I_c/β which goes through R_F. $U = RI$ so the DC operating point of the amplifier will be shifted. To make matters worse the value of R_F is higher than the one agreed. That moves the DC operating point even further out of range. As the whole chip was already optimized, it resulted in a very narrow range of preamplifier bias values where it can operate

[7]????? maybe some results from the wafer probing????

[8]β is parameter describing the transistors of the chip. The gain is proportional to this parameter.

[9]Obviously, this is only an approximative functional view of the internal structure.

effectively. As irradiation measuremens showed a 30-50% increase of resistance after irradiation, it is really necessary for Temic[10] to keep the process parameters under control in the future. They acknowledged that there were some problems keeping the process parameters within the specificaions and the two sides agreed on reprocessing the ABCD with the existing mask set (the new wafers should arrive early July). This will have the re-targeted higher beta and lower resistance included, and should permit to improve the analogue performance at least to the level of SCT128B[11].

5.3 Testing a single chip with a baby-detector connected to it

5.4 Module testing

The next step in testing the ABCD chip was to populate an Oslo-hybrid with 6 ABCD chips and connect a detector to the hybrid. The idea was to bring the module in the H8 test beam in June. Unfortunately, there was a lot of problems – no beam, then a magnet went wrong, there were problems with data acquisition, because the DAQ-team uses a different setup, and so on. Nonetheless even without a test-beam the measurements that were executed showed a lot of interesting results.

5.4.1 The setup

The setup was very similar to the previous ones, but slightly different (see fig. 5.13). The PC was replaced by the RAID, which is a VME base board with a local processing unit, memory and other resources that make it useful as a general-purpose processor witthin the VME addressing space. In particular it runs a Unix-type operating system. The *abcd* program runs on it and the data is saved on its hard-disk. The RAID can be mounted on the Sun and used transparently to the user. There is the SEQSI and the DRAFT as in the previous setups. However, this time a BC96 card is used in order to provide both the signals and the supply voltages for the hybrid, because there is no PCB, so LVDS signals have to be provided directly. There's again a separate power supply for the detector.

For every chip it was possible to set the threshold, strobe delay and the biases individually . It is also possible to set the power supply values (V_{cc} and V_{dd}) automatically by software. This is a big advantage of using this card over the baby-detector setup, where it is necessary to adjust the power supply manually every time. On the other hand BC96 caused some problems, especially instability of the clock, and noise.

[10]Temic is the manufacturer of the ABCD chips.
[11]??performance of SCT128B??

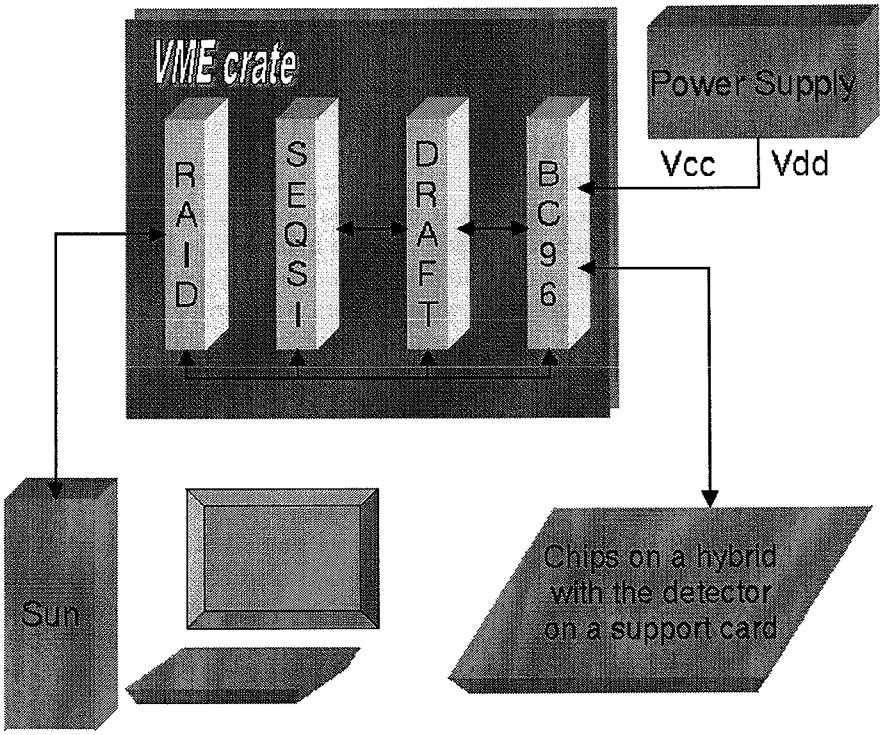


Figure 5.13: The test setup for module testing

The chips were put on an Oslo-hybrid, the details of which are in appendix .4. [12] The best chips available were used to populate the hybrid. The choice was based on results from the wafer testing: tests similar to the ones that were presented earlier (see section 5.2.2) were performed using a probe station on every chip while the wafer was still uncut [13].

5.4.2 Tests without the detector

First, tests were carried out to see what is the behaviour of the chips when placed on a hybrid. The first thing that was noticed is that it was impossible to make work the last chip. It was the case with two, three and six chips (measurments were performed after placing two, three chips in order to see if everything was going well). It turned out that the *datain* pin of a chip must be at 0 while transmitting the trailer. In the experimental setup the chips before the last had the output of the next ones tied to their *datain* so the input was in a well defined state. However the *datain* of the last one was in the air. So, at powerup this input was settling in an arbitrary state. An obvious solution was to settle it to the state 0 by grounding it, but the current drawn was too high and the bond melted. Therefore a resistor had to be placed to limit the current, but for this, the kapton cable had to be modified, so in the early measurements data were gathered only from 5 chips.

After seeing that the chips were all working, the aim of the measurements was to find the right settings for every chip. This way it would be possible to concentrate on other problems after connecting the detector to the hybrid. Of course this was based on the assumption, that the right parameters would be the same with the detector on. An assumption that turned out to be right.

Checking the strobe delay

The strobe delay was checked in order to see if the timing was right. The optimal strobe delay value was checked for different values of V_{cc}, charge, preamplifier bias and shaper bias. Seemingly the optimal strobe delay does not vary much if values close to the specified ones are used. It is safe to apply 19 ns to all chips for the ranges of $V_{cc} = 3.3 - 3.6\ V$, $I_{preamp} = 184 - 220.8\ \mu A$, $I_{shaper} = 14.4 - 22.8\ \mu A$, $Q = 2 - 6\ fC$.

Searching for the "perfect" parameters

The idea was to keep $V_{cc} = 3.4\ V$ and $V_{dd} = 4.2\ V$ because from previous measurements these seemed to be the best values and search through the range $I_{preamp} = 184 - 220.8\ \mu A$ and $I_{shaper} = 14.4 - 22.8\ \mu A$. After taking the measurements the choice was based on the S-curve and on the distribution of the noise. On fig. 5.14 the S-curves for the whole range of the shaper bias values for 202.4 μA are presented. Obviously choosing the best one by looking at this

[12] ??? is this necessary????

[13] ??? maybe wafer result??? +reference to the paper describe qualitty factor...

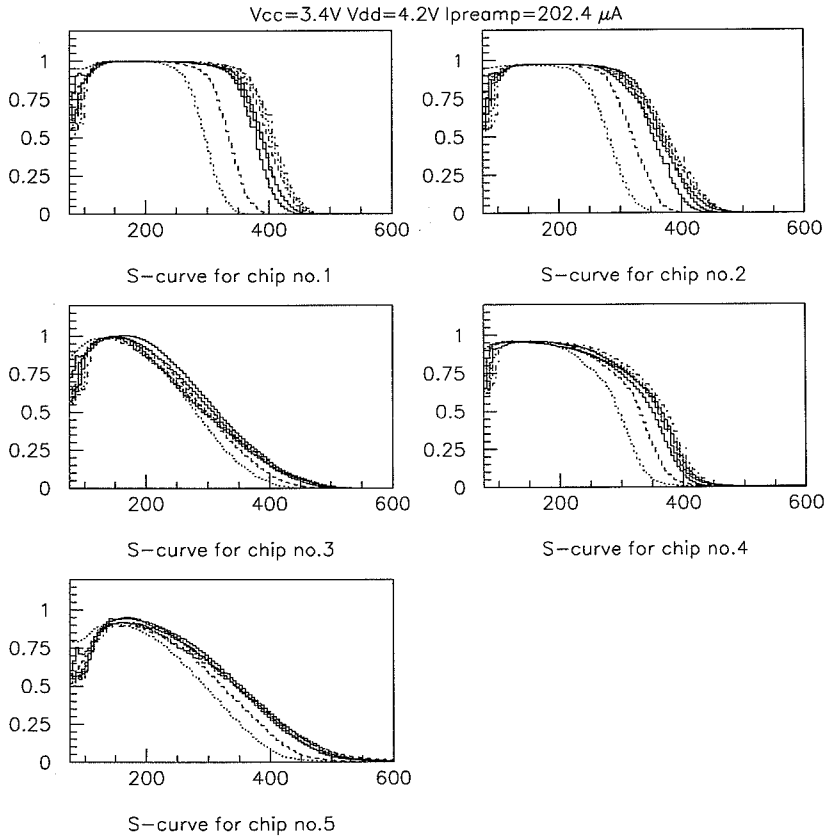


Figure 5.14: S-curves for all the shaper biases for a fixed preamp bias for all the chips

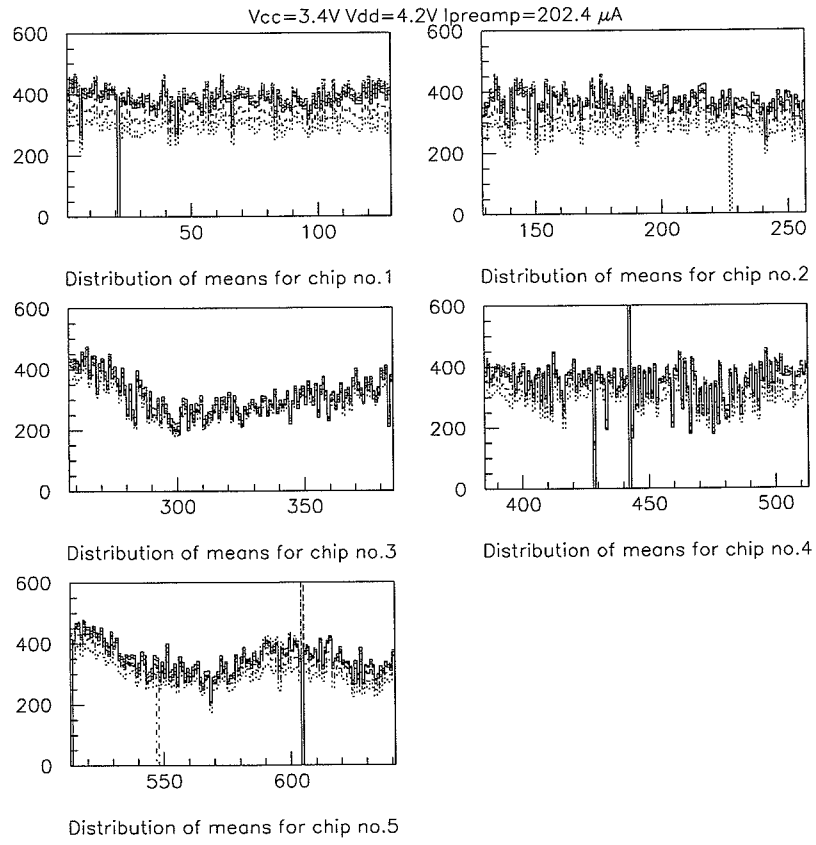


Figure 5.15: 50%-point distribution for all the shaper biases for a fixed preamp bias for all the chips

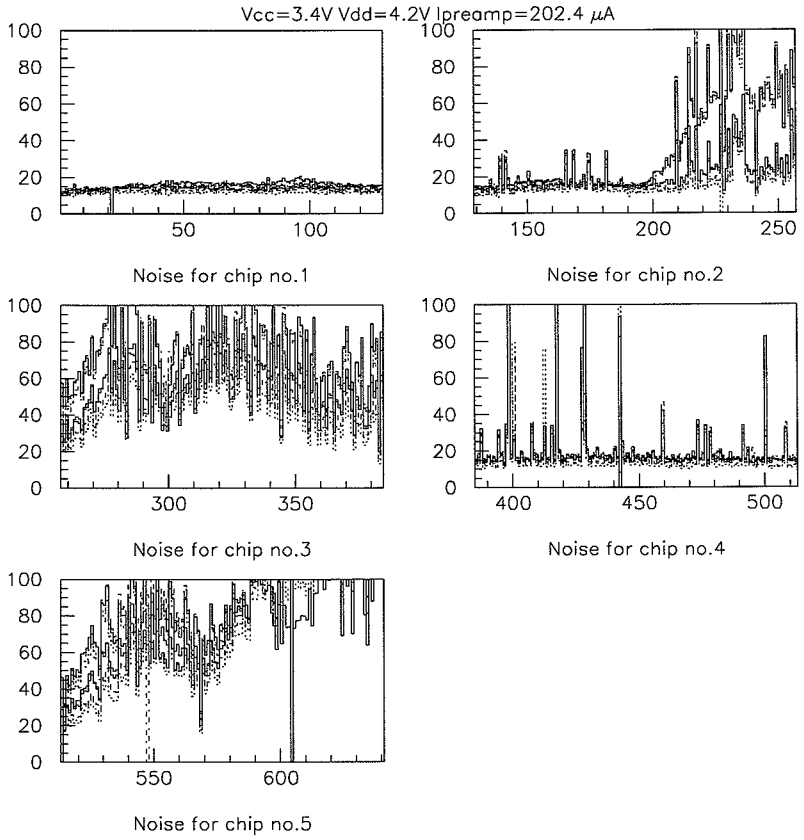


Figure 5.16: Noise disribution for all the shaper biases for a fixed preamp bias for all the chips

plot is a difficult task, but the PAW macro prints them one after another at the rhythm of the user pressing Enter, so the user can easily select the best S-curve (with the highest 50% point). Then the noise and 50%-point distributions were checked. To be accepted these distributions must have been constant, without "holes" or "bumps". The plots where noises and means were evenly disributed were always privileged, even if it meant to lose a little bit of gain.

Afterwards it looked necessary to have a higher gain in order to have results in the beam test (or with a radioactive source), so an attempt was made to increase the gain. Increasing the gain means increasing V_{cc}. V_{cc} was increased to 3.5 V (the nominal value; see appendix .3 for nominal values) that was also used in earlier measurements. Of course higher voltage caused much higher noise. In order to correct V_{dd} was decreased to 4.0 V [14]. Now the results begun to look better. Of course, the scans must have been redone because the change of V_{cc} shifts the good preamplifier values (as described in section 5.2.3). After redoing the scans the following values were found to be the best (after looking at the S-curves and the noise profiles):

Chip no.	1	2	3	4	5
Input transistor current (μA)	211.6	211.6	220.8	211.6	220.8
Shaper bias (μA)	19.2	19.2	19.2	20.4	19.2

Table 5.2: Optimal bias values for $V_{cc} = 3.5\ V$ and $V_{dd} = 4.0\ V$

Using these parameters the results presented on fig. 5.17-5.19 were obtained. The results look relatively good. Concerning the S-curves the first two and the fifth look reasonable. The problem with the 3^{rd} and 4^{th} is what was described on page 68, the granularity of the preamplifier bias values is not fine enough to reach the optimal operation, and it is impossible to set a unique V_{cc} value that would result in good input transistor and shaper currents. The means are fairly uniform, except for the third chip where there is a "hole" at the end. The noise seems to be really uniform all over the 5 chips.

There is a problem with he noise for some of the channels of the 2^{nd} and 4^{th} chips. Looking at the S-curves (see fig. 5.20) of some channels that have seemingly big noise, it turns out that there is nothing wrong with the noise, but because of the inefficiency of the channel the fit doesn't converge correctly (because it is assumed, that the S-curve has a plateau at 1).

Fig. 5.22 confirms that two chips have this strange behaviour. In the case of the 2^{nd} chip there are two different "classes" of inefficient channels, while the 4^{th} chip shows also a third "class". The reason of these inefficiencies is not clearly understood at the moment.

In order to obtain the gain and offset values for the chips several different charges [15] were injected to the chips . What was learnt from this experience is

[14] Lower digital supply means slower signals, slower edges, less parasites.
[15] In this case the internal capacitors were used.

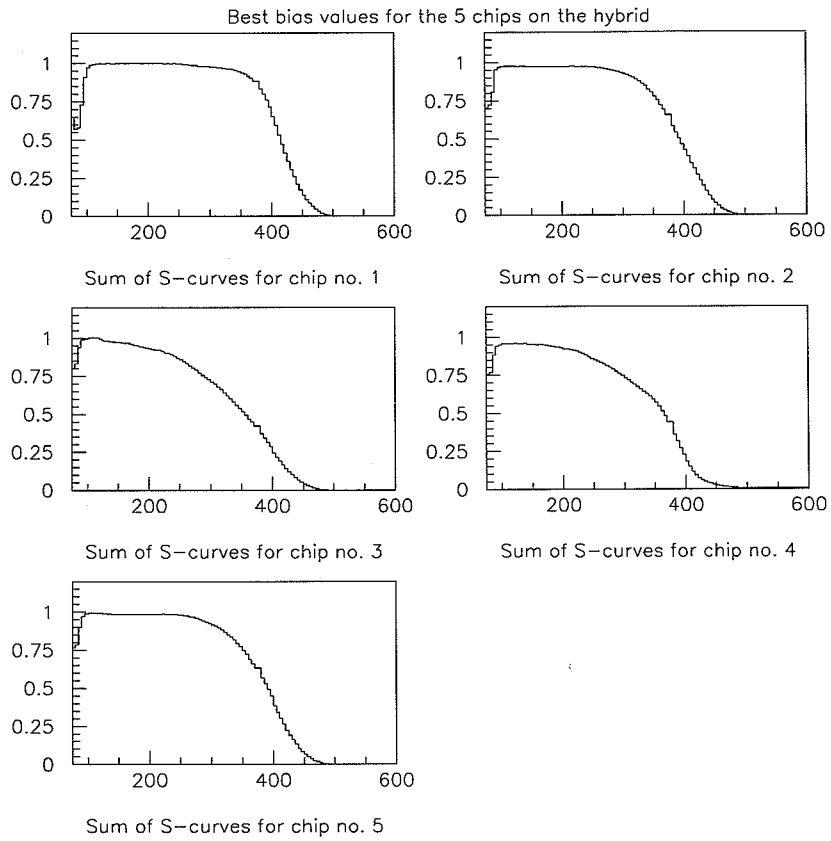


Figure 5.17: S-curves for the 5 chips with the best values for the biases

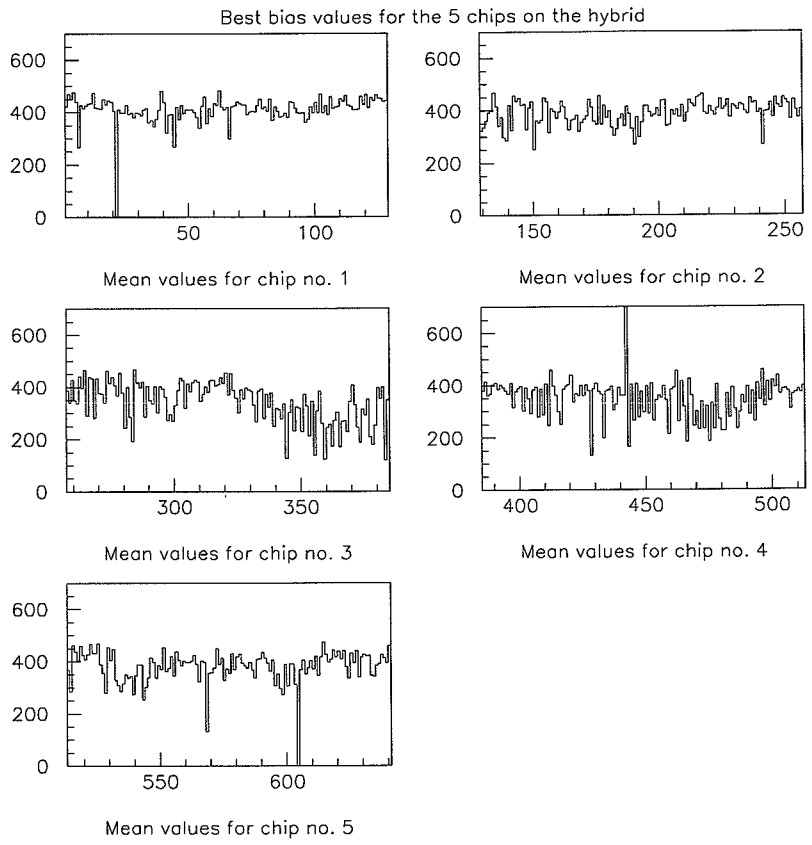


Figure 5.18: 50%-point distribution for the 5 chips with the best values for the biases

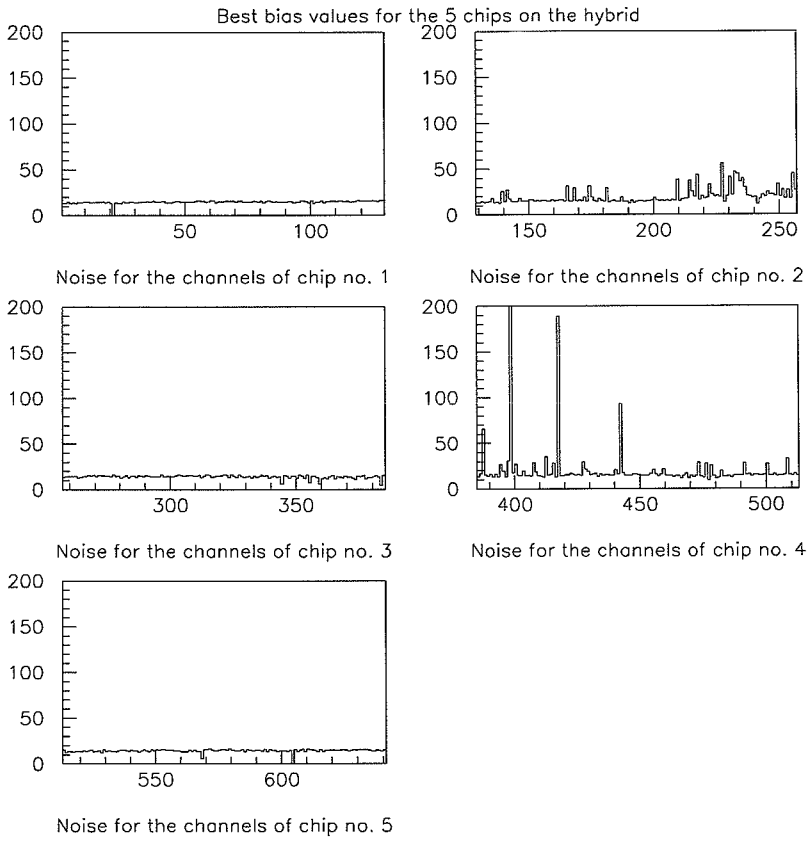


Figure 5.19: Noise for the 5 chips with the best values for the biases

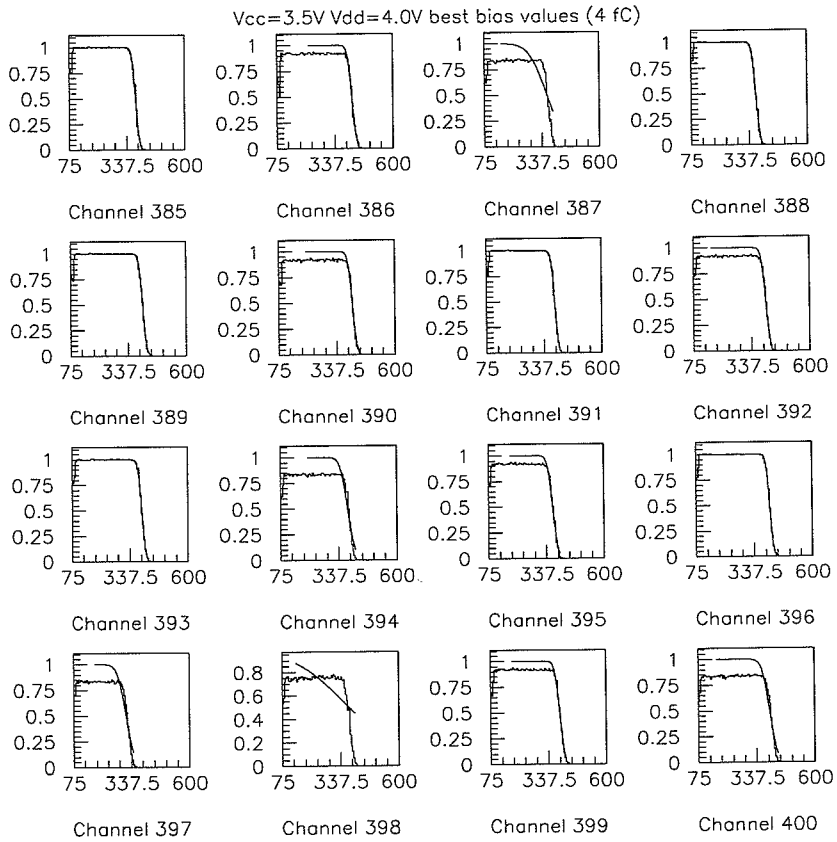


Figure 5.20: S-curves for some individual channels

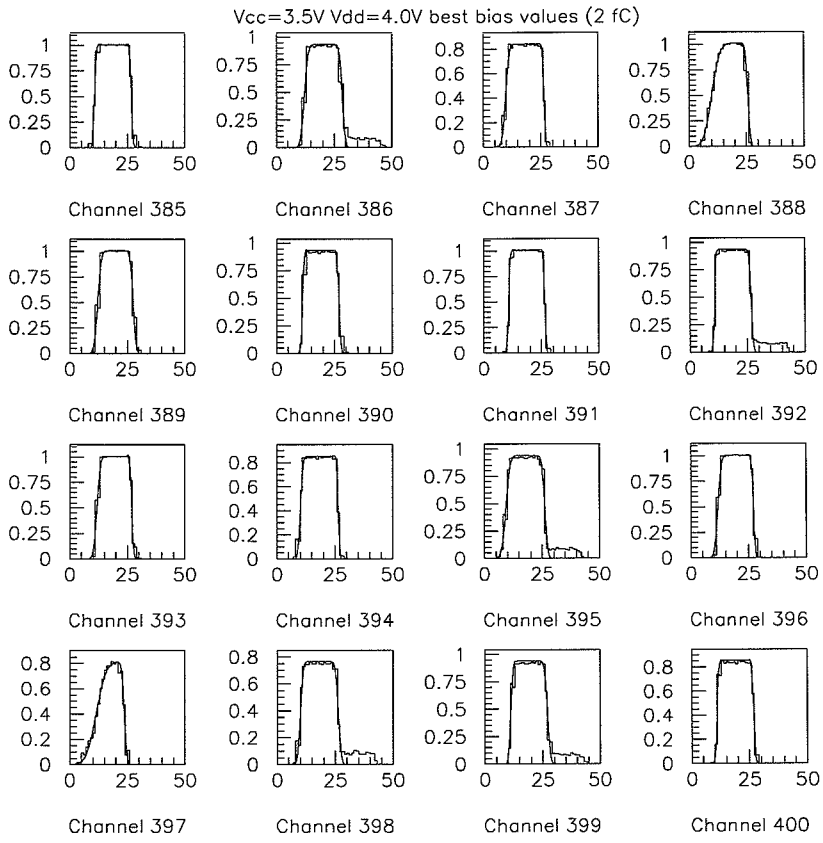


Figure 5.21: Strobe delay scans for the same channels

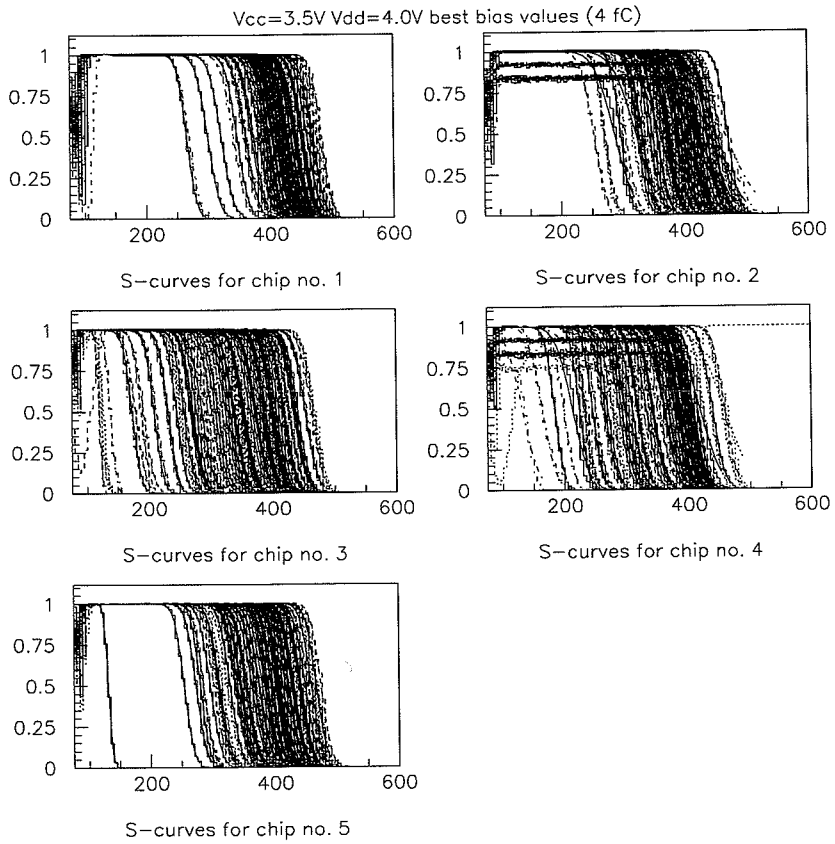


Figure 5.22: All channels plotted chip by chip

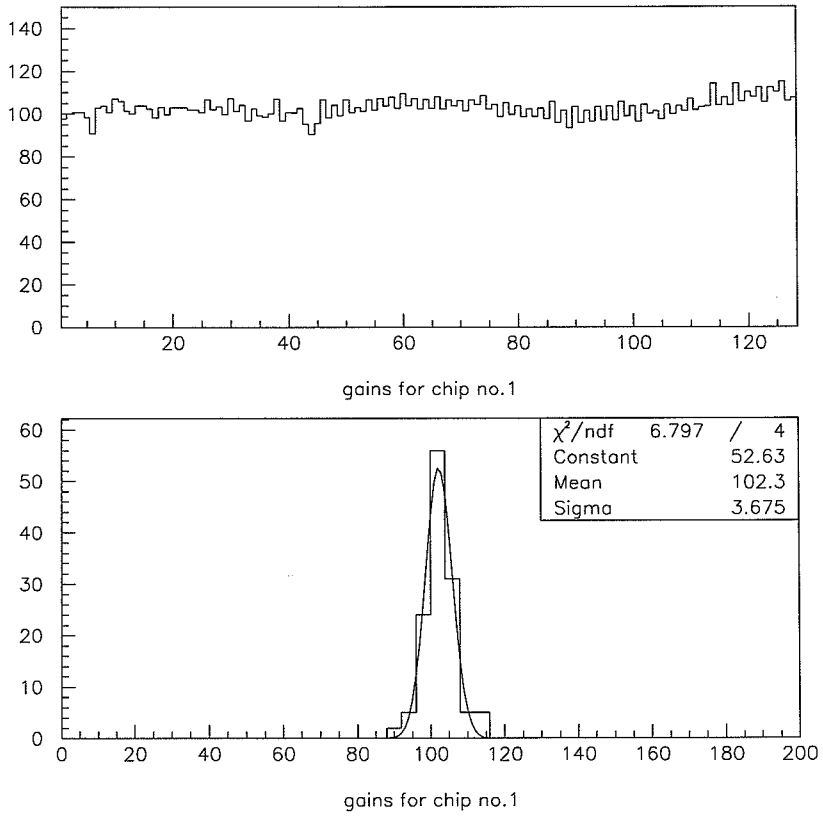


Figure 5.23: Gain distribution across the chip no.1 and its spread

Chip no	1	2	3	4	5	6
Mean of the gains (mV/fC)	102.3	98.21	109.9	97.79	101.9	101.5
Sigma of the gains	3.675	2.847	11.53	4.298	3.882	3.691
Spread of the gains	3.6%	2.9%	10.5%	4.4%	3.8%	3.6%
Means of the offsets	1.228	-1.555	-57.79	-31.39	-26.52	-21.04
Sigma of the offsets	27.5	41.21	46.85	42.58	39.97	41.65
Spread of the offsets	26.9%	42%	42.6%	43.5%	39.2%	41%

Table 5.3: Means and offsets for the 6 chips on the hybrid without the detector

that all chips but the third [16] were behaving very well (see fig. 5.23 for example). The gains were remarkably uniform across the chips. There is only the third chip which has a "hole" near its end. The gain was around 100 mv/fC, and its spread was 3.7%, less than twice the expected one[17]. However, concerning the offsets it was all the opposite [18]. The offset is too important and varies a lot from channel to channel (its spread reaches 39%, almost 10 times the expected one!). Hopefully Temic will be able to control better the process parameters and achieve better uniformity and lower offsets. The ENC is approximately 1000 e^-, so it stays under the 1400 e^- defined in the specifications, but the detector is yet to be bonded!

5.4.3 Measurements with the detector connected

Initial measurements

Finally the detector was bonded to the hybrid. Redoing the same measurements the results obtained were much worse than without the detector (see fig. 5.25). Actually they were so bad that there was impossible to do any fitting. Until a threshold of about 200 mV there is only noise! The explanation of what causes this problem came from an unlikely source: on the sixth chip there was some moisture on the bonding points of strips 664-674. So these strips were not bonded. Looking at the noise on these strips when the detector is at 0 V and at 100 V it seems that when the detector is biaised there are "hits" on the unbonded channels! The first thought was that the power supply used for biaising the detector was too noisy, so it was replaced by batteries, but nothing changed. Probably when biaising the detector, there is a loop forming between the detector and the chips, which injects to some extent the output of the amplifiers back to the strips, so there is an unwanted feedback. As it is shown on fig. 5.22 in chip no. 2 and no. 3 there are some channels that see practically 0 threshold when a 100 mV threshold is applied, so they will begin to oscillate. As fig. 5.26 shows this oscillation is not local to the channels, otherwise it wouldn't affect the unbonded strips. However, not only the oscillation spreads

[16] ???????? maybe show it

[17] In this calculation the 3^{rd} chip was omitted, as in the next ones.

[18] As it was also seen in earlier measurements.

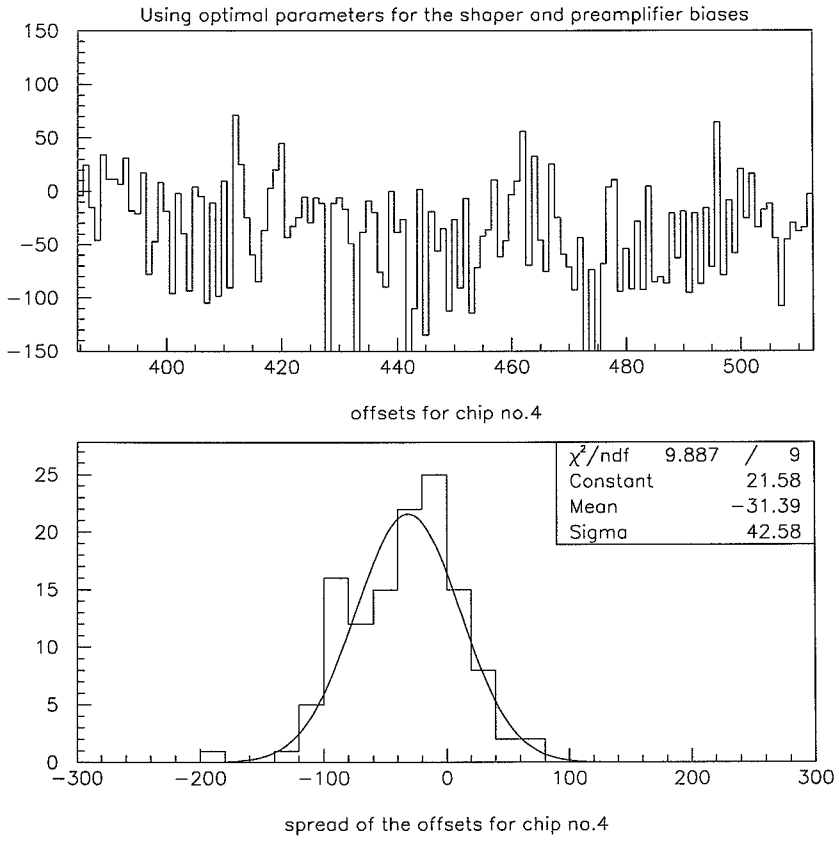


Figure 5.24: Typical offset values across a chip (chip no.4)

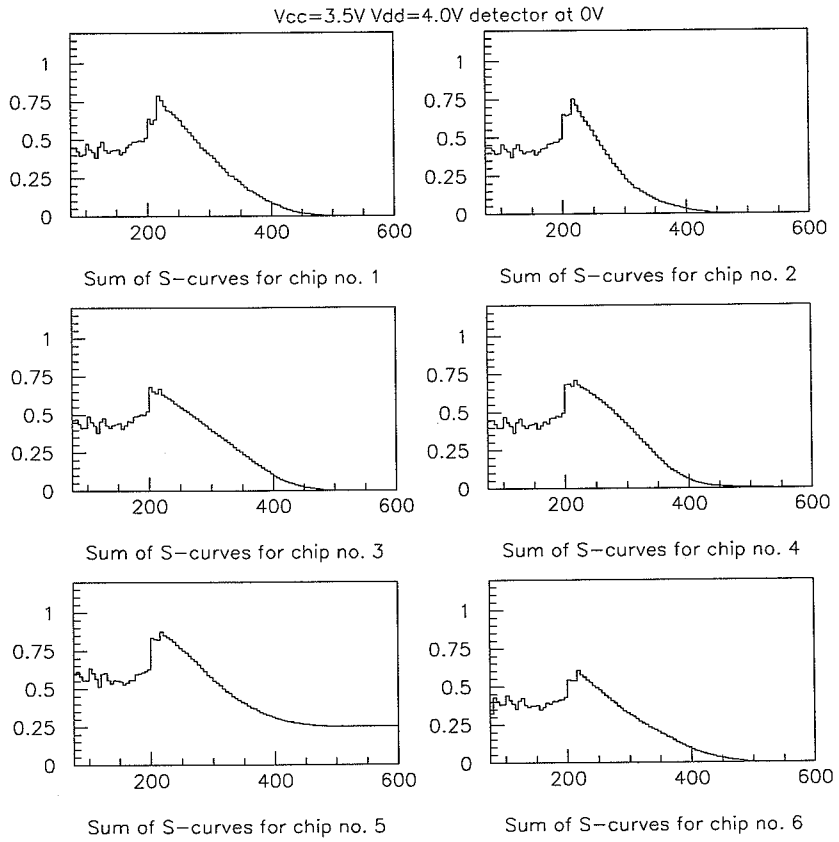


Figure 5.25: First results after bonding the detector (the best bias values were used)

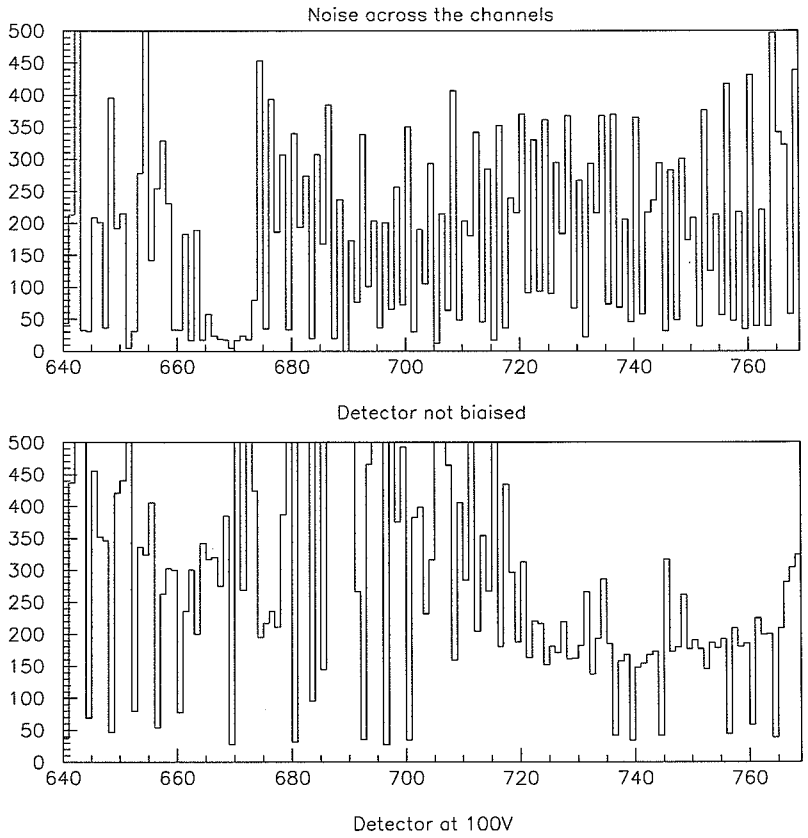


Figure 5.26: Biaising the detector gives rise to ghost hits

Chip no	1	2	3	4	5
Mean of the gains	85.57	79.28	??	78.93	80.18
Sigma of the gains	17.83	13.77	??	7.579	7.399
Spread of the gains	20.8%	17.4%	??	9.6%	9.2%
Means of the offsets	-57.13	-50.56	??	-18.59	-34.00
Sigma of the offsets	51.04	38.62	??	39.14	30.95
Spread of the offsets	59.6%	48.7%	??	49.6%	38.6%

Table 5.4: Means and offsets for 5 chips on the hybrid with the detector

Chip no	1	2	3	4	5
Mean of the gains	51.8	84.96	77.74	82.67	84.78
Sigma of the gains	13.37	8.91	9.497	13.56	3.289
Spread of the gains	25.8%	10.5%	12.2%	16.4%	3.9%
Means of the offsets	16.88	-42.53	-42.74	-78.97	-30.55
Sigma of the offsets	37.06	52.94	49.18	22.77	42.37
Spread of the offsets	71.5%	62.3%	63.3%	27.5%	50%

Table 5.5: Means and offsets for 5 chips on the hybrid with the detector and the digital and analogue grounds bonded together

over channels, but also over chips. Turning only one chip on by setting the threshold for the others to a very high value, it turned out that the results were much more like without the detector (see fig. 5.27).

In order to measure the relevant parameters the chips were turned on one by one. The first observation is that the gain is lower by 20% (this is expected due to the added capacitance represented by the strips). The next one is that the spreads are up significantly [19]. So is the noise which reaches 2315 e^-, hence it surpasses the value fixed in the specifications!

Measurements with analogue ground and digital ground connceted on the hybrid

An excellent idea was to reconsider the grounding scheme of the system. It was supposed to be a good idea to connect the analogue and digital ground on the hybrid. This way all the electrical components have their grounds in a well defined state. After making the corresponding bonds the results became much better (see fig. 5.30). However, they were still quite far from the specified values.

[19] For chip no.3 the fits even failed to converge.

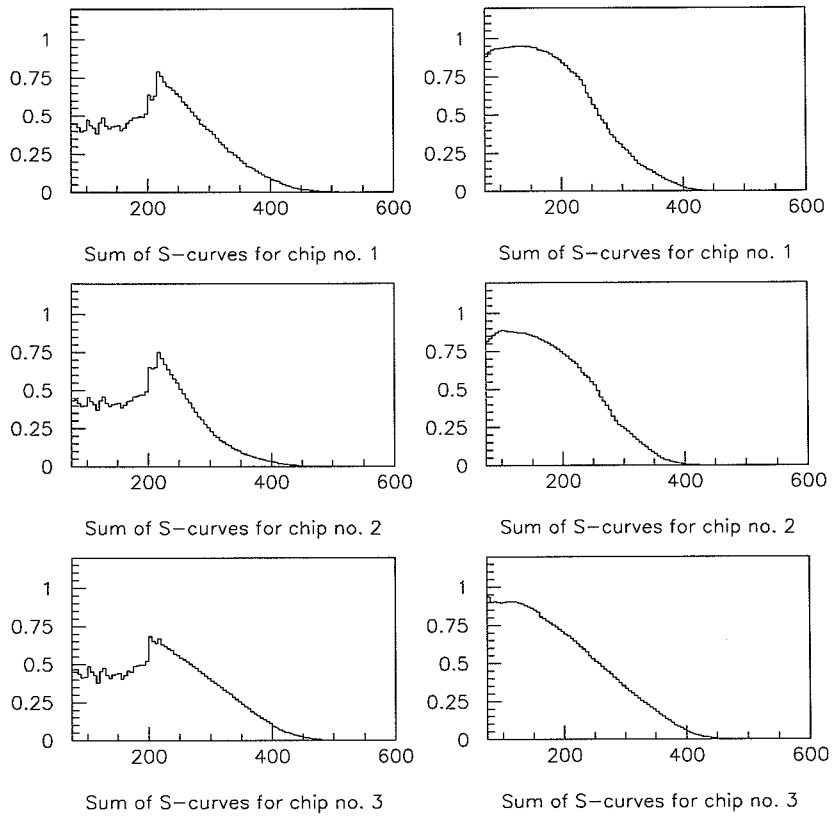


Figure 5.27: Comparing when all chips are on (on the left), and when only one (on the right)

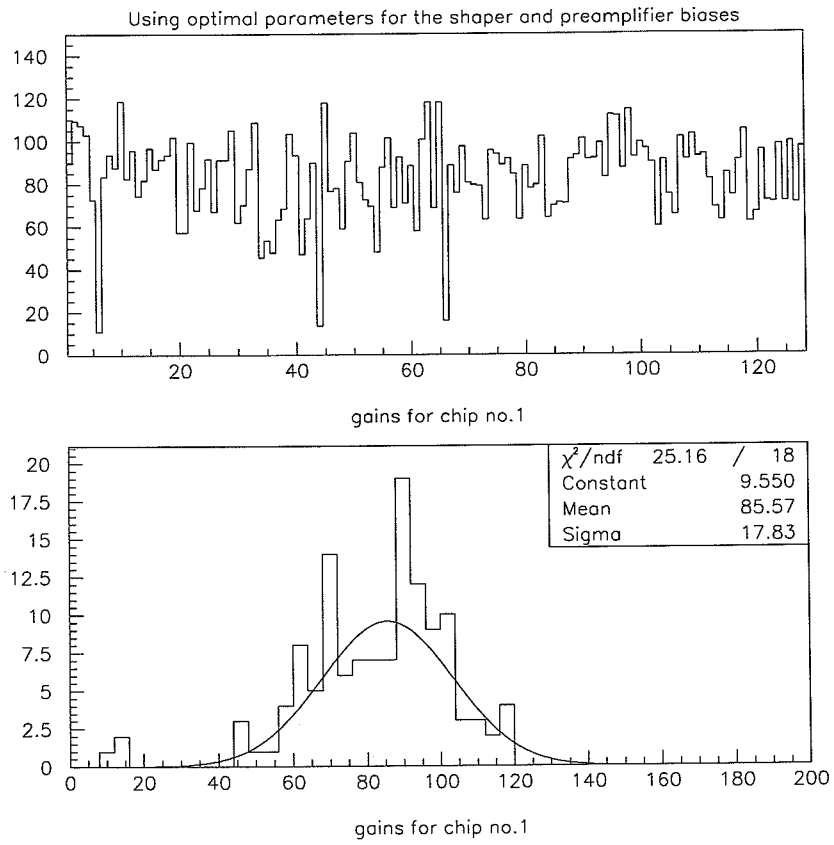


Figure 5.28: Gain distribution across the chip no.1 and its spread with detector on

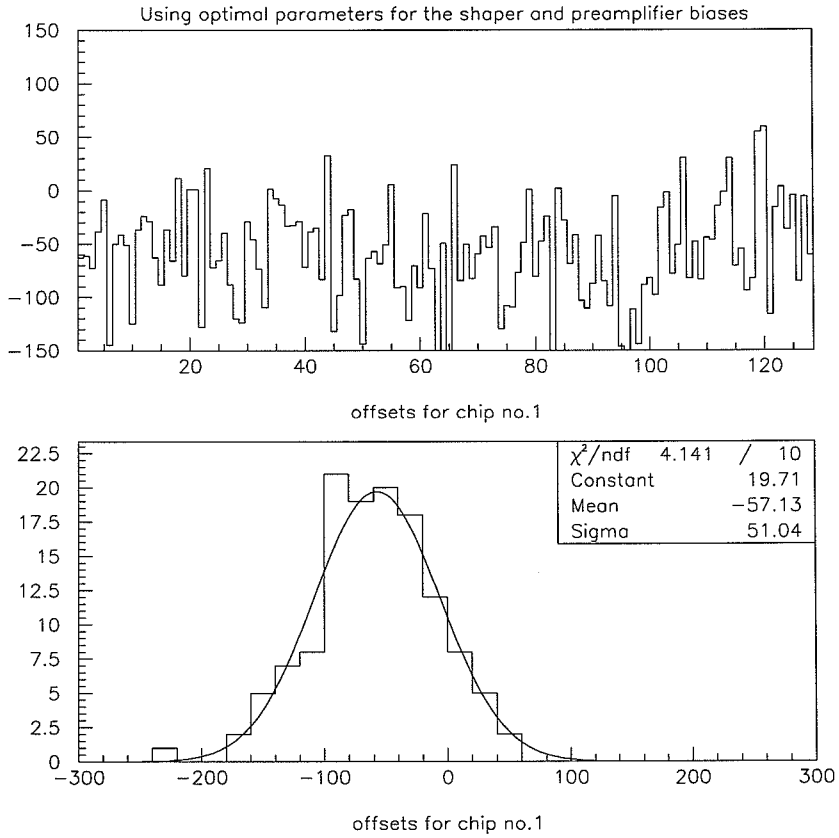


Figure 5.29: Offset distribution across the chip no.1 and its spread with detector on

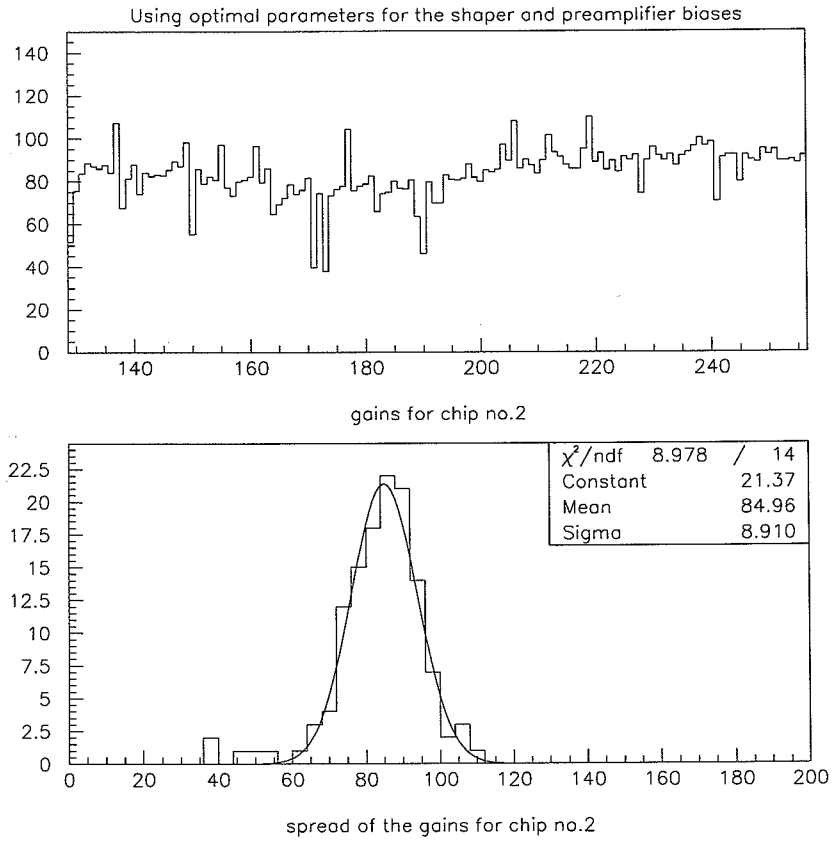


Figure 5.30: Gain distribution across the chip no.2 and its spread with detector on and the grounds connected

	Gain (mV/fC)	Spread of gains	Spread of offsets	ENC
Single chip on PCB	105	16%	17%	650
Single chip on PCB with baby-detector	??	??	??	??
6 chips on hybrid	100	3.7%	38.5%	1000
6 chips with detector (1 by 1)	81	14.25%	49.1%	2315
6 chips with detector and DGND-AGND connected	83	10.75%	50.775%	3700
Expected values	160	2%	4%	1400

Table 5.6: Resuming the main characteristics of the chip in the different measurements

5.5 Conclusions of the tests

The results of the measurements are resumed in table 5.6. It seems that it is really hard to get values matching the specifications. Of course, the main reason to that is that the company did not respect the agreed parameters. The low β lowered the gain, but it is not fully understood what caused exactly the deviation of the offsets from 0 and their extremely big spread. Hopefully the next set of wafers with the corrected process parameters will have a better behaviour, but it is clear that a lot more work needs to be done before giving green light to the mass production of the chip.

Chapter 6

Conclusions

ATLAS is one of the two general purpose *pp* experiments prepared for the Large Hadron Collider. The inner detector of ATLAS will be subject to high fluences of neutral and charged particles, and it must be still working reliably after several years of operation. Therefore, all components to be used in the inner detector have to be tested thoroughly before its construction.

The understanding of the ABCD chip is based on extensive tests in various conditions. In this paper, three major types of tests have been performed. The first involved a single ABCD chip on a PCB board. The second was a single chip on a PCB board connected to a baby-detector. Finally, the third major type was carried out on chips that were part of a fully populated module including a full-size detector.

In the first type of test, the chip was put on a PCB board designed specially for the tests. It was shown that the digital part works correctly apart from a few minor problems which will be corrected for the next batch. The gain was found to be lower than expected, around 105 mV/fC instead of 160 mV/fC. There was also an unexpectedly high spread in the values of offsets. These observations were later understood as being the result of the non-conformity of process parameters. The issue was discussed with the manufacturer, and the reprocessing of the chips has been agreed.

In the second...

In the third type of test, a hybrid was fully populated with chips and put on a detector. It was shown that connecting the detector caused an important degradation of the relevant parameters. For example, the gain was lower by 20%.

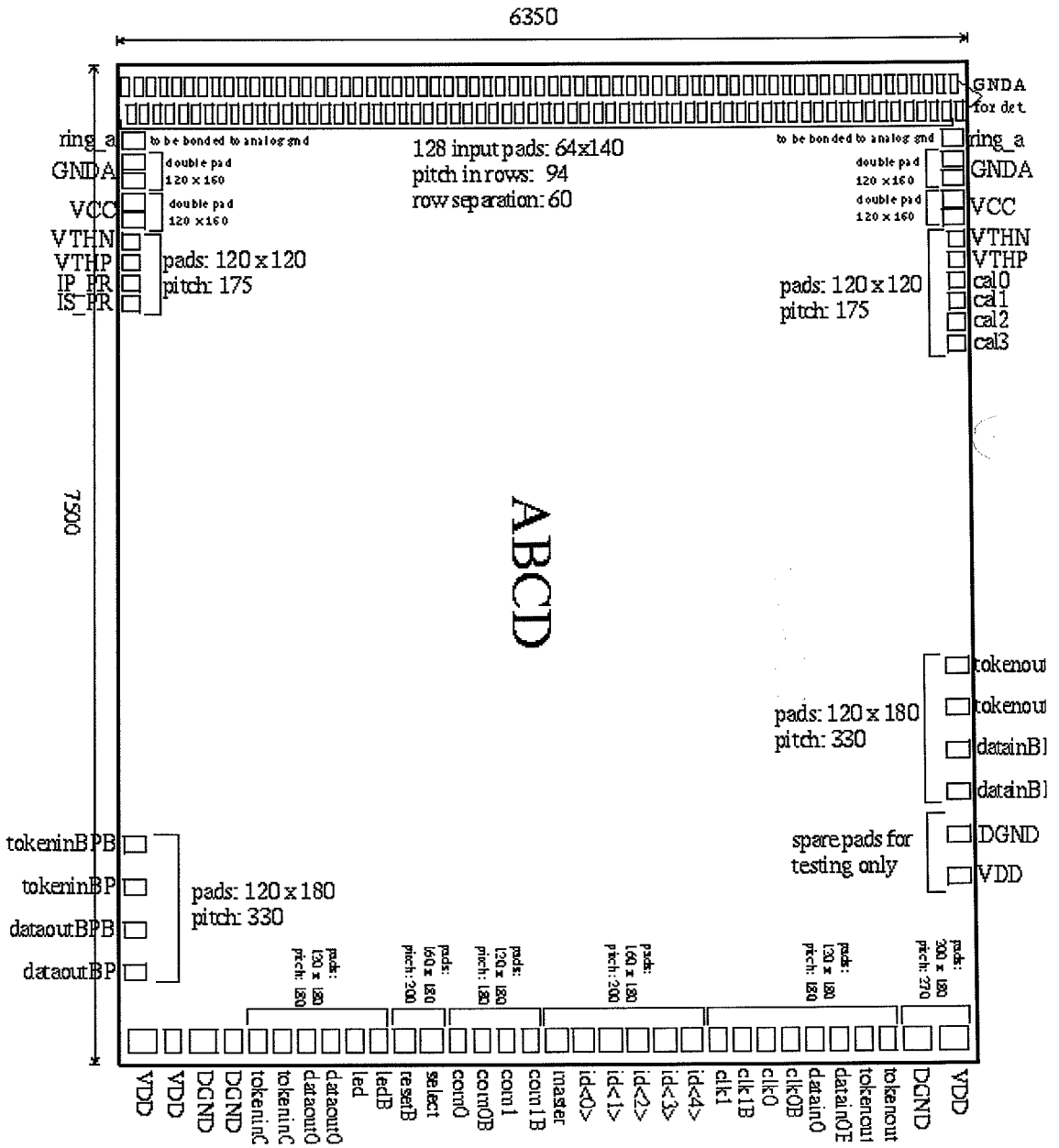
Overall, the results are promising. Hopefully, the reprocessed chips will satisfy the process parameter requirements, and show bigger gain, smaller offsets. A lot of measurements have been done, but many more need to be performed before the full-scale production can begin.

Chapter 7

Appendix

.1 Pinout of the ABCD chip

The die size is 6350 µm x 7500 µm.



1

.2 Slow control commands

Field 3	Field 4	Field 5	Field 6	Description
0001,1100	aaaaaa	000 000	dddd,dddd,dddd,dddd	Write to configuration register
1000,1100	aaaaaa	001 000	128 bits	Write to mask register
0001,1100	aaaaaa	010 000	dddd,dddd,dddd,dddd	Write to strobe delay register
0001,1100	aaaaaa	011 000	dddd,dddd,dddd,dddd	Write to threshold registers
0000,1100	aaaaaa	100 000	-	Pulse input register
0000,1100	aaaaaa	101 000	-	Enable data taking mode
0000,1100	aaaaaa	110 000	-	Issue calibration pulse
0001,1100	aaaaaa	111 000	dddd,dddd,dddd,dddd	Load bias DAC

Table .1: Control commands

Notations:

- aaaaaa = 6 bit chip address
- dddd = data value for register

.3 DC supply and control characteristics of the ABCD chip

	Pad name	Min	Nominal	Max	Absolute Max
Analogue supply	VCC	3.3 V	3.5 V	3.7 V	0 to 6 V
Analogue ground	GNDA		0 V		
Input transistor current	internal DAC	100 μA	200 μA	300 μA	
Input transistor current monitor	IP_PR	$V_{ip} = I_p \times 250\ \Omega$			
Shaper current	internal DAC	10 μA	15 μA	30 μA	
Shaper current monitor	IS_PR	$V_{is} = I_{sh} \times 250\ k\Omega$			
Discriminator threshold	VTHP	3.4 V	3.5 V	3.6 V	VCC
Discriminator threshold	VTHN		3.4 V		VCC
$(V_{THP} - V_{THN})$			0.1 V	0.9 V	0 to 2 V
Digital supply	VDD	3.5 V	4.0 V	4.5 V	0 to 6 V
Digital ground	DGND		0 V		

[1] to be compppleted!!!! colors, outputs

.4 Oslo-hybrid layout

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