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# THE TOF AND TRIGGER ELECTRONICS OF THE PAMELA EXPERIMENT FOR THE SEARCH OF PRIMORDIAL ANTIMATTER IN SPACE

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**Abstract**

The PAMELA experiment (a Payload for Antimatter Matter Exploration and Light-nuclei Astrophysics) is a space borne apparatus (which will be launched at the end of 2005 on board a Soyuz rocket) devoted to the study of the antiparticle component of cosmic rays. Its scintillator telescope system will provide the primary experimental trigger and time-of-flight particle identification.

## 1 Introduction

The PAMELA apparatus [1], following the general requirements to obtain particle identification, comprises essentially of a Transition Radiation Detector (TRD) as a $\beta$ selector, a magnetic spectrometer (characterized by a MDR of

800 GV/c) to measure particle's charge and momentum, an imaging calorimeter to discriminate at the level of $10^4 \div 10^5$ between electromagnetic and hadronic showers, and a Time-of-Flight (ToF) system with a time resolution of about 110 ps.

The Time-of-Flight system [2] of PAMELA is composed of several layers of plastic scintillators read out by photo-multiplier tubes. The ToF must provide a fast signal for triggering data acquisition in the whole instrument, measure the flight time of particles crossing its planes in order to derive their velocity $\beta$ and eventually reject *albedo* particles, and determine the absolute value of charge $z$ of incident particles through the multiple measurement of the specific energy loss $\mathrm{d}E/\mathrm{d}x$ in the scintillator counters. Additionally, segmentation of each detector layer in strips can provide a rough tracking of particles, thus helping the magnetic spectrometer to reconstruct their trajectory outside the magnet volume.

## 2 ToF electronics and trigger

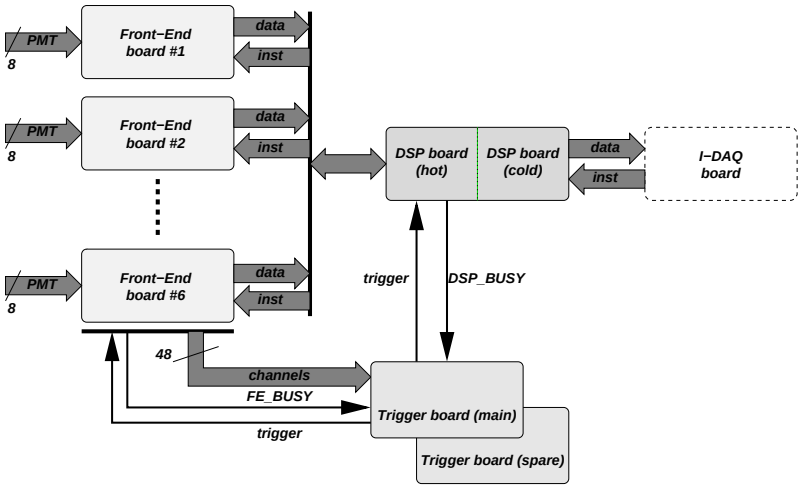


Figure 1: General ToF electronics layout.

The ToF and trigger electronics for PAMELA is a complex system made of nine boards in the 6U VME format. These are the six Front-End (FE) boards, the DSP board and the two identical trigger boards (one "hot", the other "cold"). The purpose of this system is to collect the signals coming from the 48 PMTs of the ToF, measure their arrival time with respect to the trigger pulse and their charge, generate the signals for the trigger, handle the busy

logic for all subsystems, and interfacing the ToF system with the general data acquisition system of the PAMELA apparatus.

The ToF electronics has to comply to the following requirements:

- guarantee a wide dynamic range in the charge measurement to allow the measurement of the energy release of $z > 1$ particles (up to carbon);
- add a negligible contribution to the overall ToF time resolution. This implies a contribution from time digitization which has to be less or equal than 50 ps.

In the mean time, the electronics must ensure a low power consumption, a high reliability and good radiation hardness. Generally speaking, the space environment is highly hazardous for our apparatus, both for the wide temperature ranges and the high doses of ionizing radiations, and since no replacement for defective components is possible once the satellite is in orbit, the issue of reliability of all the electronic devices is crucial for the survival of the instrument during the three years of expected mission lifetime. Therefore a great effort has been paid in implementing both hardware and software redundancy, that is to mean the replication of at least all critical components. An overall scheme of the ToF and trigger electronics is shown in Fig. 1.

### 2.1 Front End board

Each FE board receives the analog signals coming from 8 PMTs. For each channel the input is split in two branches, which are fed into the time and charge sections, respectively. The first section measures the arrival time of the signal with respect to the trigger pulse, and generates the signal for trigger formation. The other section measures the charge of the PMT signal.

*Time section*

For each PMT, the anode line is coupled to a fast discriminator. To minimize the time-walk effect, a double threshold discriminator has been chosen, mod. AD8611 manufactured by Analog Devices, which has a maximum propagation delay of 4 ns. Its two thresholds can be set by remote, each through a DAC. The discriminated signals are shaped, translated in the LVDS standard and sent to the trigger board. The discriminator is part of a more complex logic that controls a double-ramp Time-to-Amplitude-to-Time (TAT) converter. A low-loss, low-thermal drift, storage capacitor is charged with a high-stability constant current source during the time between the pulse edges of the FE discriminator signal and the trigger signal. The arrival time of the latter starts the discharging of the capacitor with a constant current which is about 200 times smaller than the previous. Hence, measuring the discharging time, a

time expansion factor of 200 is obtained. A fast discharge is produced if the trigger is not generated within 150 ns from the signal edge. The logic needed to control the TAT converter is fully implemented in a low-power, rad-tolerant FPGA, mod. 54SX08A manufactured by Actel [3]. Since each of these devices serves two channels, four of these FPGAs are mounted on the FE board.

*Charge section*

The amplitude of each PMT pulse is measured with a Charge-to-Time (CT) Converter. A charge amplifier collects the anode current from the PMT and provides an output signal which is proportional to the total current. A pulse stretcher operates by charging-up a capacitor at the peak value of the input waveform and then discharges it linearly. This signal has a length proportional to the maximum voltage reached on the capacitor and hence to the PMT charge. The last stage of the CT converter is a discriminator that generates the digital pulse with a length equal to discharging time of the pulse stretcher.

*Digital section*

The output digital signals coming either from the time of charge sections, are sent to a 100 MHz multichannel, common start, Time-to-Digital Converter (TDC), fully implemented in a FPGA, mod. 54SX32A manufactured by Actel. The circuit (realized with a 12 bits Gray counter and 8 registers) has a 10 ns resolution over a time window of 40.95 $\mu$s, which means (taking into account the time expansion factor) a 50 ps resolution on a 200 ns range. The first edge of the trigger signal starts the counter: when a new signal edge arrives at one of the channel inputs, the hit control logic writes the current value of the free running counter in its own register. The registers are 12+4 bits long to encode the channel number. Since each TDC receives a signal for measuring the time and one for the charge from each channel, the board houses two converters. The readout and the initialization of the TDCs is performed by a dedicated 54SX32A FPGA which acts as an interface between the FE and the DSP boards. Upon request from the DSP board it acquires data from the two TDC and writes them in a 16 hits-deep FIFO. Data are then serialized and transmitted according the Data-Strobe protocol at 16 Mbit/s.

## 2.2 DSP board

The readout of all PAMELA data is performed through a Data-Strobe serial link, with a dedicated link for each subsystem. To readout the six FE boards of the ToF subsystem an interface DSP board has been developed which collects the data from all the boards and transmit it, through the serial link, to the main

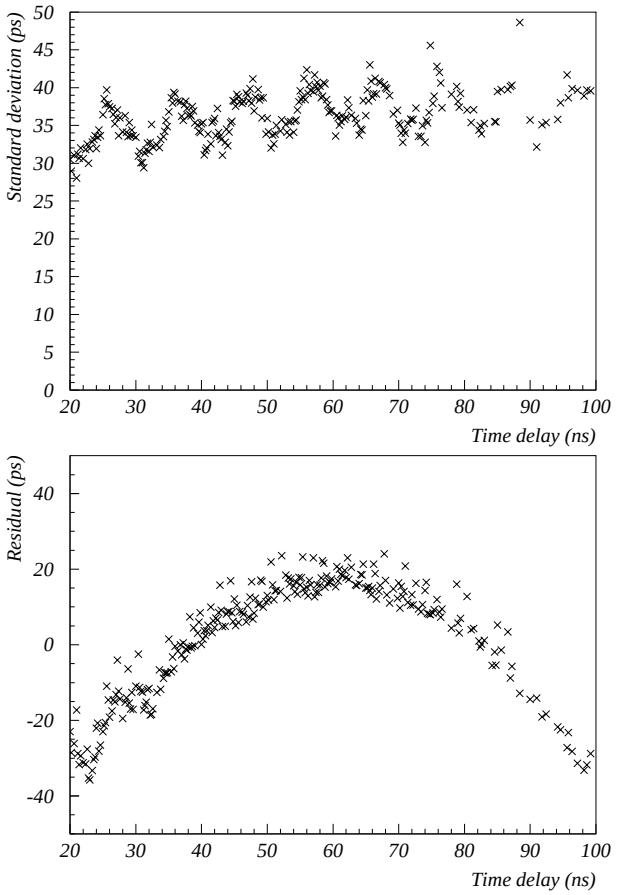


Figure 2: Results from the measurement of the integral nonlinearity.

DAQ. On this board is mounted a Digital Signal Processor (DSP), mod. ADSP-2187L manufactured by Analog Devices. The DSP collects the data and builds the data packet for the main DAQ. All the state machines needed to decode the macrocommands from the CPU of PAMELA and to control the interface with the DSP, are implemented on a 54SX32A FPGA. Another FPGA of the same kind controls the data flow with the FE boards. In order to increase the reliability of the system, two copies of this circuit are implemented on the same VME board: the "cold" version can be turned on if there is a failure of the "hot" one, thus preserving the full functionality of the board.

### 2.3 Trigger board

The trigger board is a complex digital board that generates the first level trigger for the apparatus and performs several more tasks. It receives the 48 signals from the ToF system for the main trigger and 8 signals from the other subsystems capable to generate self-trigger for particular events. To guarantee synchronization of the data acquisition the trigger board manages the 20 busy lines coming from each of the PAMELA subsystems. All the input and output lines are in the LVDS standard. About 60 rate counters, dead/live-time counters and the logic to generate calibration pulses sequence for different subsystem of the apparatus are also implemented on the board. The logic is distributed on 9 54SX32A FPGAs. Control masks select trigger types and allows the selection of failed (noisy or dead) ToF channels. The pattern of the channels fired for each trigger is generated for each event. A DSP (ADSP-2187L) is used to manage the data structure organization and to monitor the rate counters of the ToF channels and other subsystems.

## 3 Performance of the ToF electronics

Many tests of the performances of the ToF electronics has been made on the flight model of FE boards. Time resolution and integral nonlinearty have been mesured with a pulse generator, mod. 81132 manufactured by Agilent [4]. In Fig. 2 the results of two measurements are shown.

## References

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