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TECHNICAL SPECIFICATION
MONOLITHIC TRANSCEIVER
FOR FASTBUS CABLE SEGMENT—CSX*

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INTRODUCTION

These specifications describe a basic 5-channel differential transceiver integrated circuit. Several options are detailed to facilitate final design and configuration choices for this development. The relative preference of these options is given below:

Option	Description	Preference (Highest=1)
	4 mA Design	1
	6 mA Design	2
1.	Power Supply Extended Range	1
2. a	Current Select - Digital	2
2. b	Current Select - Analog	3
3. a	CSX/FPIO Fuse Programmable	1
3. b	CSX/FPIO Gate Programmable	2
4.	CSX/SIO Bonding Option	3

An example of preferred transceiver choices is:

- 4 mA output current for drivers
- 25 mV Input Sensitivity for receivers
- Extended power supply voltage ranges - (Option 1)
- Digital Current Select - (Option 2.a)
- CSX/FPIO Fuse Programmable - (Option 3.a)

The FASTBUS Cable Segment is part of ANSI/IEEE Standard 960-1986.

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1. Basic Specifications

All specifications shall apply over stated operating ranges for power supply voltages and ambient temperature.

a. Power Supply Voltages

Logic	VCCL = 5.0 V
Interface	VCCI = 5.0 V
	VEEI = -5.2 V

Option 1: Extended Operating range for interface supply voltages:

VCCI Range:	+5.0 V to +12.0 V
VEEI Range:	-5.2 V to -12.0 V

Note: Any significant increase of operating range limits above the nominal 5V values is considered useful. Supply voltages are permitted to be nonsymmetrical with respect to GND.

b. Power Supply Voltage Tolerance

Above and below nominal value or range:

± 5% Min.

c. Power Supply Input AC Rejection

Adequate power supply noise rejection is desirable to prevent erroneous CSX responses.

d. Leakage Currents

At differential I/O terminals for Logic 0, DISABLE or POWER-OFF states:

< 20 uA Desirable

< 40 uA Maximum

Minimizing leakage currents is of high prioriy.

e. Internal Capacitance

At differential I/O terminals:

< 10 pf Typical

f. Propagation Delay

Between differential and single-ended I/O terminals for either direction; from control inputs to any I/O terminal

< 15 nsec Typical

(Condition: RL = 50 Ohm, CL = 10 pf at differential I/O terminals; CL is parasitic capacitance from pcb traces, connectors, etc.)

g. Single-Ended I/O and Control

1. Inputs: 1 ALS TTL load equivalent
2. Data Outputs (Receiver/Buffer):

10 LS TTL loads equivalent, 3-state

h. Temperature Range - Operational

Standard Commercial 0 deg. - 70 deg. C Ambient

i. Overvoltage Protection

Overvoltage Protection for differential I/O terminals is desirable.

2. Differential Current Driver Specifications

a. Current Source and Sink Outputs

For Logic 1: $I = Is \pm 10\%$
where Is = 4 mA Desirable

Section 4 discusses applicable design trade-offs.

Option 2: Driver Current Control

1. First Preference: Digital Current Select input (ISEL) to double output currents.

2. Second Preference: Analog current program terminal requiring a single external component (resistor for example) for 5-channel transceiver.

b. Current Source-Sink Match
Matching Error for Logic 1:

$$\frac{|\text{ Diff Is }|\ \times\ 100\%}{\text{Is Av}} < 10\% \text{ Max.}$$

It is desirable to maintain this match also during output transitions.

c. Current Source Compliance Voltage Range

(VCC-1.0) V to (VEE+2.0) V Minimum
(VCC-0.5) V to (VEE+1.0) V Desirable

d. Current Sink Compliance Voltage Range

(VEE+1.0) V to (VCC-2.0) V Minimum
(VEE+0.5) V to (VCC-1.0) V Desirable

e. Output Transition Times

10 ns > TR, TF > 5 ns Typical
(Load RL=50 Ohm, CL=10 pf)

f. Output Disable
Transceiver Disable controls must be effective during power supply On-Off transitions and keep driver outputs in Hi-Z state.

3. Differential Receiver Specifications

a. Differential Input Sensitivity VDI

Defines minimum input signal including offset voltage for which output reaches proper logic state at specified propagation delay.

$$< \pm \text{ VDI Minimum}$$
$$< \pm \text{ VDI Desirable}$$
$$\text{where VDI} = 50 \text{ mV Minimum}$$
$$= 25 \text{ mV Desirable}$$

The allowable design range and applicable trade-offs are discussed in Section 4.

b. Input Hysteresis

$$\pm 10\% \text{ VDI Desirable}$$

c. Common Mode VCM Voltage Range

$$| \text{VCM} | > 1/2 \text{ (VCC-VEE)} - 2.0 \text{ V Mininimum}$$
$$> 1/2\text{(VCC-VEE)} - 1.0 \text{ V Desirable}$$

d. Common Mode Noise Rejection

Receiver should reject common mode signals including pulses within its VCM range over its entire signal bandwidth.

e. Differential Input Voltage VDI Range

$$\text{VDI Range: (VCC-VEE) -2.0 V to -2.0 V Minimum}$$
$$| \text{VDI} | > \text{(VCC-VEE) V Desirable}$$

f. Output Transition Times

$$\text{TR,TF} < 5 \text{ ns Typical}$$
$$\text{(Load CL} = 50 \text{ pf)}$$

4. Design Trade-Offs

The range of trade-off possibilities of output currents and voltage compliance for the driver, input sensitivity for the receiver are illustrated by two examples:

a. Low-Level Example

Driver Current (Item 2.a): Is = 4 mA
Receiver Input Sensitivity (Item 3.a):

VDI = 50 mV Minimum
VDI = 25 mV Desirable

This is considered the low-level limiting specification. It is also the preferred specification.

Advantages:

- For multiple drivers on bus, the driver compliance voltage limits are relaxed.
- Chip power dissipation is low.

Disadvantages:

- Small signal-to-noise ratio on bus.
- High input sensitivity for receiver.
- Receiver requires higher gain resulting in reduced speed.

b. High Level Example

Driver Current (Item 2.a): Is = 6 mA
Receiver Input Sensitivity (Item 3.a):

VDI = 75mV Minimum
VDI = 50 mV Desirable

This is considered a high level limiting specification due to multiple driver requirement.

Advantages:

- Improved S/N ratio.
- Reduced gain and sensitivity requirements for receiver.

Disadvantages:

- Higher driver compliance limits required.
- Higher power dissipation.

5. Quint Transceiver Chip Block Diagram and Packaging

The proposed package for a 5-channel transceiver is a Plastic Leaded Chip Carrier package with 28 leads (PLCC28 JEDEC Standard MO-047AB).

a. CSX/BIO Bussed I/O Transceiver

The basic quint transceiver is shown in Figure 1.A. Package pin-out and control input descriptions are given in Figure 1.B. BIO refers to bi-directional, bussed single-ended I/O connections (SBi) for the first 4 channels.

b. Option 3 - CSX/FPIO Field Programmable I/O Transceiver

This design utilizes field programmable fuses and/or gating logic to allow user choice of Bussed I/O or Split I/O CSX configurations.

- Option 3.a: CSX/FPIO Fuse Programmable

  Choice of CSX/BIO or CSX/SIO configuration is by means of field programmable internal fuse links. The block diagram is shown in Figure 2.A; pin-out and control descriptions for BIO/SIO configurations are detailed in Figure 2.B.

- Option 3.b: CSX/FPIO Gate Programmable

  Choice of BIO or SIO configurations is by means of gating and buffer logic. A single internal fuse link controls the gating logic. Figure 2.C illustrates this option. If no fuse link is implemented, the use of one package pin for control is possible. This is a less desirable approach, since the ENDR5 input will be sacrificed.

c. Option 4: CSX/SIO Package Bonding Option

This option employs alternate bonding connections from chip to PLCC package to produce a CSX/SIO transceiver (Figure 2.D). A bonding connection from GND to the control logic block changes the control inputs from BDIR and BEN* to ENBREC and ENBDR*. The transceiver chip remains the same as in Part 5.a for the CSX/BIO.

6. Option 5: Quint transceiver for ECL

This option specifies a companion transceiver design with 10K ECL compatible single-ended I/O and control input connections. All other specifications remain the same as in Sections 1 to 5 above.

Implementation of TTL and ECL compatibility on the same chip, with selection made by fuse programming or by bonding option, is a highly desirable feature.

List of Figures

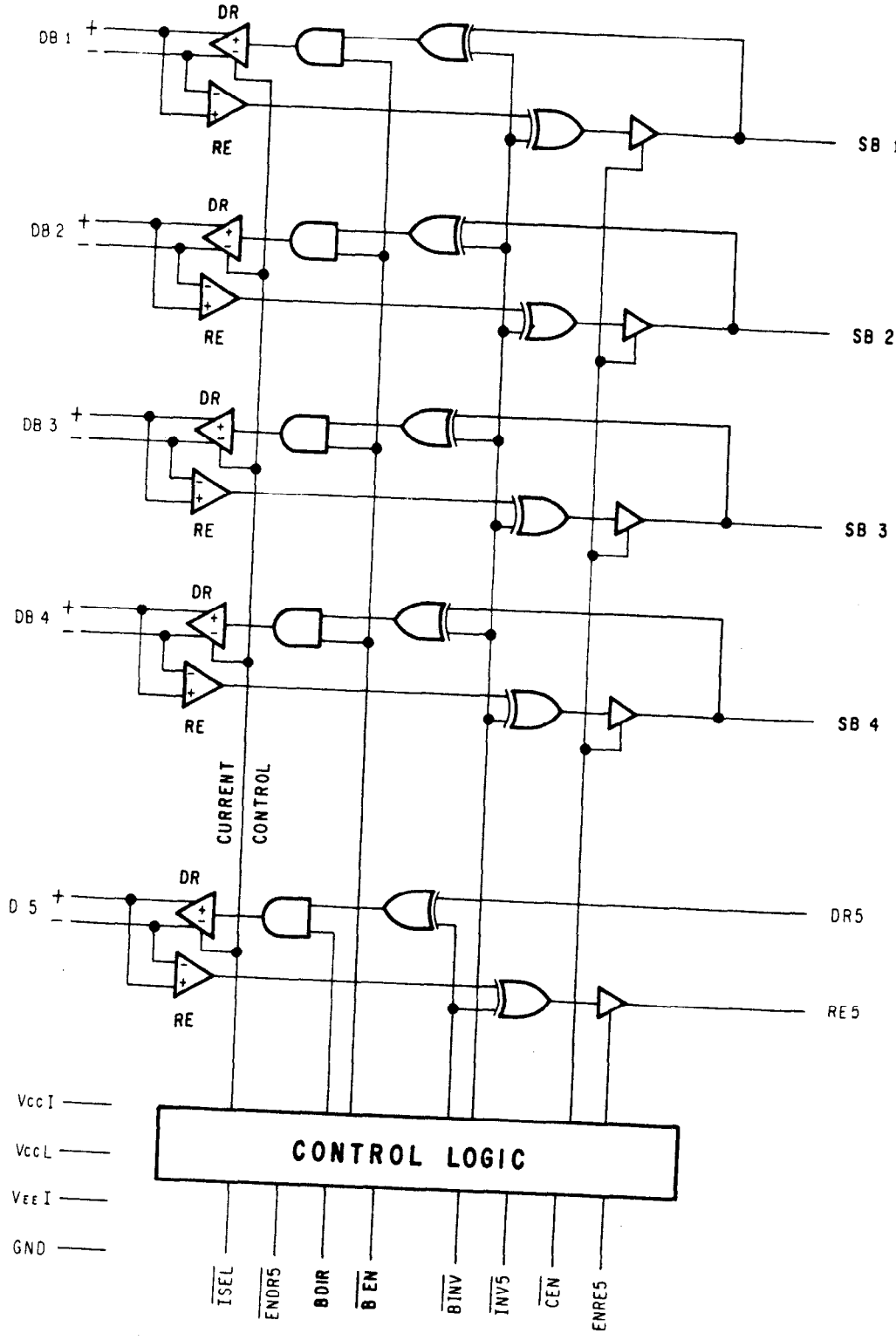

FIG. 1A — CSX/BIO BUSSED I/O TRANSCEIVER

12-86 VKI 1

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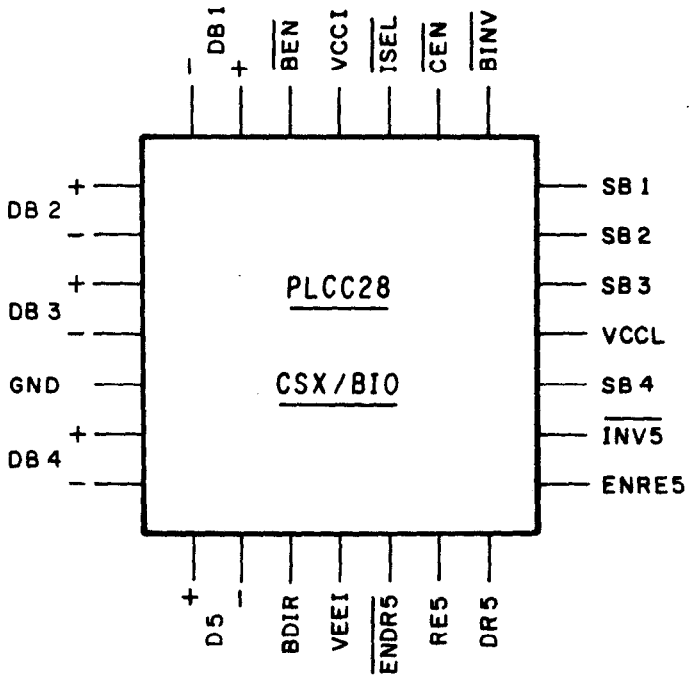

DBi – Differential Bus I/O Terminals
SBi – Single-End Bus I/O Terminals
DRi – Current Driver Inputs
REi – Receiver Outputs

CSX/BIO FUNCTION TABLE			
	L	H	DESCRIPTION
$\overline{ISEL}$	2IS	IS	DRIVER CURRENT CONTROL
$\overline{CEN}$	EN	DIS	ALL DR AND RE OUTPUTS
$\overline{BEN}$	EN	DIS	DR 1-4 AND RE 1-4 OUTPUTS
BDIR	$\frac{SBi \rightarrow}{DBi}$	$\frac{DBi \rightarrow}{SBi}$	BUS DIRECTION CONTROL
$\overline{BINV}$	$\frac{SBi =}{DBi}$	$\frac{SBi =}{DBi}$	BUS INVERT CONTROL
$\overline{INV5}$	$\frac{RE5 =}{\overline{DR5}}$	$\frac{RE5 =}{DR5}$	DR5, RE5 INVERT CONTROL
$\overline{ENDR5}$	EN	DIS	DRIVER 5 OUTPUT
ENRE5	DIS	EN	RE 5 OUTPUT
All control inputs have on-chip pull-ups to Logic = H level.			

FIG. 1B – CSX/BIO PIN-OUT AND FUNCTION TABLE 12-86 VKI 6

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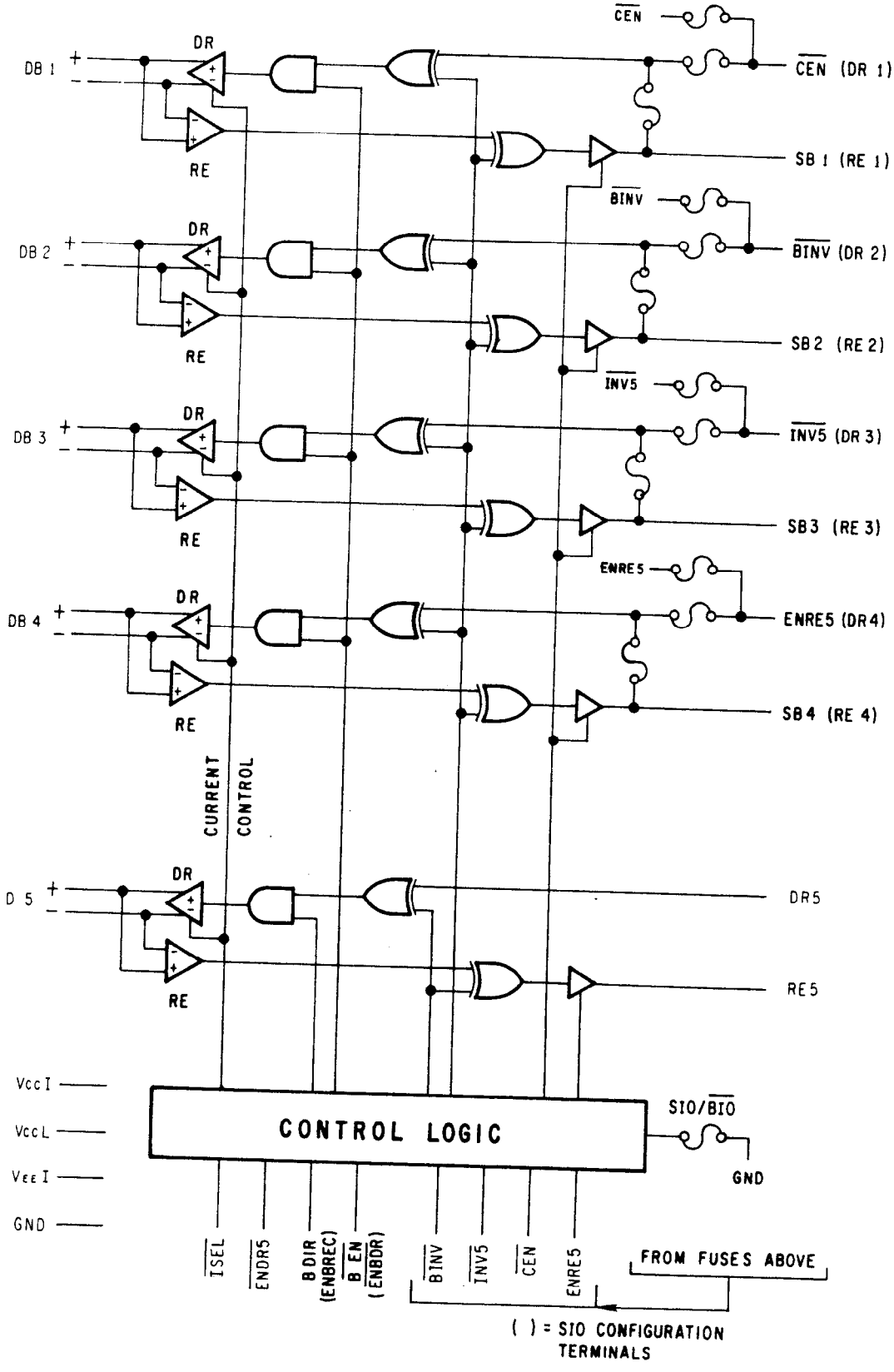

FIG. 2A – CSX/FPIO FUSE PROGRAMMABLE TRANSCEIVER

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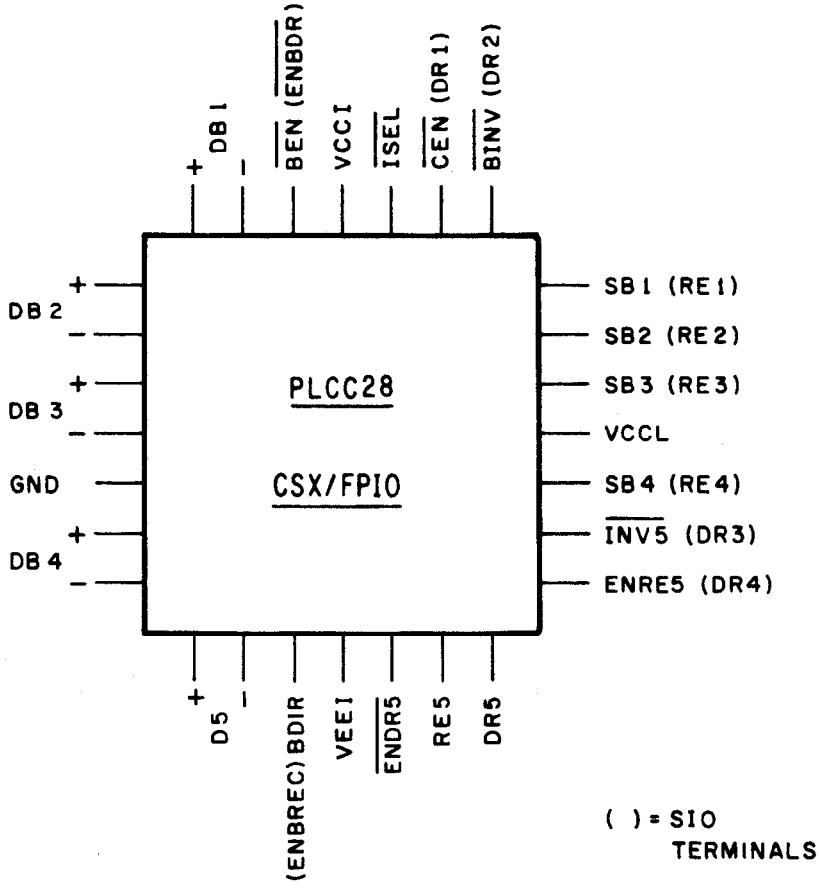

DBi – Differential Bus I/O Terminals
SBi – Single-End Bus I/O Terminals
DBi – Current Driver Inputs
REi – Receiver Outputs

CSX/SIO FUNCTION TABLE			
	L	H	DESCRIPTION
$\overline{\text{ENBDR}}$	EN	DIS	DR1-4 OUTPUTS
ENBREC	DIS	EN	RE1-4 OUTPUTS
Other SIO functions and all BIO functions as in FIG.1B. All control inputs have on-chip pull-ups to Logic = H level			

FIG. 2B– CSX/FPIO PIN-OUT AND FUNCTION TABLE 12-86 VK1 5

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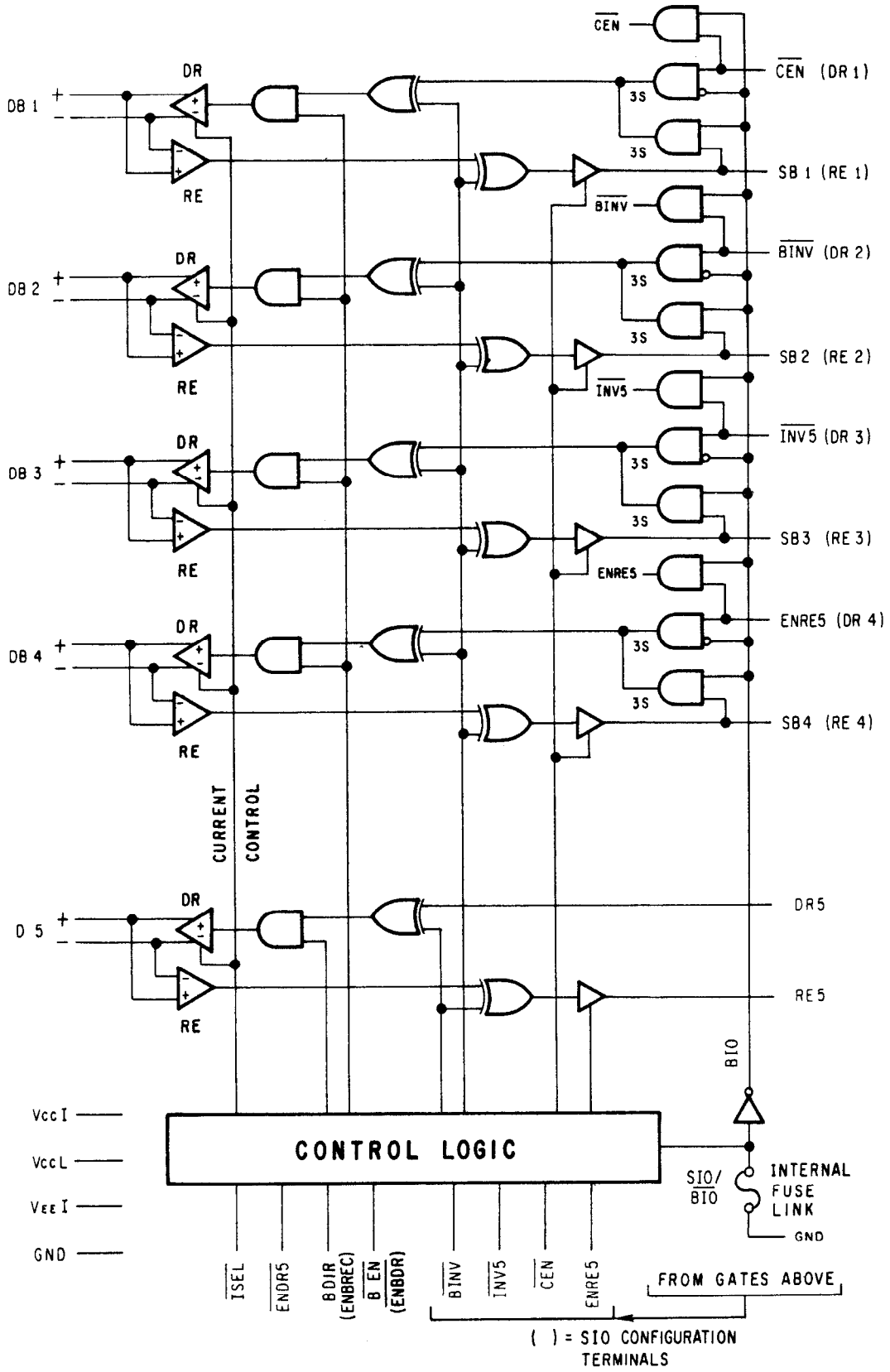

FIG. 2C – CSX/FPIO GATE PROGRAMMABLE TRANSCEIVER

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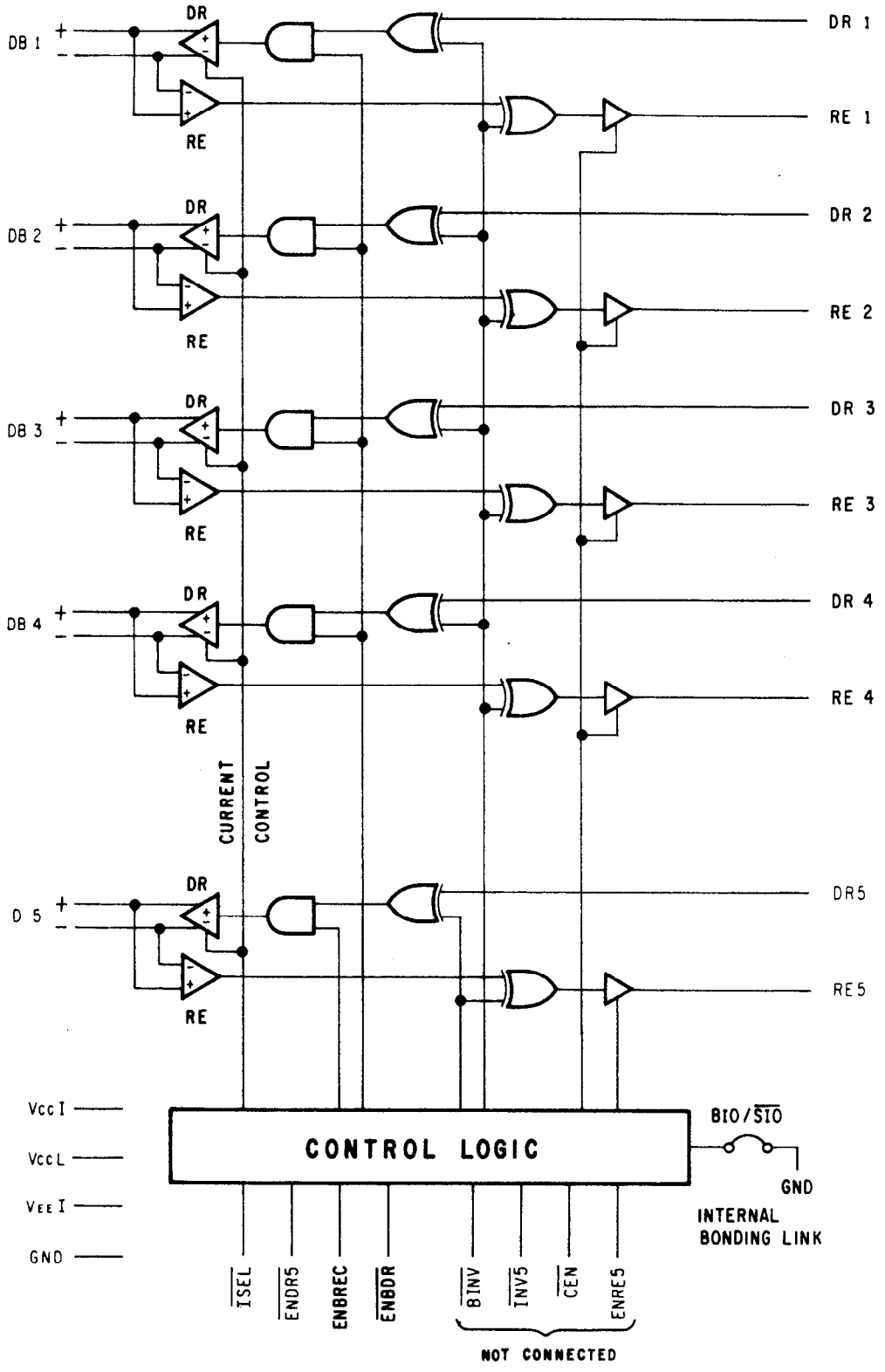

FIG. 2D— CSX/SIO TRANSCEIVER BONDING OPTION

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