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DØ Silicon Tracker Technical Design Report

DØ Upgrade Collaboration

July 1, 1994

Contents

Chapter 1

Overview and Physics Motivation

1.1 Introduction

DØ was designed with the goals of efficient identification of leptons and jets over a wide rapidity region. This was achieved by using fine grained, hermetic electromagnetic and hadronic calorimetry, muon detection using thick magnetized iron, and non-magnetic inner tracking. Over changing running conditions and detector technology, we have tried to maintain our basic philosophy of full coverage for lepton and jet identification. The DØ upgrade (Fig. 1.1) extends the capability of the detector to include track momentum determination and vertexing while maintaining angular coverage to $\eta = \pm 3$. In addition to the silicon tracker discussed in this report the upgrade includes:

- A 2 Tesla superconducting solenoid magnet
- Four superlayers (*xuvx*) of scintillating fiber tracking
- A preshower detector surrounding the solenoid
- New muon system and calorimeter electronics
- Improvements to the trigger and DAQ systems

In this way DØ can continue to address a wide range of collider physics topics into the next century.

1.2 Physics Goals

Over the next decade the collider program is likely to have a dual emphasis: top and high-p_t physics, as well as lower p_t beauty and QCD physics. The two kinematic regimes impose different demands on the detectors. Our silicon tracker design represents a compromise between these two regions.

A wide range of studies have been performed on the physics capabilities of the upgraded DØ detector [1, 2, 3, 4, 5] addressing a range of physics topics. We summarize here some of the physics topics which drive the design.

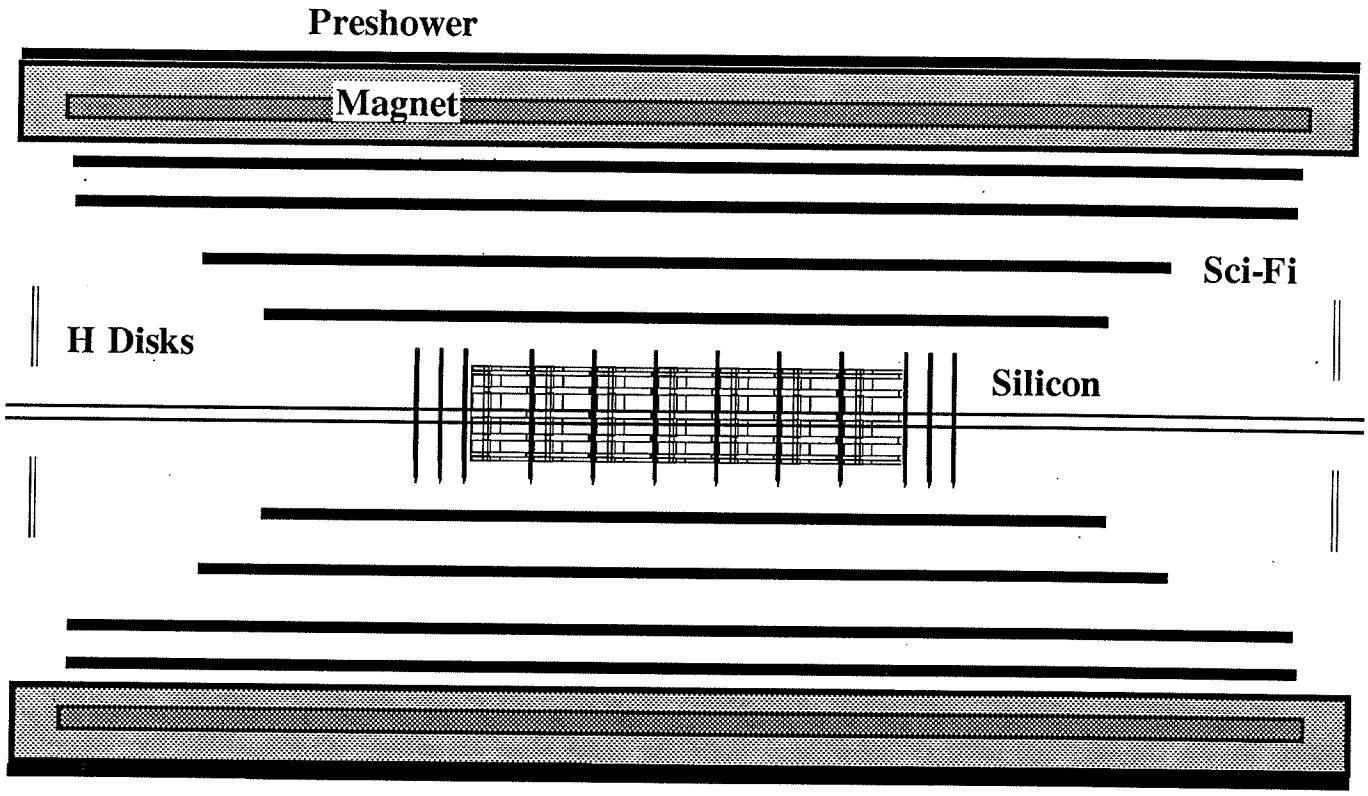

Figure 1.1: The DØ Upgrade detector

1.2.1 Top Physics

The primary role that the silicon tracker will play in top physics is b-jet identification. In the standard model top quarks will decay primarily through the $t \rightarrow Wb$ mode. Backgrounds include $W + jet$ and QCD events. W's can decay to leptons or jets, with a small fraction of b-jets. The detector will be asked to:

- Separate $t\bar{t} \rightarrow lepton + b\bar{b} + W(\rightarrow 2\ jets)$ from the background process $W \rightarrow lepton + 4\ jets$.
- Identify the b-jet in top events to reduce combinatorics in top quark mass calculations.
- Identify electrons, muons, and tau leptons from both b and W decay.

Top jets are the most challenging environment for the DØ tracking system. The very high top mass implies dense, collimated jets of particles at low values of rapidity. These considerations drive us to a redundant system in the central rapidity region with multiple layers and small angle stereo.

1.2.2 Beauty Physics

The Tevatron collider is a copious source of B mesons and b physics is likely to become an increasing focus of DØ as we gain the ability to reconstruct track momenta and vertices. B physics differs markedly from high-p_t physics in that the emphasis is on high rates, low to moderate p_t, and large angular coverage. Figure 1.2 shows the rapidity and momentum distributions of B mesons at the Tevatron.

DØ's b physics goals will include CP violation in a "standard" mode, such as $B \rightarrow \psi K_s$, as well as modes which e^+e^- B-Factories will find difficult, such as B_s mixing. Our superb lepton identification over $\eta = \pm 3$ is crucial to DØ's b physics plans. For b physics the detector will be asked to:

- Find vertices in three dimensions with good proper time resolution.
- Fully reconstruct multi-prong charm and beauty decay chains.
- Tag "partner" b decays using leptons, vertex reconstruction, or charm identification.
- Trigger on b candidate events using track impact parameters and lepton identification.

It is clear from Fig. 1.2 that forward acceptance is crucial for b physics. The need for full coverage becomes more apparent when one considers that a tag on the partner b, which may be separated in rapidity, is necessary for b physics studies such as mixing and CP violation. The crucial parameter in B_s mixing studies is lifetime resolution, which translates almost directly to a requirement on vertex resolution.

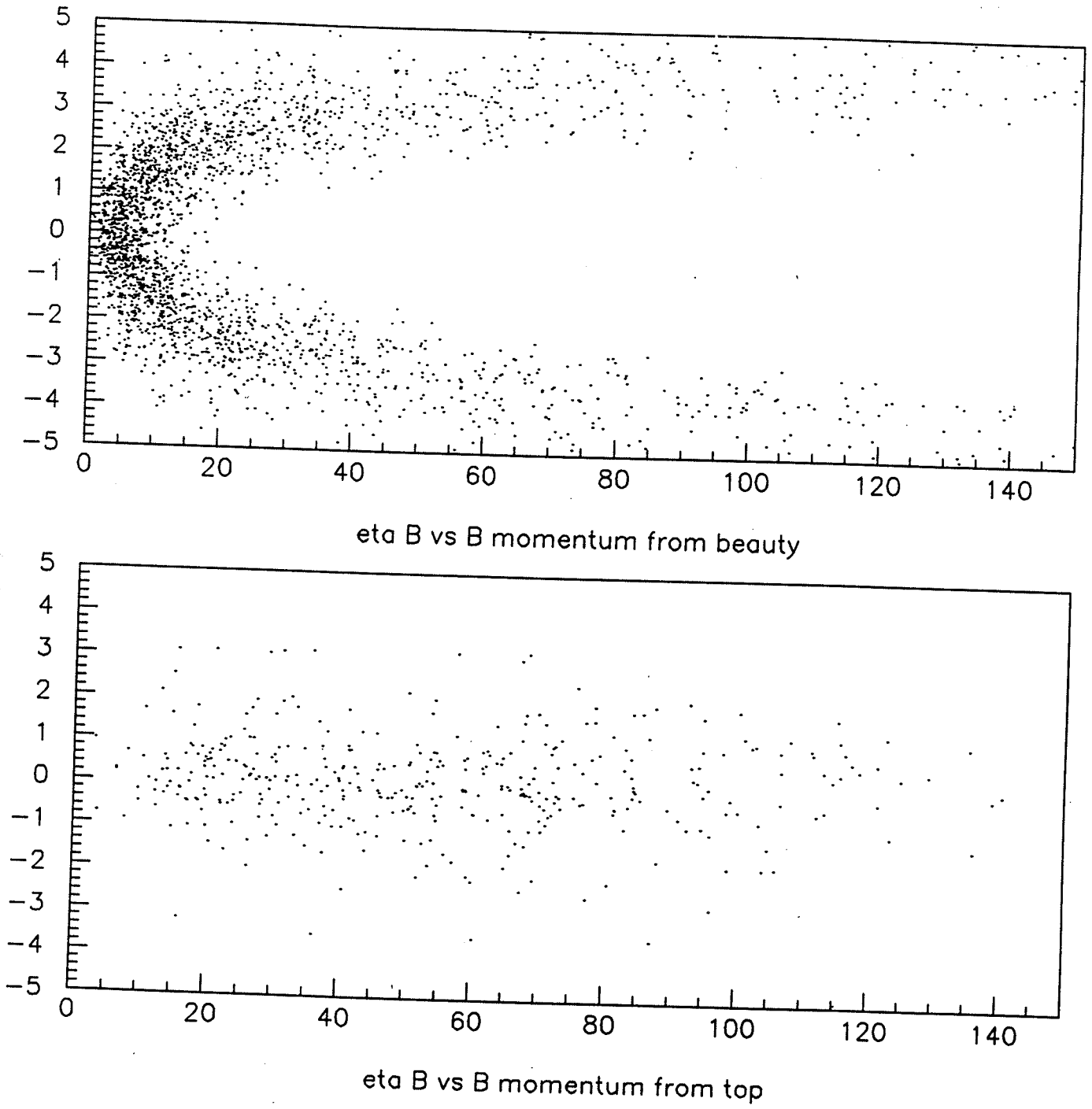

Figure 1.2: Rapidity and momentum distributions of B mesons produced directly and by the decay of 140 GeV/c^2 top quarks at the Tevatron.

1.3 Tevatron Parameters

The upgraded Tevatron in Run II is expected to have the following parameters:

- Interaction region length of $\sigma_z \approx 25\,\text{cm}$.
- Luminosity of $10^{32}\,\text{cm}^{-2}\text{s}^{-1}$.
- Crossing interval greater than or equal to 132 ns.
- Beam transverse sigma of less than $50\,\mu\text{m}$.

Some of these parameters are expected to vary over the lifetime of the detector, for example the Run IIa crossing interval may be 396 ns, changing to 132 ns in Run IIb.

Each of the machine parameters has an effect on the silicon design. The luminosity sets a scale for the radiation damage expected over the life of the detector, which in turn dictates the operating temperature (see Section 2.3). The long interaction region length sets the length scale, and motivates our disk/barrel design. The crossing interval sets the design parameters for the electronics and readout as well as the probability that multiple interactions occur in a single crossing. Finally the small beam radius compared to a typical B track impact parameter of $300\,\mu\text{m}$ means that fast impact parameter triggers can be contemplated.

1.4 DØ Silicon Tracker Design

1.4.1 Overall Design

The basic philosophy of the DØ silicon tracker is to maintain track and vertex reconstruction over the full η acceptance of DØ. This task is complicated by the Tevatron environment. In a machine with a point source luminous region the IP could be surrounded by detectors in a roughly spherical geometry. This would allow all tracks to intersect the detector planes at approximately normal incidence and provide optimal resolution. The Tevatron IP has a σ_z of 25 cm. In this situation it is difficult to deploy detectors such that the tracks are generally perpendicular to detector surfaces for all η. This forced us to a hybrid system, with barrel detectors measuring primarily the r-ϕ coordinate and disk detectors which measure r-z as well as r-ϕ. Thus vertices for high η particles are reconstructed in three dimensions by the disks, and vertices of particles at small values of η are measured in the barrels.

The interspersed barrel-disk design is shown in Fig. 1.3. In such a system the disk separation must be kept small to minimize extrapolation errors. However, each plane of disks also represents a dead region between the barrels which lowers the overall efficiency of the detector. Thus there is a compromise between vertex resolution at large η (1/disk spacing) and efficiency at small values of η.

This design clearly puts a premium on a minimal gap between barrel sections. In our design this gap is minimized in several ways:

1. Inboard mounting of the electronics. The readout electronics and their supports are mounted on top of the active detector surface. This means that extra inter-barrel space is not needed for "ears".

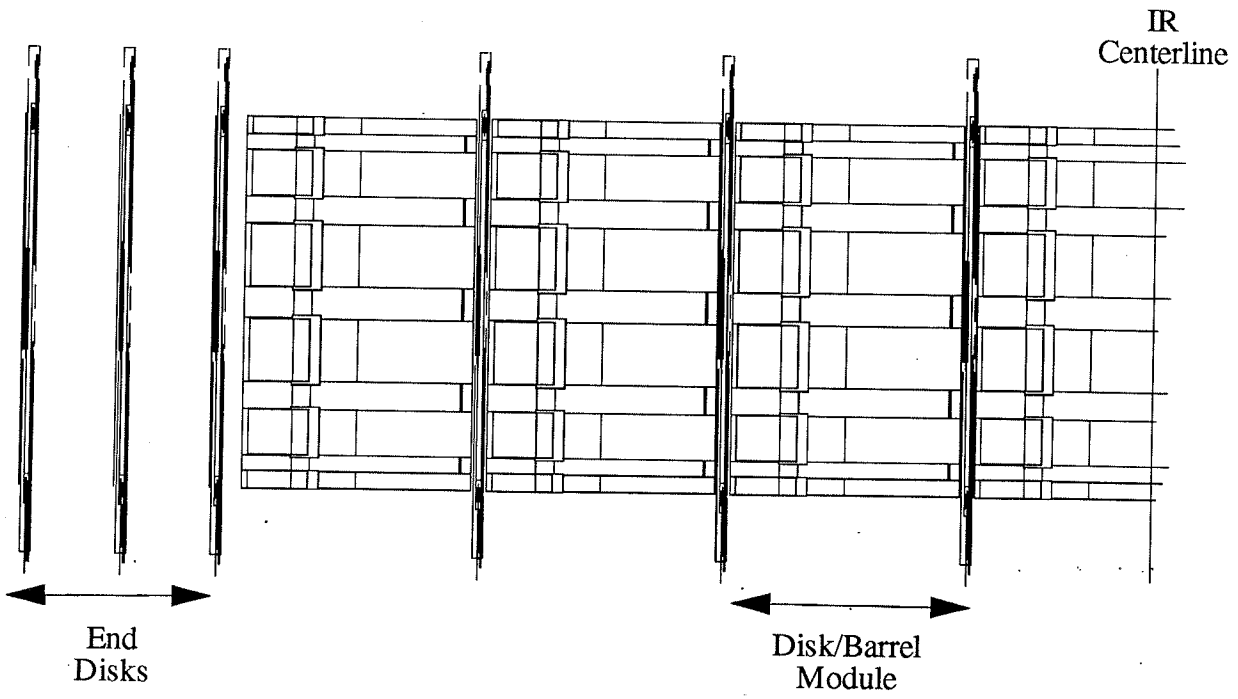

Figure 1.3: DØ silicon tracker interspersed barrel-disk design

2. Inboard routing of cables. Cables which supply power, control, and readout bus signals are routed to the outer radius between detector layers rather than off the ends of the ladders.

3. Thin disk modules. The disk detectors are designed to be as thin as possible consistent with mechanical rigidity. In these modules the electronics is mounted outboard of the silicon with flexible jumpers to bring the signals to the readout chips.

Finally, the design is constrained by the mass and funding budgets. The detector can not have an infinite length, an infinite number of layers, or an infinite number of channels. Given these onerous constraints we have chosen the following overall geometry:

- 7 barrel segments
- 4 detector layers per barrel
  - 2 single-sided layers
  - 2 double-sided layers
- 12 F (small diameter) double-sided disks
- 4 H (large diameter) single-sided disks

	F	H	L1	L2	L3	L4	TOTAL
# detector sides	2	1	1	2	1	2	
# assemblies (both sides)	12	4	7	7	7	7	44
R (min) (cm)	2.57	9.5	2.77	4.61	6.83	9.16	
R (max) (cm)	9.96	26	3.58	5.49	7.52	9.99	
$\|z\|$ (min) or $<dz>$ (cm)	6.4	110	$<12>$	$<12>$	$<12>$	$<12>$	
$\|z\|$ (max) (cm)	54.8	120	42	42	42	42	
# ladders/assembly	12	24	12	12	24	24	
Detector length (cm)	7.5	14.86	6	6	6	6	
Min. detector width (cm)	1.673	2.42	2.115	3.395	2.115	3.395	
Max. detector width (cm)	5.692	6.40	2.12	3.40	2.12	3.40	
Detector area (cm^2)	27.62	65.53	12.72	20.4	12.72	20.4	
Strip pitch (μm)	50	50	50	50	50	50	
# IC's/side	8	10	3	5	3	5	
# detectors/readout unit	1	2	2	2	2	2	
# detectors/assembly	12	48	24	24	48	48	
# detectors (total)	144	192	168	168	366	366	1344
Silicon mass (g)	278	440	149	240	299	479	1885
Sides$\times$area (cm^2)	7954	7528	2137	6854	4274	13709	41222
# sets IC's/assembly	24	24	12	24	24	48	
# sets IC's	288	96	84	168	168	336	
# IC's	2304	960	252	840	504	1680	6540
# kchannels	294.9	122.9	32	108	65	215	837

Table 1.1: Numbers of detectors and geometric parameters of the tracker.

Table 1.1 shows the numbers of detectors and the geometric parameters of the tracker. The 12 cm long barrel segments are separated by 8 mm gaps containing F disks at $|z| =$ 6.4 cm, 19.2 cm and 32.0 cm. Three more F disks are located at each end of the barrel at $|z| = 44.8$ cm, 49.8 cm and 54.8 cm, as shown in Fig. 1.3. The H disks are located at $|z| = 110$ cm and 120 cm.

1.4.2 Performance Considerations

There has been considerable study of optimum designs for tracking and vertexing systems in a collider environment [6]. The basic concerns are 1) momentum resolution, 2) vertex resolution, 3) r-z measurement, and 4) pattern recognition.

Momentum Resolution

Momentum resolution of the tracker is determined by the strength of the magnetic field, its radius, the accuracy of measurement of the helix, and the amount of multiple scattering. We can define an overall figure of merit as the inverse measurement error $(1/\sigma)$ times the

field integral (BR) in the r-ϕ dimension times the lever arm (R), *i.e.* BR^2/σ. The silicon provides an accurate measurement of the track angle at small radius, but the measurement of the sagitta and outer points in the central rapidity region are performed in the fiber tracker. The silicon serves to anchor the track at the inner radius. The number and detailed location of silicon layers does not have a major effect on the momentum resolution.

A plot of the momentum resolution as a function of η for a 1 GeV/c p_t track originating at $z = 0$ is shown in Fig. 1.4. The solid line shows the resolution for the tracker excluding the H disks. As η increases beyond 1.8, tracks begin to miss the last fiber tracker layer and the effective value of BR^2 decreases, rapidly destroying the momentum resolution. Momentum resolution can only be maintained if the detector resolution also improves as $1/R^2$ as $R \to 0$. We have attempted to preserve momentum resolution in the forward direction by adding large area "H" disks, with 10 μm resolution, which cover radii less than 26 cm. These disks do not need to have low mass and can be made more cheaply than the delicate "F" disks and ladders. In the region covered by the H disks the resolution is comparable to the fiber tracker for radii $r > \sqrt{(0.5\text{m})^2 \times \frac{10\,\mu\text{m}}{120\,\mu\text{m}}} = 14\,\text{cm}$. The effect of the silicon on the resolution including the H disks is shown in the dashed line in Fig. 1.4.

Vertex Resolution

Vertex resolution considerations can be understood by considering a simple two layer silicon system with identical resolution at the inner and outer radii, r_1 and r_2. The impact parameter resolution is given by:

$$\sigma = \sigma_{meas} \left\{ \frac{\sqrt{1 + (r_1/r_2)^2}}{1 - (r_1/r_2)} \right\}$$

A similar formula holds for disks where r_1 and r_2 are the radii of the first and last hits on a track passing through several disks. We see that the impact parameter resolution is dependent on the ratio of inner to outer radii of the detector. The cost depends strongly on the outer radius.

Given the above considerations we have decided on a compact system with the inner ladders as close to the beam pipe as is mechanically comfortable and with an outer radius which is consistent with deploying four layers of detectors.

Vertex resolution is also affected by the detector resolution, σ_{meas}. This is primarily a function of the detector strip pitch, which is constrained by existing interconnect and amplifier technology. Our strip readout pitch is chosen to be 50 μm.

Naively the resolution is the pitch/$\sqrt{12}$. In a system where pulse height information is available the resolution is improved by the sharing of charge among two or more readout strips. These charge sharing effects can reduce the resolution from 14 μm (*i.e.* 50 μm/$\sqrt{12}$) to 5–10 μm, depending on the amount of sharing. The effective strip pitch can also be reduced by intermediate strips at smaller pitch (25 μm) which couple capacitively to the instrumented strips.

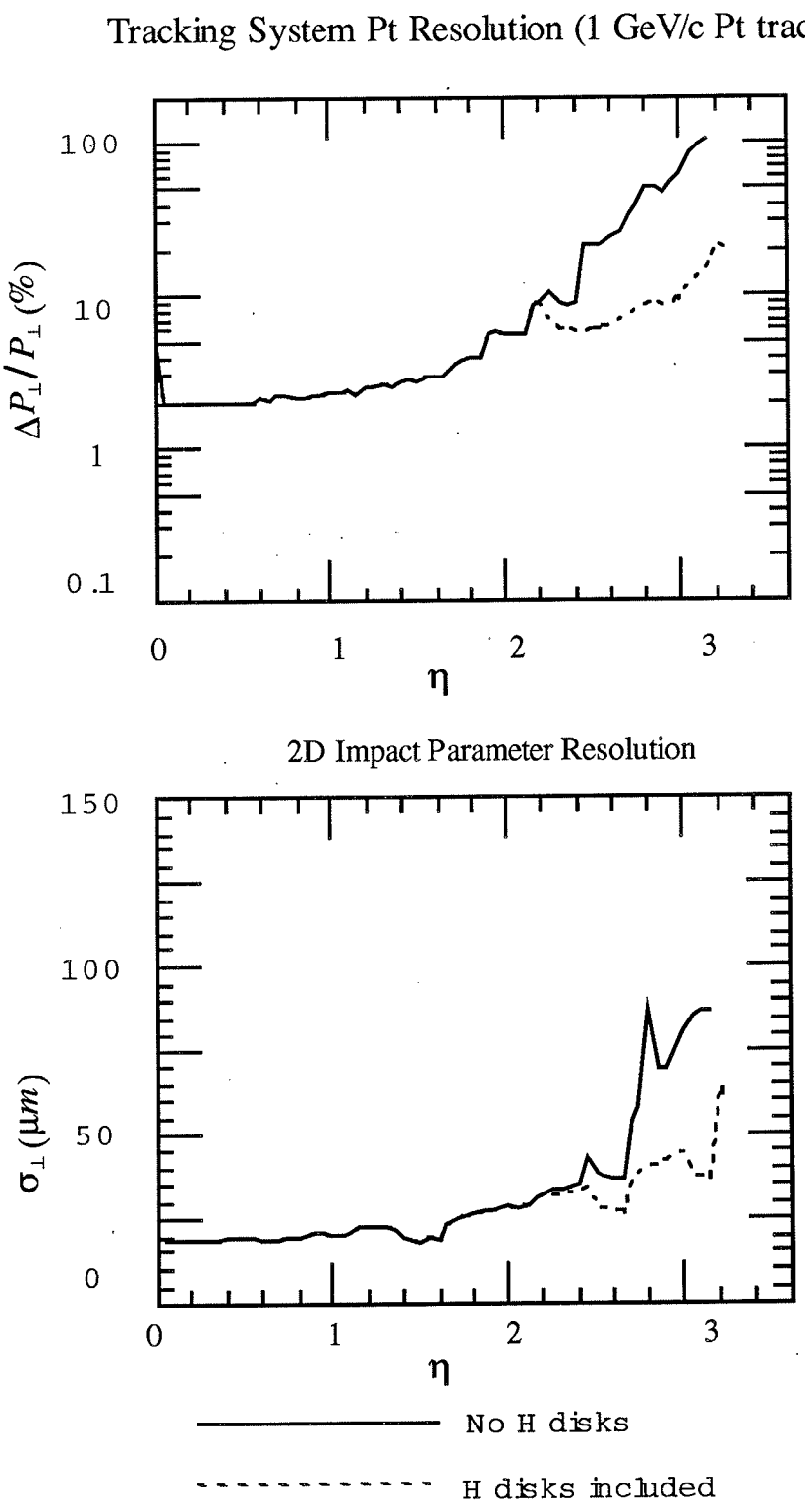

Figure 1.4: Momentum resolution and impact parameter resolution *versus* pseudorapidity.

Measurement in r-z

There are two scales relevant to the r-z measurement in the silicon detectors. The first scale is that of the secondary vertices, with impact parameters in the $100\,\mu$m range. This can only be accomplished with detectors which incorporate large stereo angles (90° is the most straightforward). The other relevant scale is that of the primary vertex measurement. The needs here are determined by the necessity of separating multiple event vertices. This scale is in the several mm–1 cm range. In this case we only need stereo angles of a few (1–4) degrees. We note that for a 2° stereo angle in both the silicon and fiber tracker the angular resolution using the outer fiber tracker layer is about 7 mr and the resolution using the outer and inner silicon layers is about 6 mr.

The r-z resolution also can affect the lifetime, momentum, and mass resolutions of the experiment. If we measure the impact parameter only in the r-ϕ (p_t) plane the lifetime can be written as: $\tau = DL/\gamma c$. Here $DL = DL_\perp/\cos\theta$ where DL is the decay length, $DL_\perp$ is the decay length measured in the transverse plane, and θ is defined from the vertical axis ($\eta = 0$). For $p_\perp \approx m$ the lifetime error due to the r-z (θ) measurement is always smaller than 0.4% for $|\eta| < 1.7$. The errors in the mass and momentum resolution are also negligible for 2° stereo angles [7].

We have chosen to implement the DØ silicon tracker barrel with small angle stereo only, providing r-z resolution at the vertex of $0.5 - 1$ mm, enough to separate primary vertices from multiple events but not enough to be useful for full three dimensional secondary vertex reconstruction unless the disks are involved. Small angle stereo was chosen (and large angle stereo excluded) for several reasons:

1. The pattern recognition problems inherent in the extrapolation from the scintillating fiber system to the silicon tracker were such that small angle stereo planes are necessary to resolve ambiguities in the track extrapolation to the silicon. Thus the tracking system must have at least two small angle stereo planes.

2. The critical dimension for secondary vertices at low η is r-ϕ. Simulations showed that the high resolution r-z measurement is not necessary for top physics [7].

3. Tracks at moderate to high values of η (> 1.5) would pass through many strips of large angle stereo detectors. This makes pattern recognition difficult and impairs the resolution for these tracks.

4. Tracks at $|\eta| > 1.7$ will be well measured in three dimensions by the disks.

5. The implementation of double-sided large angle stereo barrels is technically difficult, requiring either double metalization technology on the detectors or an external fine pitch kapton or glass jumper. This was judged to be too risky.

With a 2° stereo angle and 12 cm barrels there is a triangular dead region which extends from the readout wire-bond to the end of the detector. This area can be as wide as $12\,\text{cm} \times \tan(2°) = 4\,\text{mm}$ if the wire-bonds are at the edge of the detector. These dead regions can result in a significant loss in r-z coverage. This problem can be dealt with either by introducing some sort of a jumper (*i.e.* double metalization as in item 5 above), or by

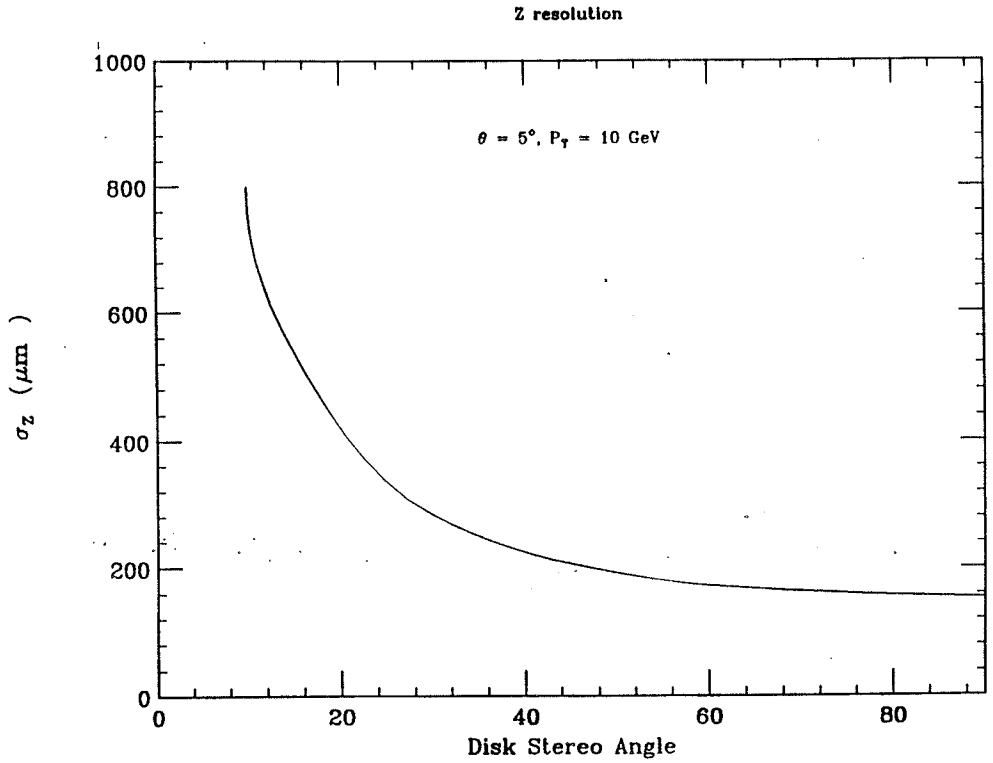

Figure 1.5: Z resolution *versus* disk stereo angle.

having sufficient overlap to cover the dead regions in the adjacent detector. We have chosen the latter course and in all cases the intra-layer overlap is sufficient to keep the r-z dead area to less than 0.5% of the total active area.

In contrast to the barrels, we intend to use the disks to provide full three dimensional vertex reconstruction. The current disk design, with $\pm 15°$ stereo double-sided detectors, was chosen after careful analysis of the tradeoff between resolution and mechanical complexity. Figure 1.5 shows the r-z impact parameter resolution as a function of the disk stereo angle. It is clear that one gains rapidly between 0° and 30° and rather slowly afterward. This drove us to a disk design which has sufficiently large stereo to reconstruct vertices (30°) which also fits on a single double-sided wafer, so no inter-detector wire-bonds are necessary. Tests of these detectors are discussed in Section 2.4.

Pattern Recognition

The number of track hits as a function of pseudorapidity for the upgraded tracker is shown in Fig. 1.6. Each fiber superlayer or silicon plane is counted as one hit. DØ has performed extensive studies of the pattern recognition capability of this detector [1, 2, 3, 4, 5, 6]. In these studies much of the pattern recognition is performed in the outer scintillating fiber layers and tracks are extrapolated to the silicon barrels. Studies have also been performed

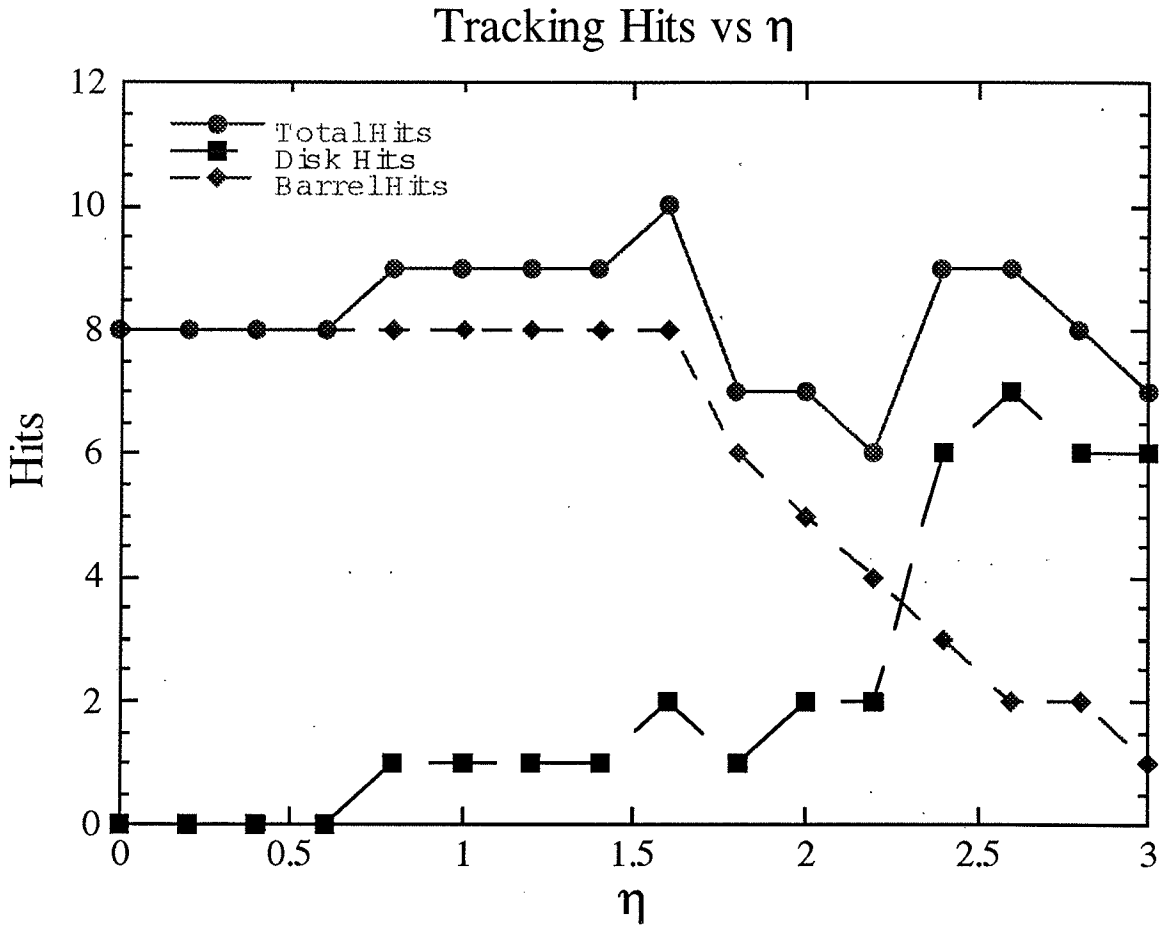

Figure 1.6: Number of silicon tracker hits *versus* pseudorapidity.

on pattern recognition in the forward direction using the silicon disks. These results have also been satisfactory [7]. It may be useful to rotate alternate wedge detectors by 15° to break the ambiguities induced by having a number of identical views.

1.5 Silicon Tracker Mass Issues

The amount of material has a dominant effect on the performance of a vertex detector. Multiple scattering in the inner layers of the detector will limit the angular resolution of tracks, affecting the accuracy with which an extrapolated impact parameter can be determined. Material will also affect momentum resolution and cause conversions, bremsstrahlung, and secondary interactions. In the DØ detector design, with short strips in both barrels and disks, the detector volume per amplifier is small. This means that there must be a great deal of attention paid to the mass of the passive elements such as cables and support structures to insure that the mass ratio of passive to active material is not so large that our physics

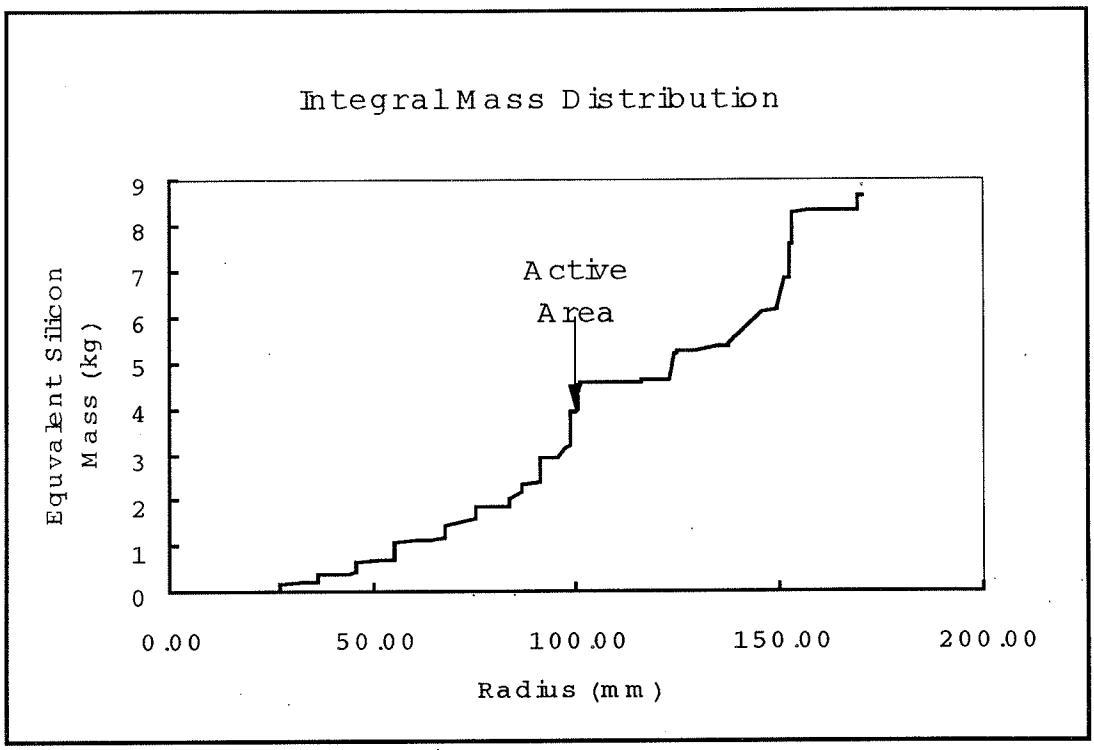

Figure 1.7: Radial distribution of equivalent silicon mass.

goals are compromised.

We have used a large spreadsheet to carefully itemize all significant contributions to the detector mass. Each block of material is characterized by its location, shape, mass, and equivalent silicon mass, *i.e.* mass of material $\times$ $(L_{rad}/L_{rad}(\mathrm{Si}))$. Table 1.2 summarizes the material contributions from various parts of the detector. The total mass of all silicon detectors is 1.44 kg. The mass of the rest of the detector including supports, cables, and utilities is 7.1 kg. The cables and support structures were considered to extend to $|z| = 0.5$ m for the purpose of the mass calculation.

In addition to the total mass the radial distribution must be considered to properly understand the physics consequences. Mass at small radii can destroy the impact parameter resolution for low p_t tracks by smearing the track angle by multiple scattering. Mass at large radii is less harmful. Harmful effects which are independent of radius include conversions and radiation. Figure 1.7 shows the calculated radial distribution of equivalent silicon mass. Much of the mass is concentrated beyond the 10 cm active radius of the silicon. There is a large spike at 16 cm corresponding to the support trough, cables, and matrix cards. To date our Monte Carlo studies have simply taken the active mass distribution and multiplied by factors of between 3 and 6 (Fig. 1.8). In the future we intend to use the detailed mass distribution for further studies of mass effects on detector resolution.

SUBTOTALS	Mass [kg]	Si Mass [kg Si]	% Mass [%]	% Si Mass [%]	Mass Silicon
0 1 2 3					
Total (including 7 modules)	14.267	9.801			6.80
Detector	8.169	5.831	57.26%	59.49%	4.04
All Modules	7.192	5.142	50.41%	52.47%	3.57
Module:	1.027	0.735	7.20%	7.50%	0.51
Silicon	0.190	0.189	18.46%	25.79%	0.13
Ladders	0.167	0.166	16.21%	22.64%	0.12
Disks	0.023	0.023	2.25%	3.15%	0.02
Passive	0.838	0.545	81.54%	74.21%	0.38
Bulkhead	0.224	0.075	21.77%	10.18%	0.05
Water Lines	0.024	0.017	2.37%	2.35%	0.01
Water in Line	0.007	0.004	0.70%	0.59%	0.00
Cable Suppor	0.018	0.016	1.73%	2.20%	0.01
Ladders	0.289	0.205	28.18%	27.90%	0.14
Disks	0.172	0.115	16.78%	15.59%	0.08
Pigtails	0.103	0.113	10.00%	15.40%	0.08
End Disks	0.978	0.688	6.85%	7.02%	0.48
Water Manifolds	0.973	0.641	6.82%	6.54%	0.44
Half Cylinder	2.987	1.443	20.94%	14.73%	1.00
Half Cylinder Supports	0.057	0.095	0.40%	0.97%	0.07
Cables	1.017	0.933	7.13%	9.52%	0.65
Matrix Cards	0.951	0.821	6.66%	8.38%	0.57
Beam Pipe	0.113	0.038	0.79%	0.39%	0.03

Table 1.2: Material contributions from silicon tracker parts.

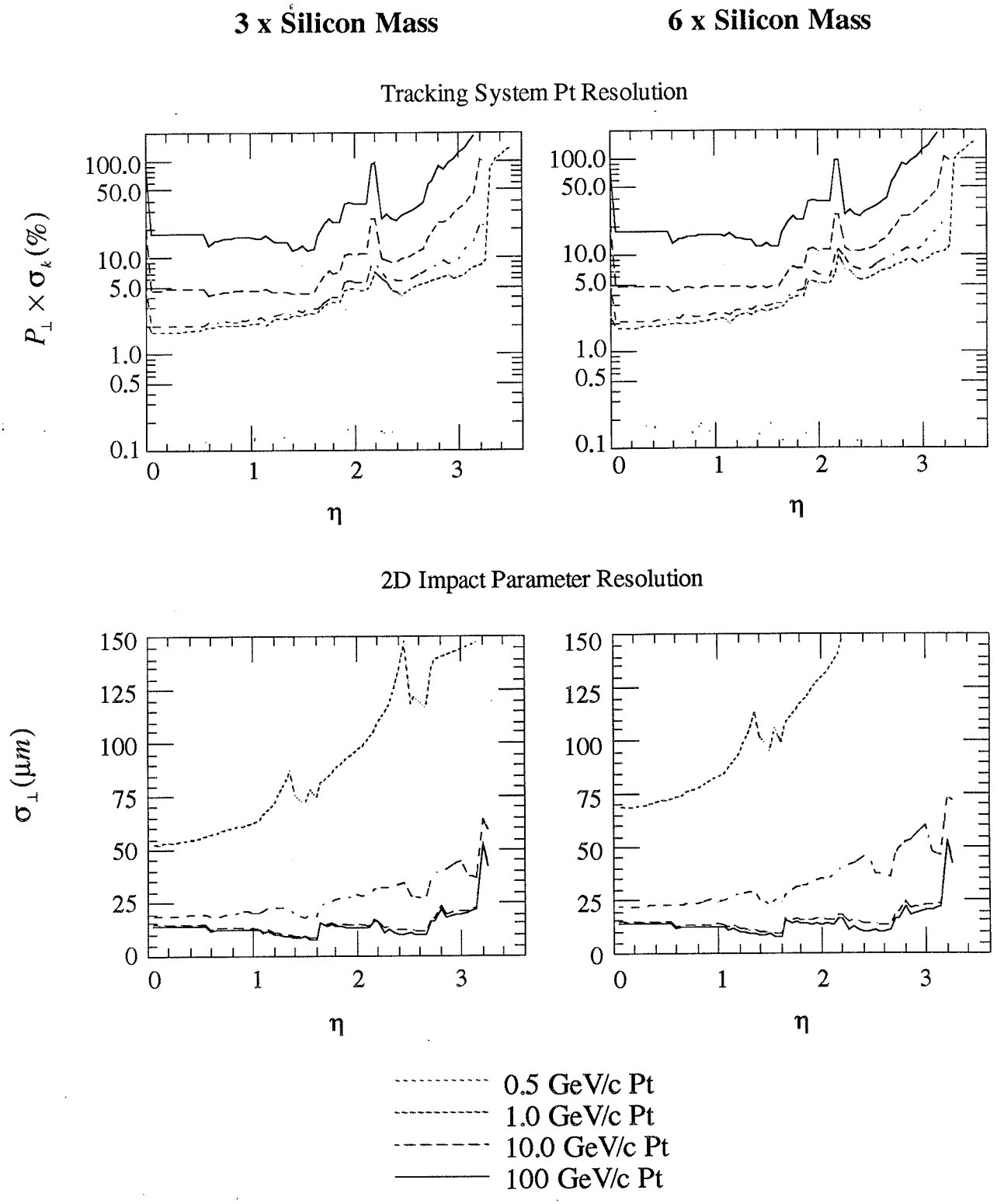

Figure 1.8: Momentum resolution *versus* pseudorapidity with "scaled-up" active mass distribution included.

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Chapter 2

Silicon Detectors

2.1 Design and Specification of Silicon Detectors

The DØ silicon tracker geometry requires three different types of silicon detectors. In the barrel there are two types: a single-sided detector with 384 strips and dimensions 60 mm × 21.2 mm; and a double-sided detector with 640 strips per side and dimensions 60 mm × 34.0 mm. These detectors are designed to be read out by three SVX-II chips or ten SVX-II chips (five on each side) respectively. The other detector type is a double-sided wedge-shaped detector with 1024 strips on each side. Twelve of these detectors are assembled to form a complete 360° disk. The wedge detectors are read out by eight SVX-II chips on each side.

Figure 2.1 shows the layout of the barrel detectors and the wedge detector on 4 inch silicon wafers. Only one wedge detector can be accommodated on a single wafer, whereas three of the narrow barrel detectors or two of the wider barrel detectors can be fabricated on a single wafer. The detectors are arranged to fit inside a 9 cm diameter circle to optimize the yield in fabrication. The 1 cm peripheral area is used for wafer handling during processing.

The design of the H disks has not yet been finalized. Our cost estimate is based on a design where the disks are composed of 24 wedge assemblies of two detectors each. Each wedge would be read out by ten SVX-II chips. We expect to finalize the H disk design this summer with our colleagues from Moscow State University. In the remainder of this chapter we will discuss only the barrel and F disk detectors.

2.1.1 Detector Specifications

The design specifications for the silicon detectors [1] are summarized in Table 2.1. The strip pitch is 50 μm for all detector types. This was chosen to give good position resolution ($\leq$10 μm) and to match the pitch of the SVX-II readout electronics. For the double-sided detectors, stereo strips are used to give 2-dimensional hit information.

The detector specifications are designed to ensure minimum noise in the readout electronics and maximum radiation tolerance. The details of the detector design are discussed below.

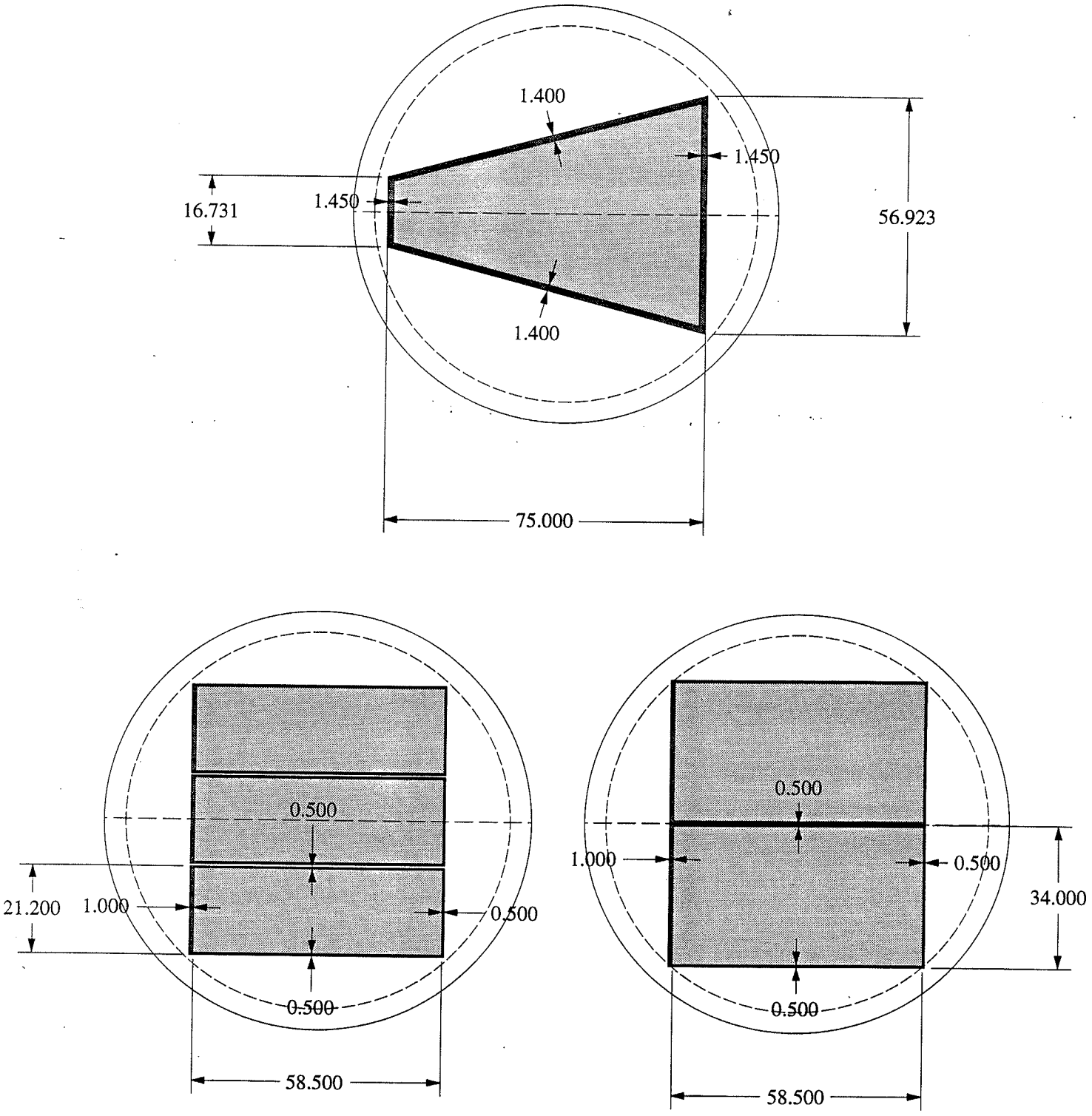

Figure 2.1: Detector layouts on a 4 inch silicon wafer. The lightly shaded areas are the active areas and the darkly shaded areas are the inactive regions. All dimensions are in mm.

(1) Size	
Wafer size	4-inch
Thickness	300 ± 15 μm
Flatness	≤ 20 μm
wedge detectors:	
Detector shape	Trapezoidal
Height	75.000 mm
Base width	56.923 mm
Top width	16.731 mm
Dead regions	1.40 mm (sides), 1.45 mm (base, top)
barrel detectors:	
Detector shape	Rectangular
Dimensions (narrow detectors)	60.000 mm × 21.200 mm
Dimensions (wide detectors)	60.000 mm × 34.000 mm
Dead regions	0.5 mm (sides), 1.00 mm (bias end)
(2) Strip Geometry	
Stereo angle	± 15° (wedges), 0° and 2° (barrels)
Readout strip pitch	50 μm (perpendicular to strips)
Bond pad pitch	51.764 μm (wedges), 50 μm (barrels)
(4) Electrical Specifications	
Depletion voltage	35 ± 15 V
Active area leakage current	≤ 120 nA/cm^2 (measured at FDV*)
Breakdown voltage	$> 2 \times$ FDV (defined at 10μA)
Guard ring leakage current	≤ 5 μA (measured at FDV*)
Coupling capacitance	≥ 25 pF/cm
Coupling capacitor breakdown voltage	≥ 100 V (defined at 2nA)
Interstrip resistance on n-side	≥ 2 MΩ
Polysilicon resistor value	2.0 ± 0.5 MΩ
Percentage of strips meeting specifications	$\geq 99.5\%$
Radiation hardness	> 3 Mrad charged particles
	$> 10^{13}$ neutrons / cm^2

* FDV = Full Depletion Voltage

Table 2.1: Design specifications for the DØ silicon microstrip detectors.

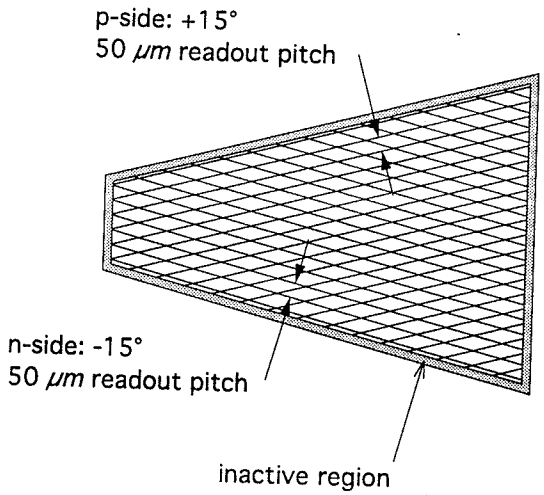

Figure 2.2: Layout of the strips on a double sided-wedge detector.

2.1.2 Wedge Detectors

The wedge detectors are double-sided with height 7.5 cm, active area 24.5 cm^2 and 1024 readout strips on each side. The readout pitch is 50 μm on both sides. The strips on the p-side are at a stereo angle of $+15°$ and those on the n-side are at $-15°$. The strip length varies across the detector, as shown in Fig. 2.2. To avoid dead regions and to aid in alignment, there is an overlap of 707 μm between the active regions of neighboring wedges.

The detectors are fabricated on n-type silicon of thickness 300 μm and resistivity >5 kΩcm. They are ac-coupled to the readout electronics by capacitors integrated directly onto each strip. The capacitor is formed by a thin dielectric layer between the strip implant and the aluminum metallization. Polysilicon resistors are used to bias the strips since this technology has been shown to be radiation hard [2, 3]. Prototypes of the wedge detectors have been fabricated and tested (see Section 2.2).

Figure 2.3 shows a schematic of the p-side of the wedge detector mask layout. The p^+ strips are at a pitch of 50 μm. The strips are metallized and the bond pads are angled at 15° to allow parallel wire-bonding to the SVX-II chips. The effective bonding pitch is 51.8 μm. On the n-side, the n^+ implants are at a pitch of 50 μm. On both sides, the implanted strips are connected via polysilicon resistors to a bias line. The polysilicon resistors have a nominal design value of 2 MΩ. Two sets of bond pads, offset by 2 mm, were provided on the prototypes to allow us to support the region underneath the bond pads during ultrasonic wire-bonding.

The nominal implant strip width for the readout strips on the p-side and n-side is 10 μm. This value was chosen to give a small interstrip capacitance and a reasonably large value for the coupling capacitance. The coupling capacitors are formed by growing a 200 nm silicon dioxide layer over the strip.

It is well-known that for n-type bulk silicon, the positive fixed oxide charge can create an accumulation layer at the silicon surface, causing a very low impedance path between neighboring n^+ strips. To circumvent this, p^+ isolation implants have been introduced between the n^+ strips in the prototypes fabricated at Micron Semiconductor. The width of this im-

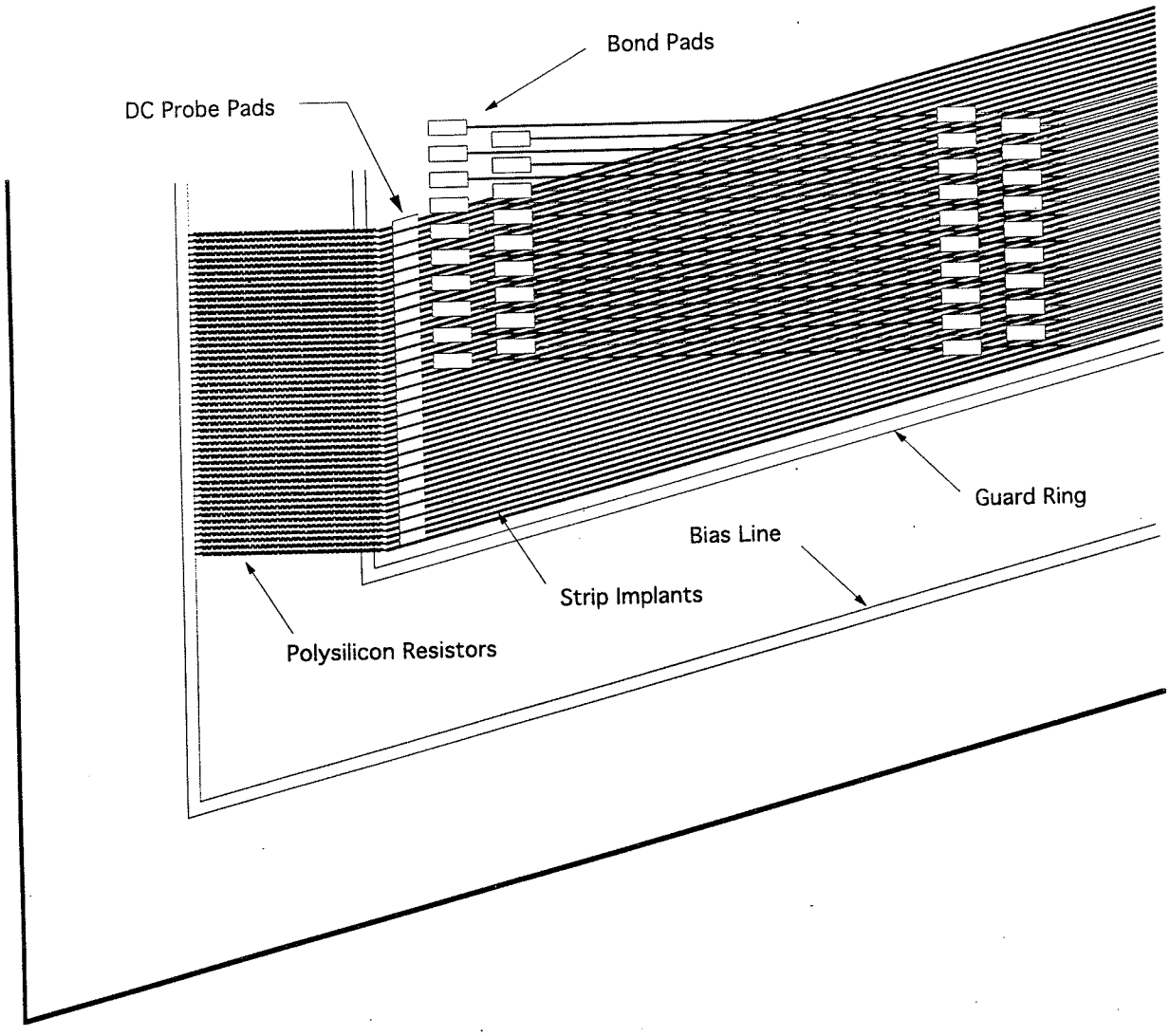

Figure 2.3: Schematic of a wedge detector layout with polysilicon biasing (p-side).

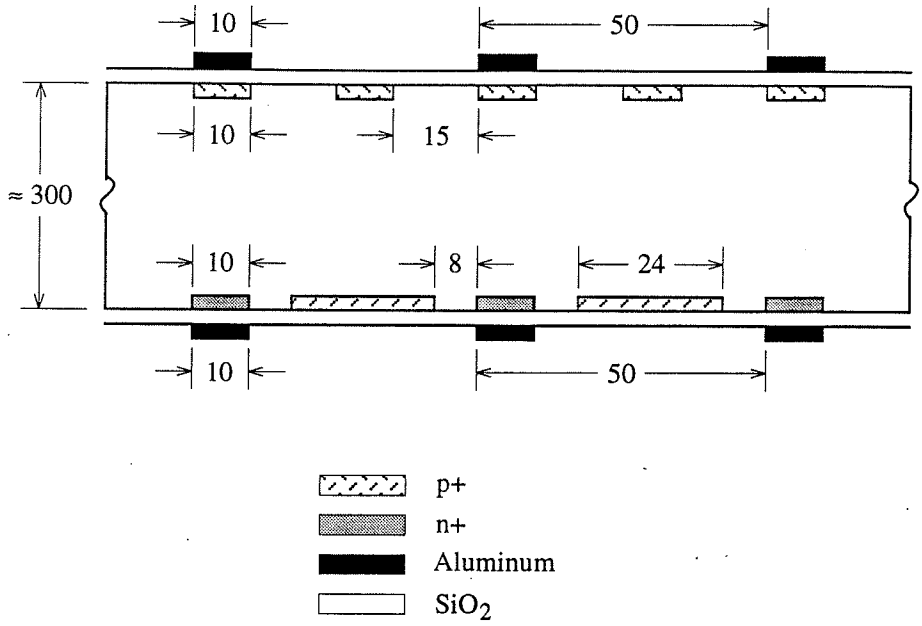

Figure 2.4: Cross-section of the double-sided detector design. All dimensions refer to the mask design and are in microns.

plant (24 μm) was chosen to be as wide as possible to achieve a low interstrip capacitance [4]. Figure 2.4 shows a schematic cross-section through the silicon wafer transverse to the strip direction for the prototype wedge detectors. For the final detectors we may need to increase the strip width to obtain a higher coupling capacitance. In this case, the intermediate strips on the p-side would be omitted.

2.1.3 Barrel Detectors

The barrel detectors are 6 cm long with 50 μm readout pitch. The strips on the n-side are parallel with the p and $\bar{p}$ beams (*i.e.* axial) and those on the p-side are at a stereo angle of 2°. Apart from the different detector shape and stereo angle, the design of these detectors is similar to that of the wedge detectors described above. A schematic mask layout for the barrel detectors is shown in Fig. 2.5.

A barrel ladder is constructed by wire-bonding two detectors together to give a total active strip length of 11.7 cm. Bond pads are therefore provided at both ends of the detector as shown in Fig. 2.5. The pads at the end of the detector containing the polysilicon biasing will be used to bond to the SVX-II readout electronics and those at the opposite end will be used for bonding to the second detector.

2.2 Results from Wedge Detector Prototypes

In this section we describe the results from measurements on the prototype wedge detectors [5]. We have concentrated our efforts on these detectors since they are more novel than

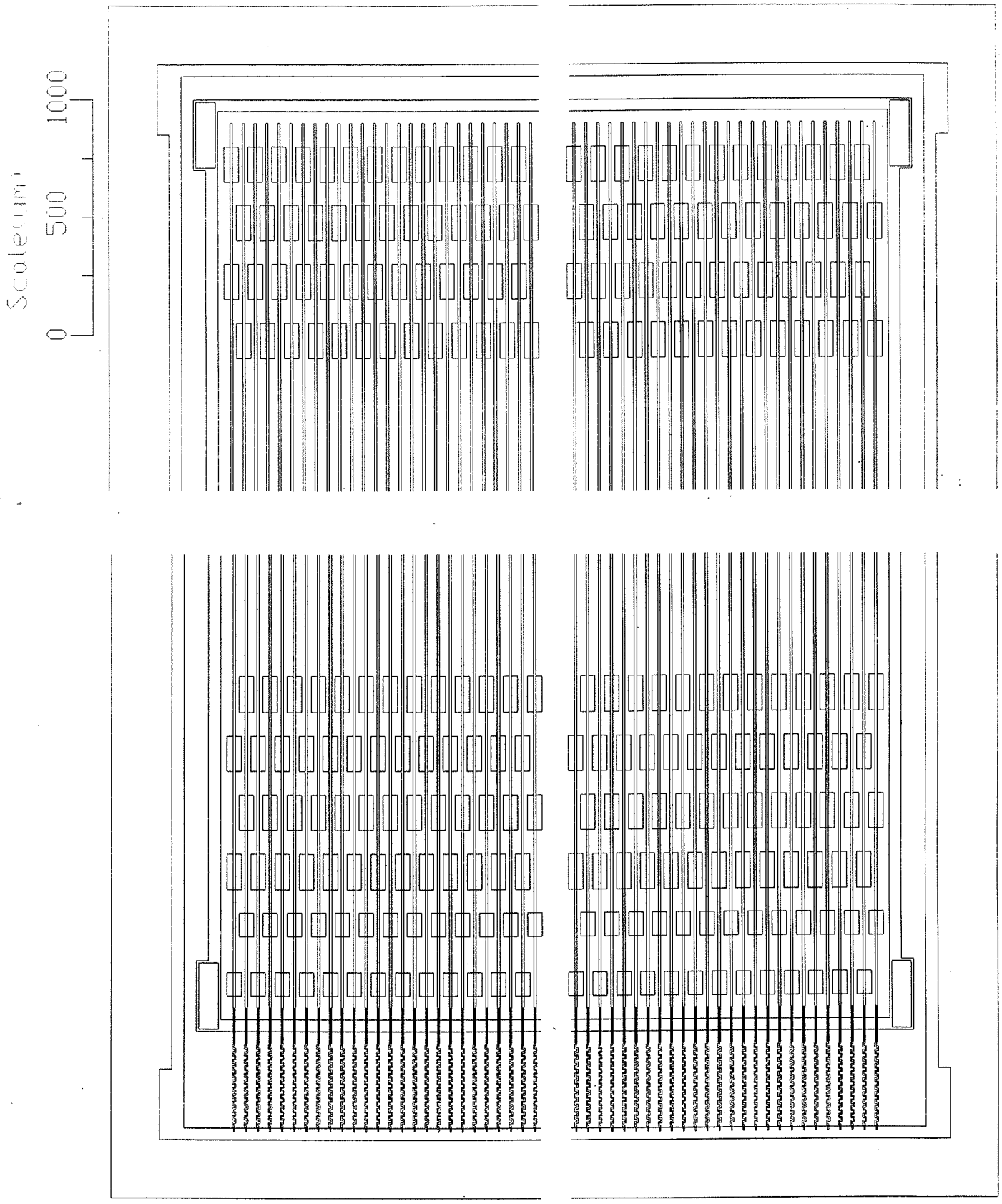

Figure 2.5: Schematic of a barrel detector layout (axial strip side).

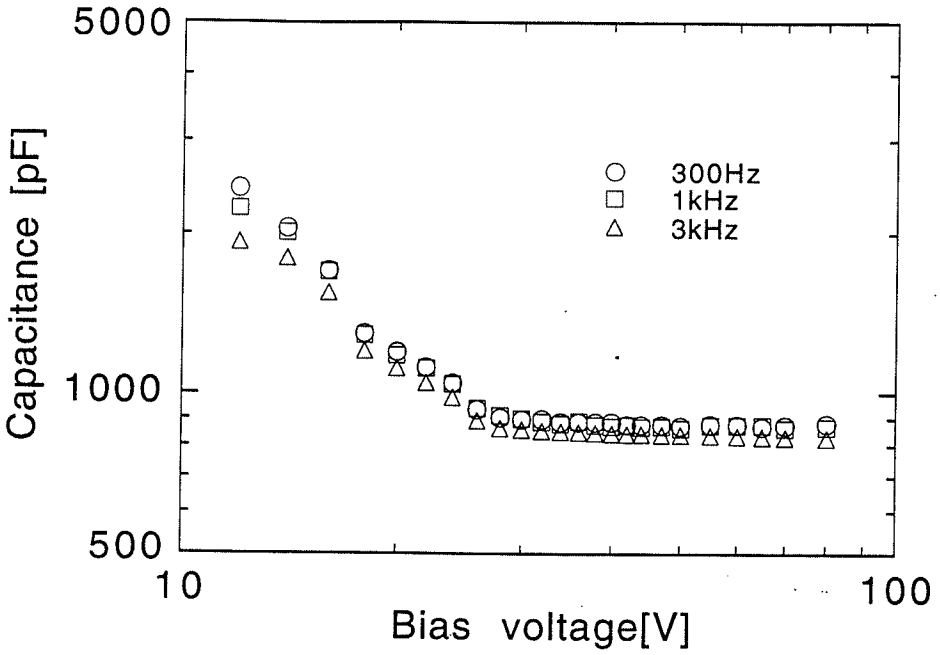

Figure 2.6: Total detector capacitance versus bias voltage for a prototype wedge detector.

the barrel detectors. The mask designs for these detectors were done by the UC Riverside group in close collaboration with the detector manufacturers. Two sets of prototype wedge detectors have been fabricated, one set at Micron Semiconductor, UK [6] (11 detectors) and another at SINTEF SI, Norway [7] (9 detectors). Unless specifically indicated, all of the results here refer to the detectors fabricated by Micron, since these detectors met all our design specifications (Table 2.1.)

2.2.1 Depletion Voltages

A measurement of the full depletion voltage is necessary to determine a suitable operation voltage for the detectors. Since it is desirable that all detectors in a barrel layer or F-disk have approximately the same operation voltage, we require the detector depletion voltages to be uniform to within ± 15 V.

We have determined the full depletion voltages of the prototype detectors by capacitance measurements directly on the detectors, without the need for test structures. Although the measurements show a dependence on frequency, this is well understood and we were able to extract the full depletion voltage from these measurements.

Figure 2.6 shows the measured capacitance versus bias voltage for one of the prototype wedge detectors. The data show the expected behavior

$$C \propto \frac{1}{\sqrt{V_{\text{bias}}}} \tag{2.1}$$

for an abrupt pn junction [8]. At full depletion the capacitance becomes roughly constant, although it continues to fall very slowly due to edge effects.

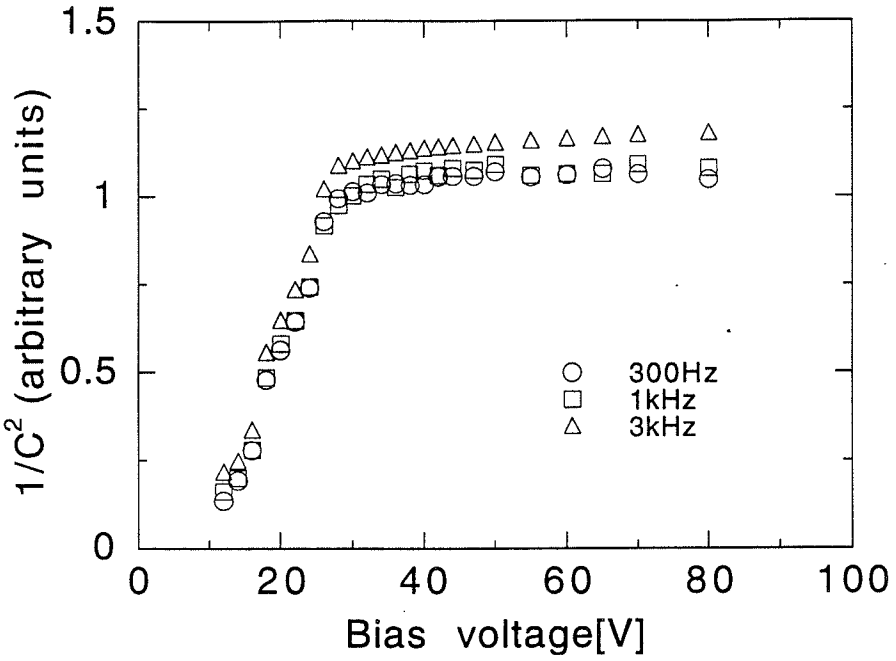

Figure 2.7: A plot of $1/C^2$ versus bias voltage for a prototype wedge detector.

This behavior is more clearly seen if $1/C^2$ is plotted against the bias voltage as in Fig. 2.7. Note the clearly visible change in slope at full depletion V_{dep}. The distributions of the depletion voltages for the two sets of prototype detectors are shown in Fig. 2.8.

2.2.2 Leakage Current and Breakdown Voltage

Shot noise due to the detector leakage current contributes to the overall noise of the readout electronics and should therefore be minimized in the detector fabrication process. Figure 2.9 shows a measurement of active area leakage current versus bias voltage for one of the wedge

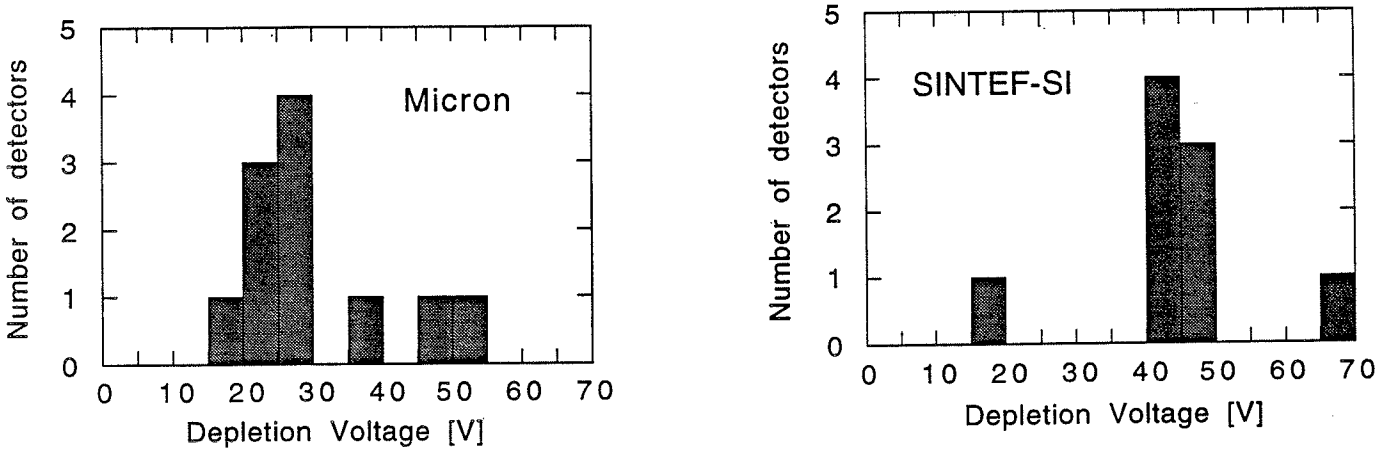

Figure 2.8: The distributions of full depletion voltage for the two sets of prototype detectors.

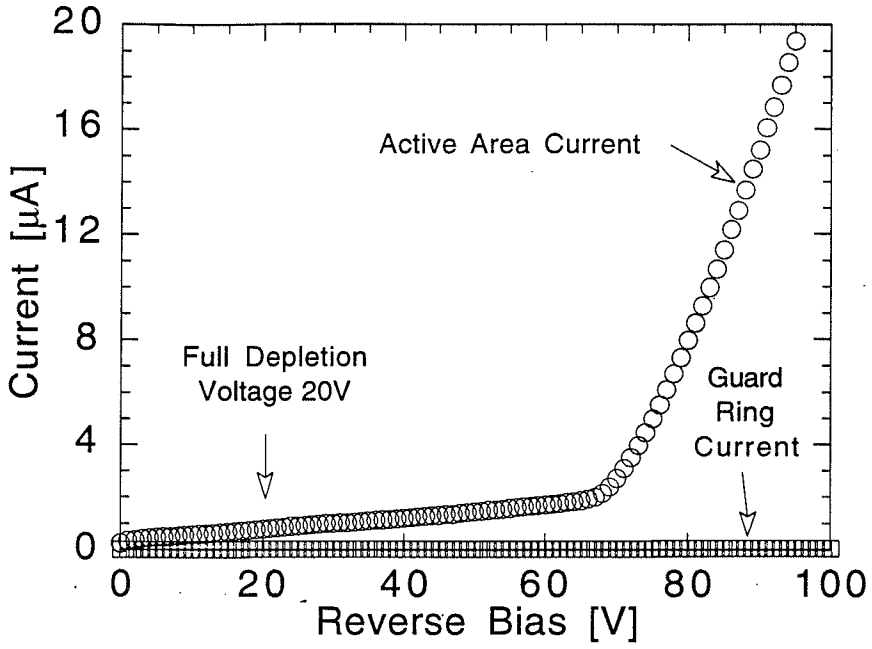

Figure 2.9: Active area leakage current versus applied voltage.

detector prototypes. The breakdown voltage (defined at a current of 10 μA) is approximately 85 V, well above the full depletion voltage (20 V).

The distributions of leakage currents at full depletion for the two sets of prototype detectors are shown in Fig. 2.10. In our specifications we require that the active area leakage current per unit area be less than 120 nA cm^{-2}. For the wedge detectors this is equivalent to a total current of about 3 μA, or 3 nA per strip. The leakage current shot noise is then negligible compared with the series noise due to the detector capacitance.

A summary of the prototype measurement results is given in Table 2.2.

2.2.3 Coupling Capacitors

(a) Breakdown voltage

One of the important design parameters of the detectors is the breakdown voltage of the coupling capacitors. This must be well above the detector full depletion voltage to ensure reliable long term operation. Also, since the depletion voltage increases with time due to radiation damage, a high coupling capacitor breakdown voltage is necessary to ensure radiation hardness.

The breakdown of the coupling capacitor was measured with probes on the detector, one connecting to the aluminum strip and the other to the dc contact pad connecting to the strip implantation for the same strip. The leakage current as a function of applied voltage was measured for two types of capacitors, one with a silicon dioxide dielectric, the other with both silicon dioxide and silicon nitride, as shown in Fig. 2.11. A current limit of 50 nA

Detector	V_{dep} [V]	I @ V_{dep} [μA]	V_{op} [V]	I @ V_{op} [μA]
MSL-905-1	18	0.300	23	0.370
MSL-905-9	35	0.560	40	0.590
MSL-935-18	49	3.600	54	3.800
MSL-935-23	50	3.400	55	3.700
MSL-969-02	29	0.450	34	0.500
MSL-969-11	27	0.500	32	0.550
MSL-969-12	25	0.460	30	0.540
MSL-969-13	24	0.675	29	0.700
MSL-969-15	20	0.800	25	1.000
MSL-969-16	28	0.440	32	0.450
MSL-969-22	23	1.800	28	2.500
SI-1024-00	65	750	70	900
SI-1024-02	47	120	52	150
SI-1024-15	18	0.200	23	0.280
SI-1024-26	42	60	47	70
SI-1024-31	44	170	49	230
SI-1024-33	45	240	50	250
SI-1024-41	47	120	52	140
SI-1024-42	40	130	45	160
SI-1024-47	44	85	49	110

Table 2.2: Summary of bulk test results. V_{dep} is the full depletion voltage and V_{op} is defined to be V_{dep} + 5 Volts. I @ V_{dep} and I @ V_{op} are the active area leakage currents measured at V_{dep} and V_{op} respectively.

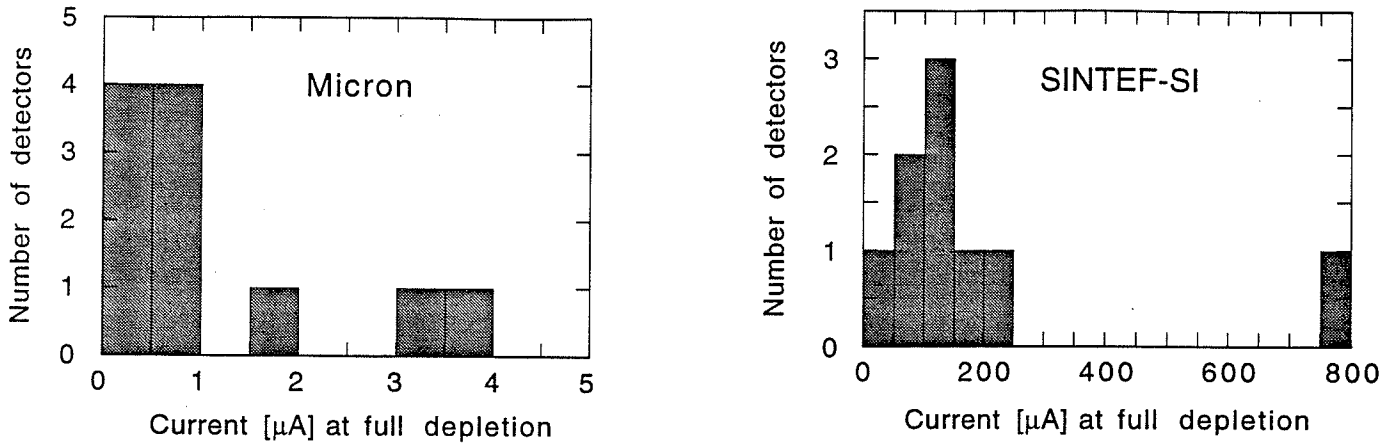

Figure 2.10: The distributions of active area currents at full depletion for the two sets of prototype detectors.

was imposed to avoid damage to the capacitors. The simple silicon dioxide capacitors have a breakdown voltage of 80 V. For the final detectors we will increase this to 100 V by increasing the thickness of the oxide layer.

(b) Capacitance

To avoid loss of signal from the detector we require $C_C \gg C_D$, where C_C is the capacitance of the coupling capacitor and C_D is the detector strip capacitance. This requirement is a trade off with the requirement of high capacitor breakdown voltage. For the prototype wedge detectors, we used a 200 nm silicon dioxide layer as capacitor dielectric. For a 10 μm strip width, this results in a predicted breakdown of $\approx$100 V and a coupling capacitance of $\approx$17 pF/cm.

The capacitance of the coupling capacitors was measured with probes on the detector, one connecting to the aluminum strip and the other to the dc contact pad which connects to the strip implantation. The capacitance is shown as a function of measurement frequency in Fig. 2.12 for a typical coupling capacitor. The decreasing effective capacitance with increasing frequency was due to the finite resistance of the strip implantation, which became significant at higher frequencies [9]. This can be well modelled using an equivalent circuit network and it is found that the true capacitance is the value at low frequency. Therefore, the coupling capacitor capacitance can be measured directly, without requiring a test structure. The measured coupling capacitance for the prototype detectors was 160 pF, *i.e.* 21 pF/cm.

2.2.4 Bias Resistors

Polysilicon resistor biasing was chosen since this method has been shown to be sufficiently radiation hard. The choice of resistance value is a trade off between minimizing the Johnson noise contribution of the resistor (favoring high values) and minimizing the voltage drop across the resistor due to radiation-induced leakage currents (favoring low values). A design value of 2 MΩ has been chosen. We estimate a 2 MΩ resistor will result in a noise contribution

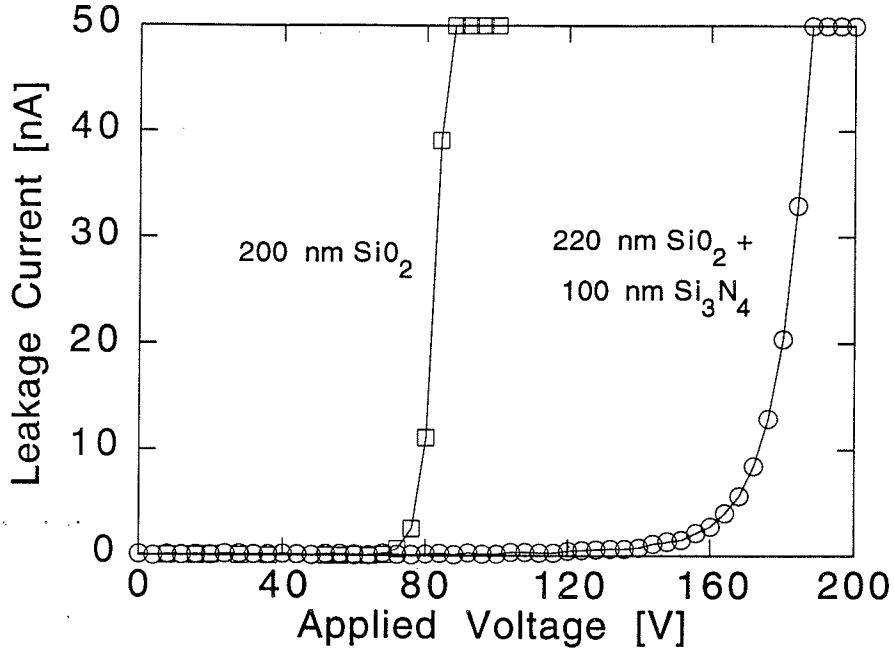

Figure 2.11: Breakdown voltage determination for two types of coupling capacitors.

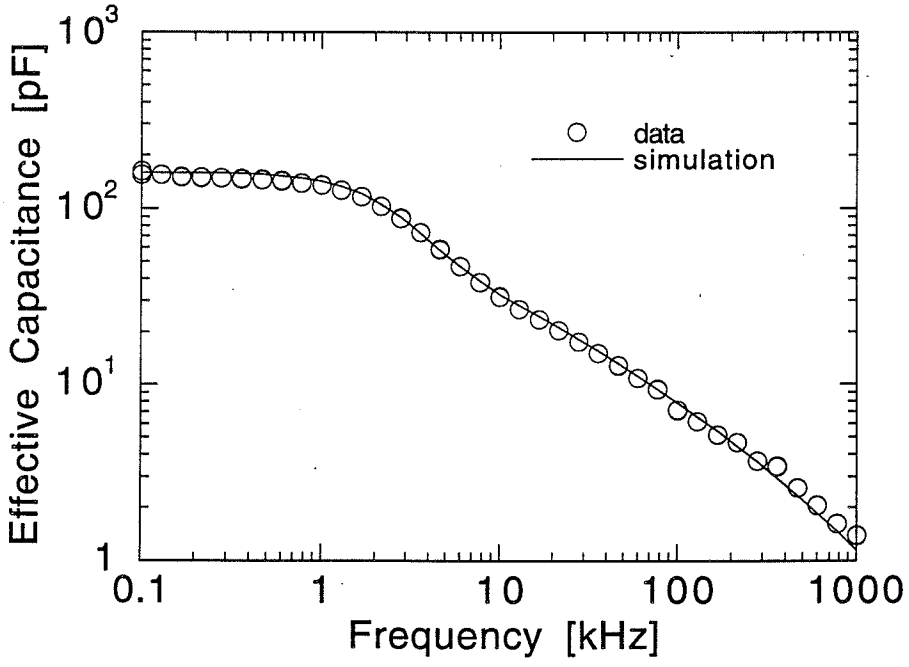

Figure 2.12: Measured coupling capacitance versus test frequency for a full length (7.5cm) strip. The solid line is a circuit model with the strip implant resistance included.

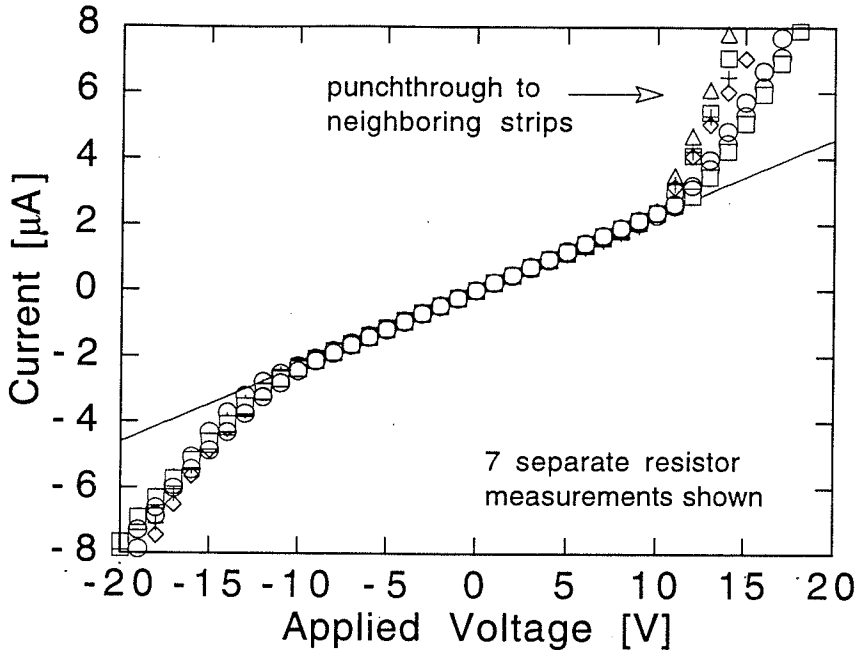

Figure 2.13: Measurement of the polysilicon resistance for a prototype wedge detector.

of 131 e^- rms (227 e^- rms) for 132 ns (396 ns) sampling time. Since the expected noise is about 1000 e^- rms (disk detectors), the noise due to the bias resistor will contribute less than 2.5% to the total noise.

The polysilicon bias resistors were measured by probing the dc contact pads, and observing the current flowing to the bias line as a function of applied voltage. The slope of the resulting line gives the polysilicon resistance as shown in Fig. 2.13. We measured values of 4.6 MΩ for the p-side resistors and 3.4 MΩ for the n-side resistors. The uniformity on each side was within 3%. For the final detectors the manufacturer will be able to tune the polysilicon doping to get the correct value of 2 MΩ on both sides. This was not possible for the prototypes because of the very small number of detectors produced.

2.2.5 n-side Interstrip Resistance

As discussed above, to obtain a high interstrip resistance on the n-side, we used a 24 μm width p^+ isolation implant between the n^+ strips. To predict the interstrip resistance for this geometry we have used the simulation tools DIOS [10] and TOSCA [11]. These programs enable a complete simulation of the electrical characteristics of the detectors. Figure 2.14 shows a plot of the calculated interstrip resistance vs. electron lifetime (τ_e) for a fixed hole lifetime (τ_h) of 100 μsec. From leakage current measurements, we have estimated the effective lifetime of the prototype detectors to be about 2 msec. The simulation then predicts an interstrip resistance of 25 GΩ.

The n-side interstrip resistance for the prototype wedge detectors was measured on a probe station by contacting dc probe pads on the n^+ strips. Figure 2.15 shows a result of such a measurement. The measured resistance is 20 GΩ, in good agreement with the

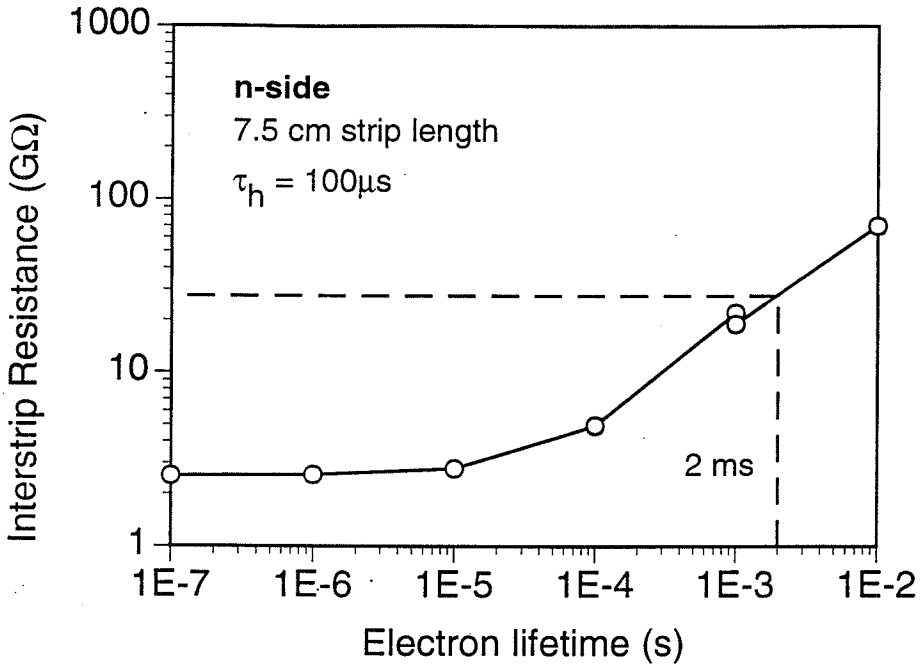

Figure 2.14: TOSCA simulation of n-side interstrip resistance vs. electron lifetime for the DØ prototype wedge detectors.

simulation. This demonstrates that the p^+ isolation implantation results in a high n-side interstrip resistance, as expected.

2.2.6 Detector Strip Capacitance

The capacitance at the input of the SVX-II is the total capacitance of one strip of the detector. Our design goal for the capacitance is 1.6 pF/cm for the p-side and 2.0 pF/cm for the n-side.

A full TOSCA simulation has been performed in order to model the total strip capacitance. The main contributions to the total capacitance are from the nearest neighbor strips, the second nearest neighbor strips and the backplane. Figure 2.16 shows these contributions as a function of bias voltage for a p-side strip with 50 μm strip pitch simulated with TOSCA. Since there are neighbor strips on each side of the strip, the total capacitance is $2C_1 + 2C_2 + C_b$, where C_1 is the capacitance to the nearest neighbor, C_2 is the capacitance to the second neighbor and C_b is the capacitance to the backplane. From the simulations we predict a total strip capacitance of 1.6 pF/cm for the p-side and 1.8 pF/cm for the n-side. Table 2.3 shows the predicted capacitances for the n-side and p-side in the disks and barrels. The highest capacitance is that of the n-side strips of the barrel ladders (21 pF). Measurements of the capacitance on prototype detectors are in progress and will soon be completed.

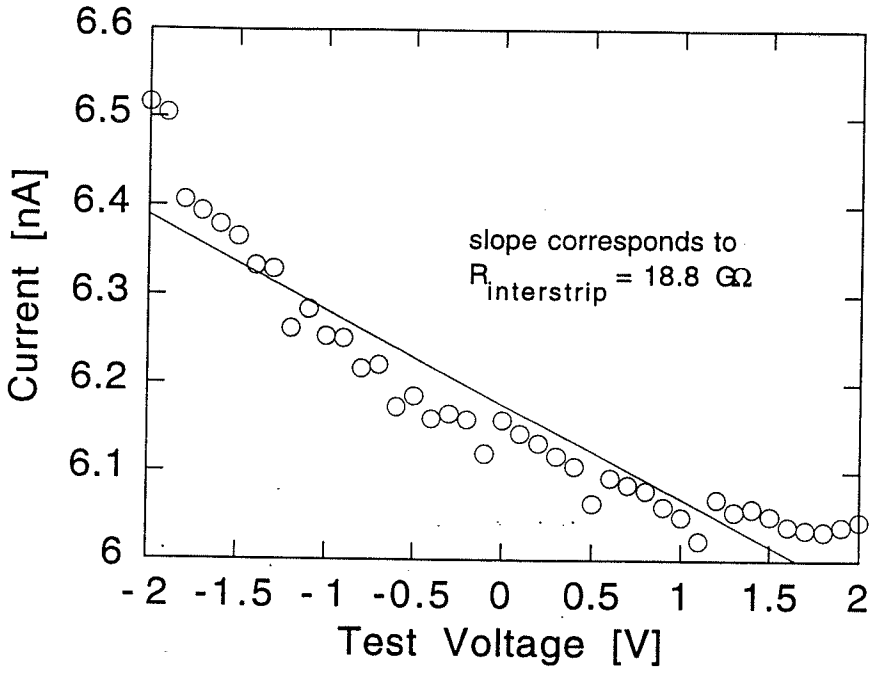

Figure 2.15: Measurement of the interstrip resistance on the n-side of a prototype wedge detector.

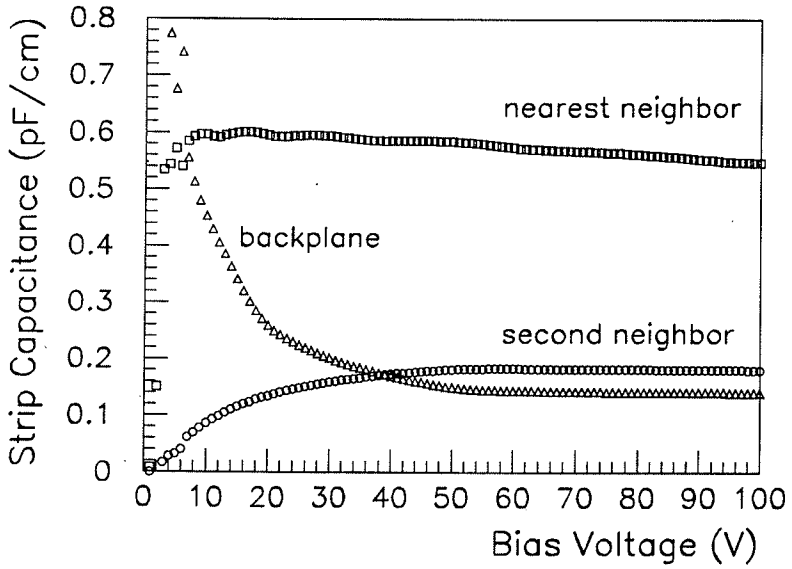

Figure 2.16: TOSCA simulation of the contributions to the p-side strip capacitance vs. bias voltage for the DØ prototype wedge detectors.

	C (pF/cm)	Barrel C_{TOT} (pF)	Disk C_{TOT} (pF)
n-side	1.8	21.0	13.5
p-side	1.6	18.7	12.0

Table 2.3: Total strip capacitance results from TOSCA simulations. The strip length in the barrel ladders is 11.7 cm and in the disks the maximum strip length is 7.5 cm.

2.3 Radiation Damage

Radiation damage is a primary concern in the design of the silicon detectors. The particle fluences expected at the interaction region of DØ have been calculated in reference [12]. The flux of charged particles varies as $r_\perp^2$, where $r_\perp$ is the perpendicular distance from the beam line. The flux of neutrons is roughly independent of $r_\perp$. The calculations are summarized in Fig. 2.17, which shows the expected fluence of charged particles and neutrons for $1\,\mathrm{pb}^{-1}$ of delivered integrated luminosity.

The important effects of radiation damage are (a) an increase in detector leakage current due to radiation induced generation-recombination centers and (b) a change in depletion voltage due to the creation of effective p-type doping centers.

2.3.1 Increase in Leakage Current

The increase in leakage current results in an increased shot noise contribution to the overall readout electronics noise. We have estimated the noise increase based on measurements of the leakage current damage constants. The worst case noise increase will be in the inner barrel layer which has a strip length of 11.7 cm and radius $r_\perp = 2.78\,\mathrm{cm}$. This case is illustrated in Fig. 2.18 which shows the equivalent noise charge contribution due to leakage current as a function of delivered integrated luminosity. We have assumed an average detector temperature of 20°C for this calculation and an SVX-II sampling time of 132 ns. As can be seen, after $2000\,\mathrm{pb}^{-1}$ the total noise contribution from the radiation-induced leakage current is about 800 e^-. Since the total noise for a barrel detector will be about 1400 e^- before irradiation, the total noise after $2000\,\mathrm{pb}^{-1}$ will be about 1600 e^-. This increase in noise will not present a problem for operation of the detectors. In fact, as described below, the limit on the detector lifetime is due to the change of full depletion voltage.

2.3.2 Change of Full Depletion Voltage

The effect of radiation damage is to create p-type centers in the bulk silicon, thereby changing the effective doping concentration. This causes type inversion of the silicon bulk from n-type

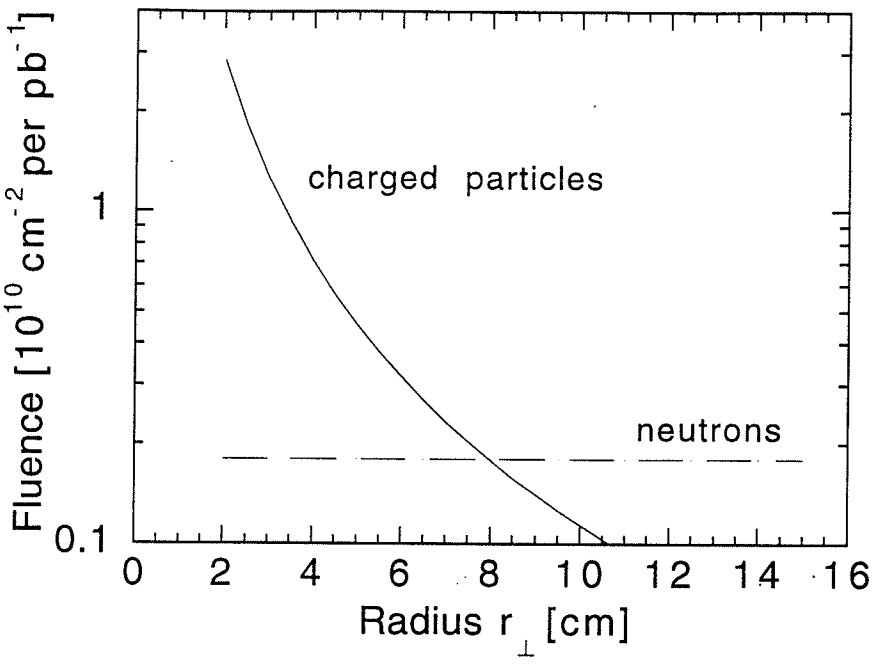

Figure 2.17: Fluence of charged particles and neutrons for $1\,\mathrm{pb}^{-1}$ as a function of $r_\perp$.

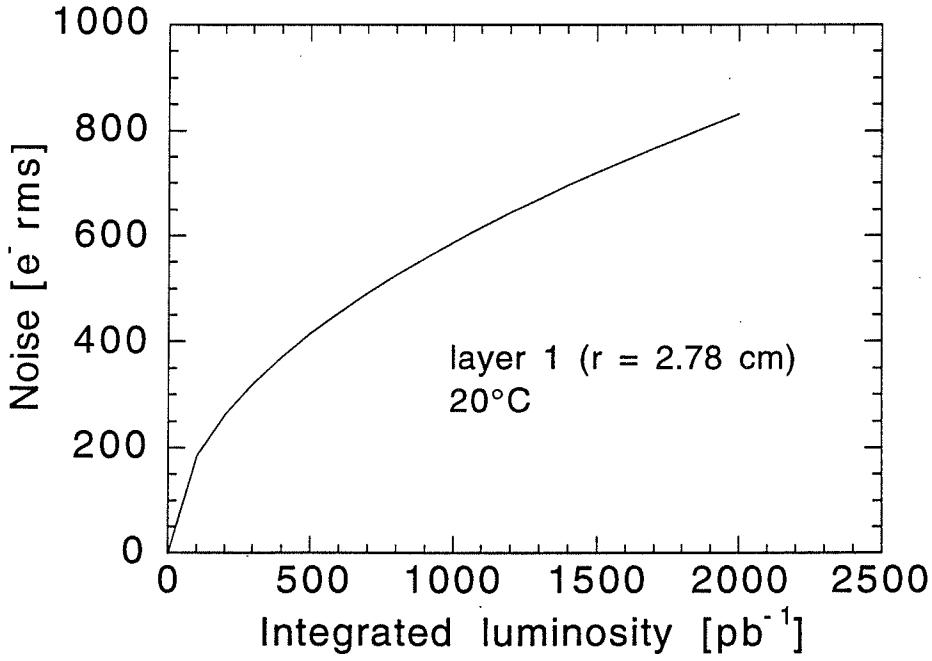

Figure 2.18: Contribution of radiation-induced leakage current shot noise vs. integrated luminosity for 132 ns sampling time.

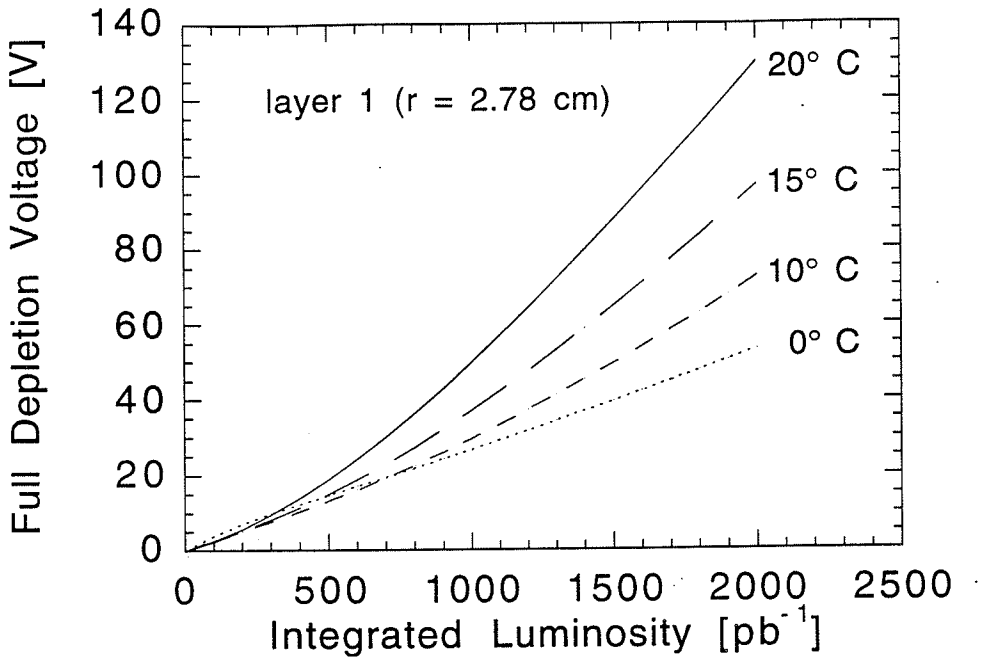

Figure 2.19: Predicted full depletion voltage as a function of integrated luminosity and temperature.

to p-type, after which the full depletion voltage increases with particle fluence. This effect has been studied in detail [13] and we are able to estimate the full depletion voltage as a function of run time. Figure 2.19 shows the calculated full depletion voltage for the inner barrel ladder as a function of integrated luminosity delivered to the DØ interaction region. The behavior is temperature dependent because of the effects of "anti-annealing". If we assume that the maximum practical operating voltage is about 100 V, the maximum lifetime of the inner barrel detectors will be approximately $1500\,\mathrm{pb}^{-1}$ at 20°C and $2000\,\mathrm{pb}^{-1}$ for 0°C operation. Note that the F-disks extend to an inner radius of 2.57 cm and operate at a temperature close to 10°C. This gives a lifetime of greater than $2000\,\mathrm{pb}^{-1}$ for the F-disk wedge detectors.

2.4 Plans for Production Electrical Testing

In order to ensure all detectors that are used to construct the DØ silicon tracker meet our specifications, we will carry out quality assurance (QA) measurements on detectors. Measurements of the electrical characteristics will be performed first, and measurements of the response of ladder and disk modules to a laser simulating a charged particle will be made after module assembly. In this section we describe the former QA tests.

The measurements will be done on an automated probe station read out by a Macintosh computer. Such a system has already been assembled at UC Riverside and similar systems will be duplicated at Fermilab and at Oklahoma University. The system consists of an automatic probe station, semiconductor source-measure units, a precision LCR meter and a video camera. The system is controlled by GPIB interface to a Macintosh computer. The

probe station measurements will consist of a measurement of the following parameters:

- full depletion voltage
- total active area leakage current at the operating voltage
- coupling capacitor short circuits (or low breakdown voltage)

Detectors with similar full depletion voltages will be grouped together for use in the same barrel segment or F-disk. The measurement of coupling capacitor shorts is particularly important. A shorted capacitor results in an excess current into the SVX-II amplifier. This may cause saturation and affect neighboring channels. Therefore, it will be important to identify strips with shorted capacitors (or low capacitor breakdown voltage) and to avoid bonding these channels to the SVX-II readout.

The measurements described above will made on every detector. Other measurements will also be made on a subset of detectors. These include measurements of parameters which are not expected to change from wafer to wafer, but may show variations between different batches of fabrication. These parameters are:

- coupling capacitor capacitance
- bias resistor resistance
- interstrip resistance
- interstrip capacitance

The results of all QA measurements will be entered into a comprehensive database so that the parameters of any detector in the DØ silicon tracker can easily be accessed.

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Chapter 3

Assembly Alignment Constraints

3.1 Introduction

This section addresses the strip-position tolerances needed to ensure the ability to trigger on tracks arising from the decay of long lived particles and to ensure that the number of constants required for event reconstruction is tractable. Section 3.2 contains a discussion of the physics constraints relevant to the tolerances, and Sections 3.3 and 3.3.1 contain results for the tolerances. Details can be found in reference [1].

3.2 Physics Constraints

The main criterion used to constrain the position tolerances is that misalignment effects should be negligible in comparison with intrinsic system resolution. The relevant resolution depends on which phase of data-taking and analysis is under consideration. The trigger-level resolution is set by the size of the interaction region, whereas the resolution scale for event reconstruction is set by the impact parameter of tracks arising from the decay of long-lived particles. Each of these is motivated in the following paragraphs.

The position of the interaction point during Run II will be known to between 20 μm and 50 μm in the plane transverse to the beam direction, and the angle of the beam with respect to the nominal direction will be known to 100 μrad. Because the silicon trigger is to be based on detecting tracks from particles decaying outside of the beam envelope, knowledge of the beam position sets the level below which misalignment effects can be ignored. It is also likely that only partial track-reconstruction will be available to measure the interaction position, emphasizing further the need to limit misalignment effects to less than the beam size.

The main physics goal associated with the silicon detector is tagging the presence of particles containing b-quarks. This will be done either by identifying tracks having a large impact parameter in the plane perpendicular to the beam or by detecting detached vertices arising from the decay of the long-lived mesons and baryons. We thus take the fundamental alignment limit at the event reconstruction level to be the impact parameter resolution in the plane perpendicular to the beam. Monte Carlo studies indicate an impact parameter resolution for high-momentum tracks of roughly 20 μm for silicon strips having a 50 μm pitch.

In order to assess the impact of detector misalignments, we consider the change in the

Misalignment Source	Tolerance (Entire Det.)	Tolerance (Ladder Segment)
Lateral Shift (ends)	25 μm	25 μm
Radial Expansion	170 μm	170 μm
Tilt	60 μrad	420 μrad
Ladder Rotation	——	670 μrad

Table 3.1: Misalignment values corresponding to the maximum allowed coherent variation for the case in which only global position corrections are available. The half length used in computing the angular requirements is 6 cm for a ladder, and 40 cm for the complete detector. The values in the line labeled "Lateral Shift" and the line labeled "Tilt" are related via Shift = (Tilt) $\times$ (half length).

mean of the impact parameter distribution for high-momentum tracks when the detector is moved from its nominal position. Four types of motion give rise to significant effects:

- Coherent lateral shifts of ladders at fixed radius.
- Coherent radial shifts corresponding to changes in the effective radii.
- Coherent tilts of the detector with respect to the beam.
- Angular rotation of one ladder with respect to others. The rotation considered is about the axis perpendicular to the plane formed by the strips in a detector.

We note that although global coherent lateral shifts do not directly affect the alignment criteria, the results obtained are directly applicable to *e.g.* coherent tilts.

3.3 Tolerances Relating to the Trigger System

As discussed in Section 3.2, the trigger-level constraints arise from the knowledge of the beam position. We thus demand that misalignments bias the mean impact parameter by less than 25 μm, a value equal to half of the beam position error. Two sets of tolerances are derived. The first set is based on the assumption that the only position corrections available to the trigger will be translations of the entire detector. The second assumes the positions of individual ladders can be corrected in real time. Both scenarios assume that no angular corrections are available. Tables 3.1 and 3.2 summarize the tolerances on strip position. The numbers given are absolute upper limits on *coherent* effects. The distributions of impact parameter shifts arising from random effects must have R.M.S. values no larger than $\sqrt{n} \times$ (*coherent maximum*) on any given quantity. Here, n is the number of ladders traversed by a given particle. Based on the current geometry, $\overline{n} \approx 6$, giving $\sigma_{\text{random}} < 2.5 \times$ (*coherent maximum*).

Misalignment Source	Tolerance (Ladder Segment)
Lateral Shift (ends)	$25\,\mu$m
Radial Expansion	Correctable to within $170\,\mu$m
Wafer Tilt	$420\,\mu$m
Wafer Rotation	$670\,\mu$rad

Table 3.2: Misalignment values corresponding to the maximum allowed coherent variation for the case in which individual ladders can be independently positioned. The first line means that the precision of the correction hardware must be better than $170\,\mu$m. The value in the line labeled "Lateral Shift" and the value in the line labeled "Wafer Tilt" are related via Shift = (Tilt) $\times$ (half length).

3.3.1 Tolerances Relating to Event Reconstruction

The offline event reconstruction could incorporate six correction constants – three corrections for the origin and three Euler angles – for each barrel segment, each ladder in a barrel, and each detector on a ladder. This leads to an intractably large number of alignment constants. To limit the number of required constants, we demand that the construction precision implies that only segment and ladder-level corrections are required.

In this case, the alignment tolerances dominantly concern the internal structure of the ladders and have little impact on the overall mechanical design. To see this consider the case of ladders tilting because of stresses induced by the overall ladder support structure. This effect could be corrected during reconstruction using the origin and Euler-angle alignment constants determined from data. Any residual tilt would then come from imperfections in the ladder construction.

There are, however, circumstances relating to the mechanical assembly which could cause ladder-by-ladder distortions not corrected by the six constants described above. For example, if the mechanical support has a different thermal expansion coefficient than the ladders, thermal expansion could cause ladders to bend. Rather than trying to compute tolerances for all such scenarios independently, we note that all distortions can be related to the four effects mentioned in Section 3.2. For example, ladder bending is conceptually identical to a position dependent change in ladder radius. We can thus express the ladder-by-ladder tolerances using the same variables as in Section 3.3. These must then be translated into limits on a specific distortion, *e.g.* bending. We also note that in order to use time-independent alignment constants, thermal and gravitational effects biasing the impact parameter must meet the tolerances given here.

Table 3.3 summarizes the allowed misalignment when requiring ladder-level misalignments to satisfy $\Delta_{\rm IP} < 10\,\mu$m. The numbers given in Table 3.3 are absolute upper limits on *coherent* effects. Limits arising from random effects are related to the coherent limits as in Section 3.3. We note that these tolerances are quite loose, and should pose little problem.

Misalignment Source	Tolerance (Ladder)
Lateral Shift	$10\,\mu$m
Radial Shift	$70\,\mu$m
Wafer Tilts	$170\,\mu$rad
Wafer Rotations	$16\,\mu$m
	(strip offset at detector end)

Table 3.3: Misalignment values corresponding to the maximum coherent variation arising from event reconstruction considerations. The tolerance on the wafer-to-wafer rotations is expressed as an offset from the nominal position at the detector ends.

Bibliography

[1] John D. Hobbs *et al.*, *Assembly Alignment Constraints for the D0 Silicon Vertex Detector Barrels*, D0 Note 2080.

Chapter 4

Mechanical Structure

4.1 Overview

The silicon detector requires suitable mechanical structures and enclosures to provide accurate positioning of the detector elements and an acceptable operating environment for the silicon. To allow optimal reconstruction of events, the positions of detector elements should be known well enough that uncertainties in their positions contribute negligibly to track reconstruction accuracies. This places requirements upon the stability of positions and upon the accuracy with which positions need to be measured. The relative positions of detector elements can be measured and verified using tracks. Limitations in this method and the potential use of silicon in triggering place constraints upon the absolute placement of detector elements as described in Chapter 3 on alignment, Section 5.2 on triggering, and in [1].

The effects of temperature on the performance of silicon are described in Chapter 2 on detectors and radiation damage. To control noise and leakage currents in a high radiation environment, the silicon will be cooled initially to a typical temperature of 15°C. The cooling is provided with a water or water/antifreeze system. The system will be designed to allow the silicon temperature to be lowered another 10°C in order to compensate for the effects of radiation damage. A quasi-hermetic gas enclosure provides a dry environment to control noise generated by leakage currents and to prevent the condensation of water. The same enclosure provides a dark environment to eliminate background from photon-induced signals.

To limit the effects of multiple scattering and the production of secondary particles and showers, it is important that the radiation length of the mechanical structure be low. This implies the use of low radiation length materials and the minimization of the mass of the support structure in a way consistent with the other requirements given above. The combination of these requirements presents a formidable design challenge.

The silicon detector assembly is shown in Fig. 4.1. The silicon wafers are held in two types of units: 120 mm long, 201 mm diameter barrels, in which the planes of wafers are parallel to cylinders about the beam line, and 200 mm diameter disks, in which the planes of the wafers are normal to the beam line. Seven barrel units and 12 disk units provide good acceptance for high-p_t physics while maintaining reasonable acceptance for high η tracks. Six of the disks are interleaved with and attached to barrels to form disk/barrel modules. The remaining disks are located at the ends of the barrel region, three at either end. The length of the central barrel region is 889 mm; the overall active length, including the end

disks, is about 1100 mm. The silicon detector, including cabling and mechanical structures, fits into a 360 mm diameter region.

Both barrel modules and end disks are supported from the top edges of a graphite epoxy composite (GEC) 2.2 m long half-cylinder trough which, in turn, is supported from the ends of the innermost scintillating fiber barrel. The half-cylinder, along with half-cylindrical top covers which are segmented in Z, also provides support for cables, cable connections, and water manifolds. GEC disks at each end of the half-cylinder and a thin covering on the innermost scintillating fiber surface provide a light-excluding dry gas enclosure.

The silicon detector inner radii have been chosen to accommodate a 38.1 mm OD, 0.51 mm wall, beryllium beam pipe which extends to $Z = \pm 762$ mm.

4.2 Barrels

The barrel silicon wafers are mounted in "ladder" structures which serve four purposes:

1. They fix the relative positions of pairs of silicon wafers and provide features which allow the wafers to be accurately positioned in the barrel.

2. They aid in flattening the wafers and in maintaining a flat shape.

3. They hold high density interconnects (HDI's) comprised of SVX-II chips, transceivers, and associated components and artwork. The HDI is located inboard of the end of the detector to minimize dead area.

4. They provide a path by which the silicon and HDI components can be cooled.

4.2.1 Ladders and Bulkheads

In each ladder, two 60 mm long rectangular silicon wafers are mounted end-to-end. Three-chip-wide single-sided ladders and five-chip-wide double-sided ladders are used. A silicon barrel comprises four ladder layers at different radii; each layer consists of an inner and an outer sub-layer. A summary of ladder dimensions is given in Table 4.1.

The mechanical structure of ladders is shown in Figs. 4.2 and 4.3. Two rails, each comprised of a (fiber composite)-Rohacell-(fiber composite) sandwich interconnect and support the silicon wafers. The choice of the fiber composite is based upon measurements made of thermal expansion coefficients and flexural moduli and is described in [2]. A layer of carbon-boron hybrid fibers plus a layer of carbon fibers is expected to be used for each fiber composite. At the HDI end, the rails are bonded to one of two 0.300 mm thick beryllium pieces which provide reinforcement in the HDI region and aid in conducting heat from the HDI components. These beryllium pieces, along with a third piece near the opposite end of the ladder, also provide features used in positioning and holding the ladder.

The ladders are positioned between two bulkheads, a water-cooled "active bulkhead" and an uncooled "passive bulkhead". Radial and azimuthal positions of the silicon are shown in Table 4.2 and Fig. 4.4. The ladders have been grouped into 24 equal ϕ towers centered on the layer 3 ladders. In layers 1 and 2, which have half as many ladders as layer 3, ladder ϕ

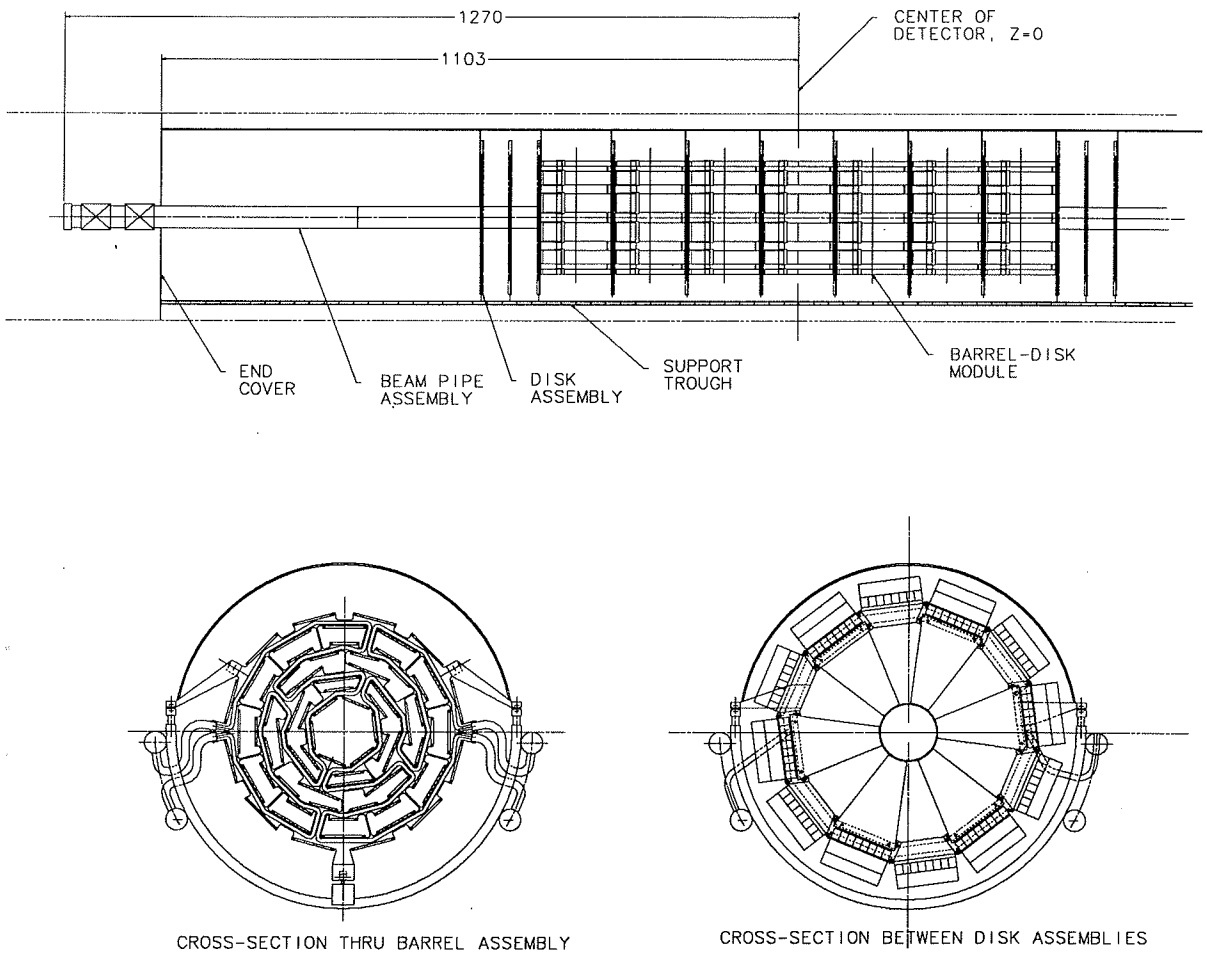


Figure 4.1: Silicon Detector Mechanical Structure

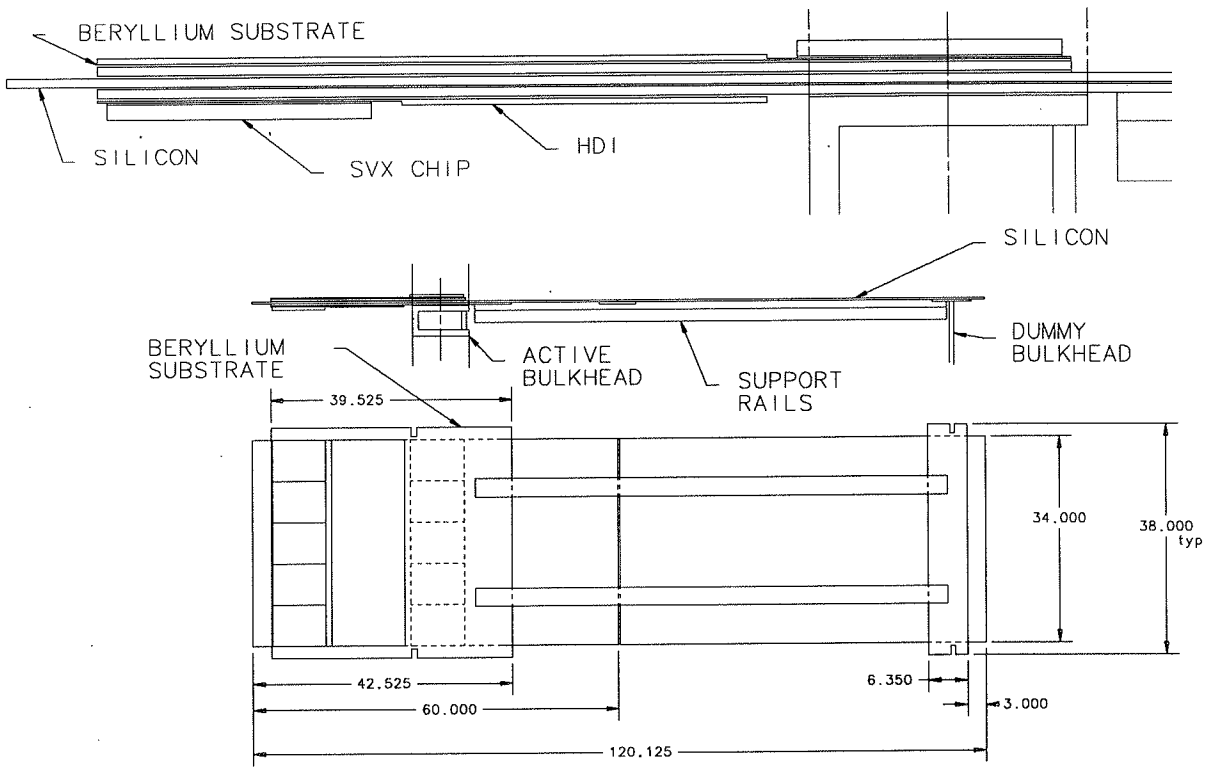


Figure 4.2: Mechanical Structure of 5-Chip-Wide Ladder

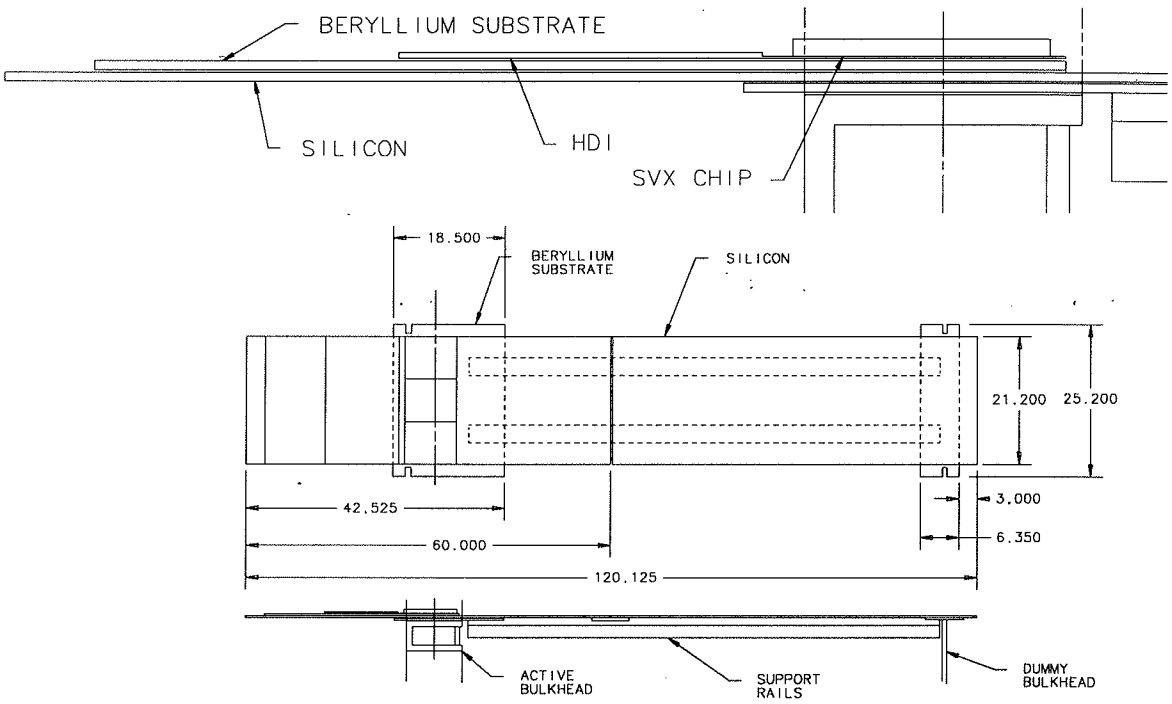


Figure 4.3: Mechanical Structure of 3-Chip-Wide Ladder

Ladder type	3-chip-wide	5-chip-wide
Single/double sided	S	D
Overall length	120.125	120.125
Length of each wafer	60.000	60.000
Wafer-to-wafer gap	0.125	0.125
Length of active portions	116.700	116.700
Maximum HDI width	25.200	38.000
Silicon width	21.200	34.000
Active width	19.200	32.000
Silicon thickness	0.300	0.300

Table 4.1: Ladder dimensions (mm)

positions have been chosen to match the joint ϕ of two adjacent towers. The tower structure is shown in Fig. 4.5. Each tower includes portions of 4 ladders.

Layer	Sub-layer	Ladders per sub-layer	R (mm)	ϕ of lowest ϕ ladder (degrees)
1	Inner	6	27.15	52.5
	Outer	6	36.45	22.5
2	Inner	6	45.50	22.5
	Outer	6	55.54	52.5
3	Inner	12	67.68	15.0
	Outer	12	75.82	0.0
4	Inner	12	91.01	0.0
	Outer	12	100.51	15.0

Table 4.2: Ladder silicon centerlines

Several considerations have driven the choice of ladder locations on the bulkheads.

1. Adequate overlap between adjacent ladders has been provided to ensure complete ϕ coverage within each layer. This places restrictions on the maximum average radius of a layer, given the active widths and numbers of ladders. The effect of overlap has been quantified in two ways: by the number of traces outer sub-layer ladders overlap inner sub-layer ladders for straight trajectories originating at the barrel centerline and by tracing trajectories just grazing adjoining ladder active areas back to the barrel centerline. For the traceback, perfect geometric positioning of the ladders, a track for a 1 GeV/c transverse momentum singly charged particle, and a 2 T magnetic field were assumed. The distance of closest approach is an indication of the amount the beam could be off the detector centerline, or secondary vertices could be separated from the primary vertex, without loss of tracks.

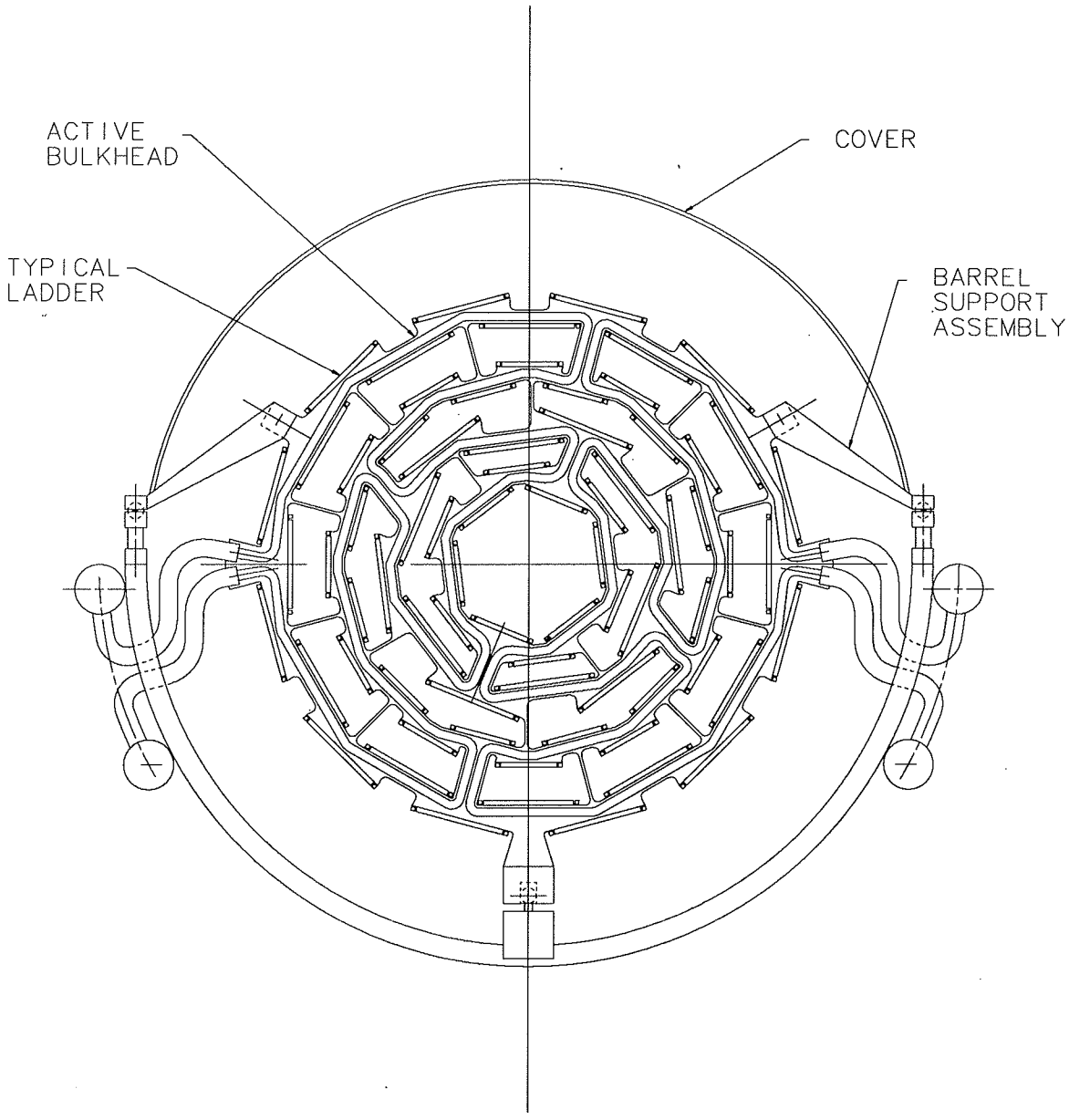


Figure 4.4: Ladder Positions on the Active Bulkhead

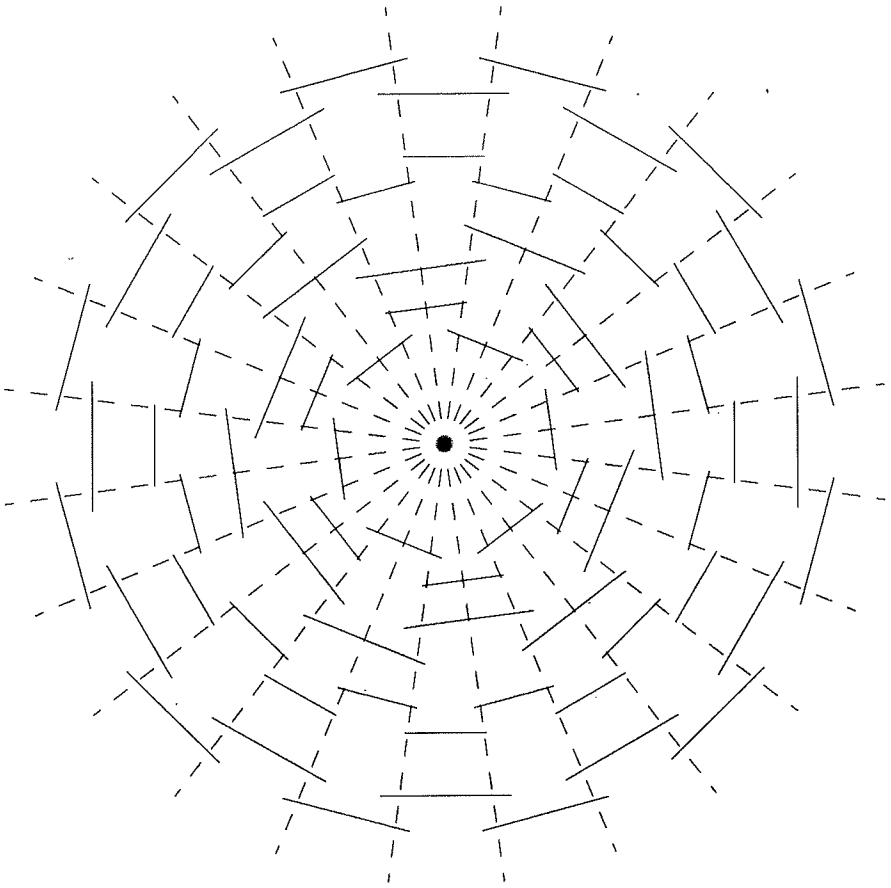


Figure 4.5: Barrel Tower Structure

For single-sided silicon, this calculation is straight-forward. For double-sided silicon, a worst case calculation has been made assuming a stereo angle of 2°. With traces aligned at the extreme readout end of the ladder, a "dead" triangle of approximate height 120 mm and base $(\tan 2°)(120\,\text{mm}) = 4.2\,\text{mm}$ is formed along one ladder edge. The worst case corner of the triangle was used in the overlap calculation. The results for each of the four layers are given in Table 4.3.

Layer	Overlap (expressed as # of 0.05 mm traces)	Traceback offset from barrel centerline (mm)
1	57	8.187
2	15	2.170
3	8	1.631
4	53	20.015

Table 4.3: Worst case overlaps and traceback to barrel centerline for adjoining ladders

2. Sufficient space has been provided between layers to permit ladder installation. The overall ladder radial space for installing ladders is indicated in Tables 4.4 and 4.5, and Fig. 4.6. The minimum bulkhead layer-to-layer radial clearance is 10.25 mm which allows 1.734 mm clearance on either surface of a ladder which is being installed, assuming a ladder is already in place on the opposite sub-layer surface.

Element	Radial height (mm)
Rail	2.500
Adhesive	0.051
Silicon wafer	0.300
Adhesive	0.076
Beryllium	0.300
Adhesive	0.076
HDI under chips	0.061
Adhesive	0.076
SVX-II chip	0.500
Wire-bonds (above chip)	0.500
Total	4.440

Table 4.4: Radial height of a ladder which is being installed

3. The space for a 3.175 mm × 7.366 mm cooling water channel places a lower bound on the sub-layer radial spacing.

4. A minimum space of 5.516 mm is left between inner and outer sub-layer ladder mounting surfaces for cables. Components which extend from the ladder surfaces reduce the clear space for cables to about 2.7 mm.

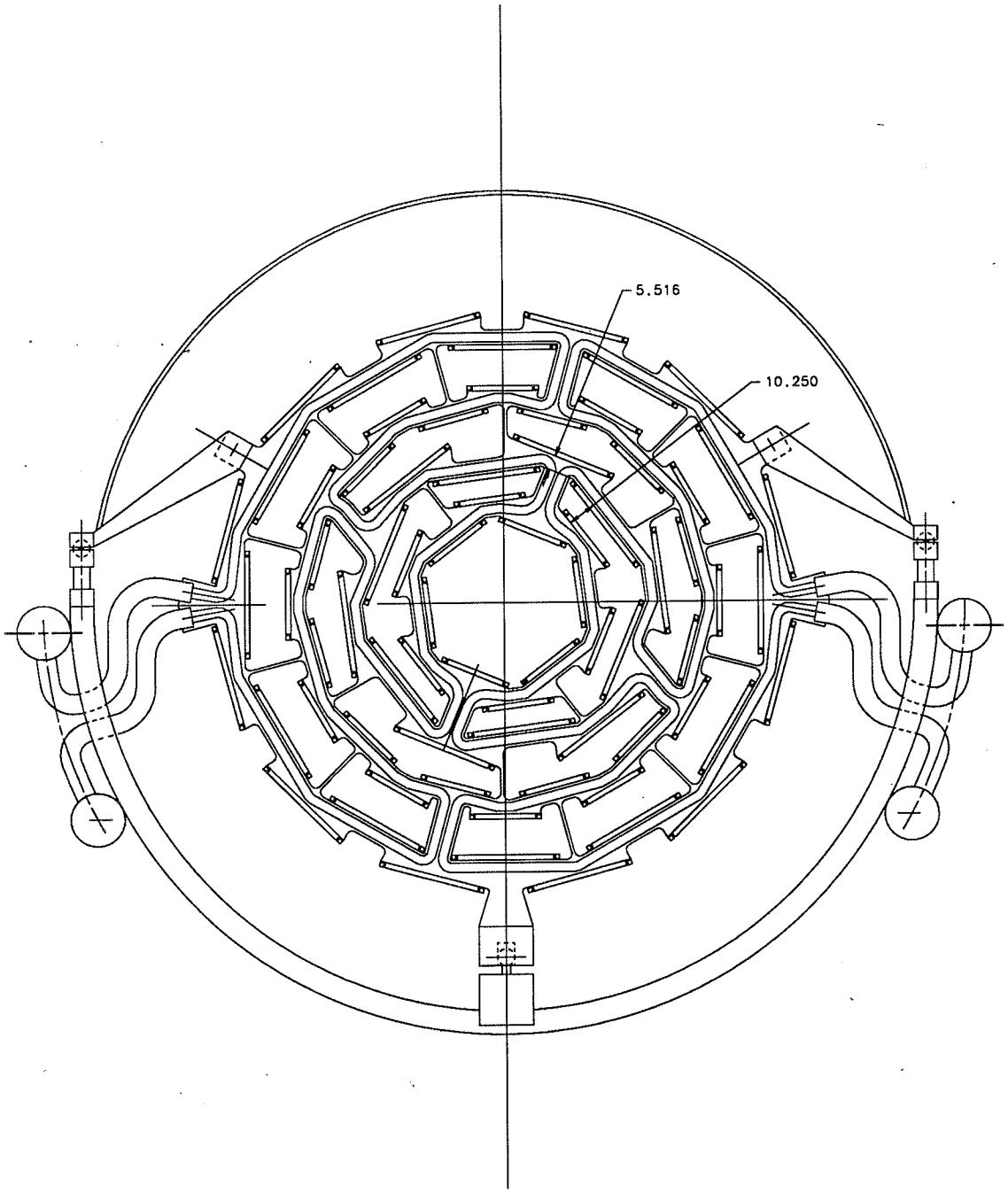


Figure 4.6: Ladder Installation and Cable Space

Element	Radial height (mm)
Adhesive	0.076
Beryllium	0.300
Adhesive	0.076
Silicon wafer	0.300
Adhesive	0.076
Beryllium	0.300
Adhesive	0.076
HDI under chips	0.061
Adhesive	0.076
SVX-II chip	0.500
Wire-bonds (above chip)	0.500
Total	2.341

Table 4.5: Radial height above the bulkhead mounting surface for an installed ladder

5. Space between adjacent ladders of a sub-layer must be left for a 9.398 mm wide layer-to-layer water connection. This limits the minimum radius of a layer, given ladder physical widths and the number of ladders in the layer.

Final machining of the active and passive bulkheads of a barrel is done with the bulkheads clamped together as a unit. This ensures that bulkhead ladder mounting surfaces and mounting features match on the pairs of bulkheads and helps ensure that installed ladders will be parallel to the beamline. Mounting surfaces are machined to a flatness of 25.4 μm and the mounting surfaces on the 9.525 mm thick active bulkhead are perpendicular to the plane of the bulkhead to 25.4 μm. This establishes a maximum ladder slope at the active bulkhead of 25.4/9525 = .00267. Assuming this slope, perfect alignment of the active and passive bulkheads, and the appropriate elastic properties of a ladder, implies about 53 μm maximum radial deflection of the ladder from a straight line [3].

Ladders are positioned laterally with the aid of posts on the active and passive bulkheads which extend from the bulkhead mounting surfaces and engage notches in the ladder beryllium. Only the beryllium piece closest to the bulkhead mounting surface and the edges of the posts closest to the ladder centerline are used for this purpose. Epoxy between the beryllium of the ladder and the bulkhead ensures that ladders do not move once they have been installed. Malleable pins through holes in the posts hold the ladder in place during gluing.

Clearances between notches in the beryllium piece of the ladder and the posts have been chosen so that ladders are placed on each bulkhead with a transverse accuracy of $\pm 6.35\,\mu$m. This accuracy and the accuracy with which silicon wafers are placed relative to the beryllium dominate the parallelism of ladders in a barrel. The absolute radial and ϕ positions of ladders are determined less well. Bulkhead absolute machining tolerances have not been fully determined; we anticipate that cost effectiveness will result in absolute radial positioning tolerances of about $\pm 50\,\mu$m and ϕ direction positioning tolerances of $\pm 25\,\mu$m.

Radial placement depends, in addition, on control of the adhesive thickness which is expected to vary by $\pm 12.7\,\mu$m. Z placement is controlled at the active bulkhead to $\pm 100\,\mu$m, including the effects of lack of bulkhead flatness. The effects of wafer placement with respect to the ladder beryllium must be combined with these accuracies in considering absolute trace positioning.

The ladders play a very important structural role in the barrels. Each barrel is a complete, internally aligned unit. All barrel positioning is done via the active bulkhead. The passive bulkhead is held and accurately positioned by the ladders and sets only the relative positions of ladders.

The barrel structure formed by the ladders and bulkheads must be sufficiently stiff that internal alignment criteria are satisfied under forces from the cables, the water connections, and thermal contraction. The required stiffness is provided without the use of additional structural members by fastening ladders to the bulkheads with epoxy. The total barrel structure has a torsional compliance of $0.11\,\mu$m/N-m assuming that the passive bulkhead positions ladders relative to each other only in r and ϕ [4]. Uncontrolled forces on the barrels are expected to be approximately 1 N. This leads to a negligible shift in ladder ϕ positions. Shear stresses in the most highly stressed epoxy joints with a 1 N force applied to the passive bulkhead at a radius of 100 mm are 0.0050 MPa, a factor of more than 1300 below the shear strength of the electrically and thermally conductive adhesive we anticipate using (*e.g.,* TraCon 2902 silver-filled epoxy). This adhesive has sufficient shear strength under the expected loadings, yet its strength is low enough that the epoxy joints can be separated for ladder removal using simple fixturing.

4.2.2 Barrel Cabling

The cables from the ladders are part of the HDI. They emerge at the HDI edge, follow paths between and around ladders to the outer radius of the barrel, penetrate the support half-cylinder (or its covers), and connect to matrix cards mounted on the outside. A fifth bulkhead ring is provided at a radius of about 130 mm to anchor the cables. The cables are grouped at the fifth ring into bundles which are brought through the half-cylinder and its covers at 1:00, 3:00, 5:00, 7:00, 9:00, and 11:00 o'clock as shown in Fig. 4.7.

Although the cables are malleable, tests with cable material have indicated that sharp bends are difficult and that bundles of cables can exert substantial forces on ladders [5]. Bend radii have been maximized within the constraint that the cables of installed ladders should not obstruct the installation of other ladders. The path segments at constant r lie between two ladder surfaces. Adequate protection of the surfaces will need to be provided. Initial testing suggests that RTV615 (General Electric) may be suitable for potting and protecting wire-bonds.

It may be necessary to fasten cables to extensions from the bulkhead at each layer. A cabling and ladder installation test of an earlier bulkhead geometry was made with a G-10 model and a second model with the present geometry is being prepared.

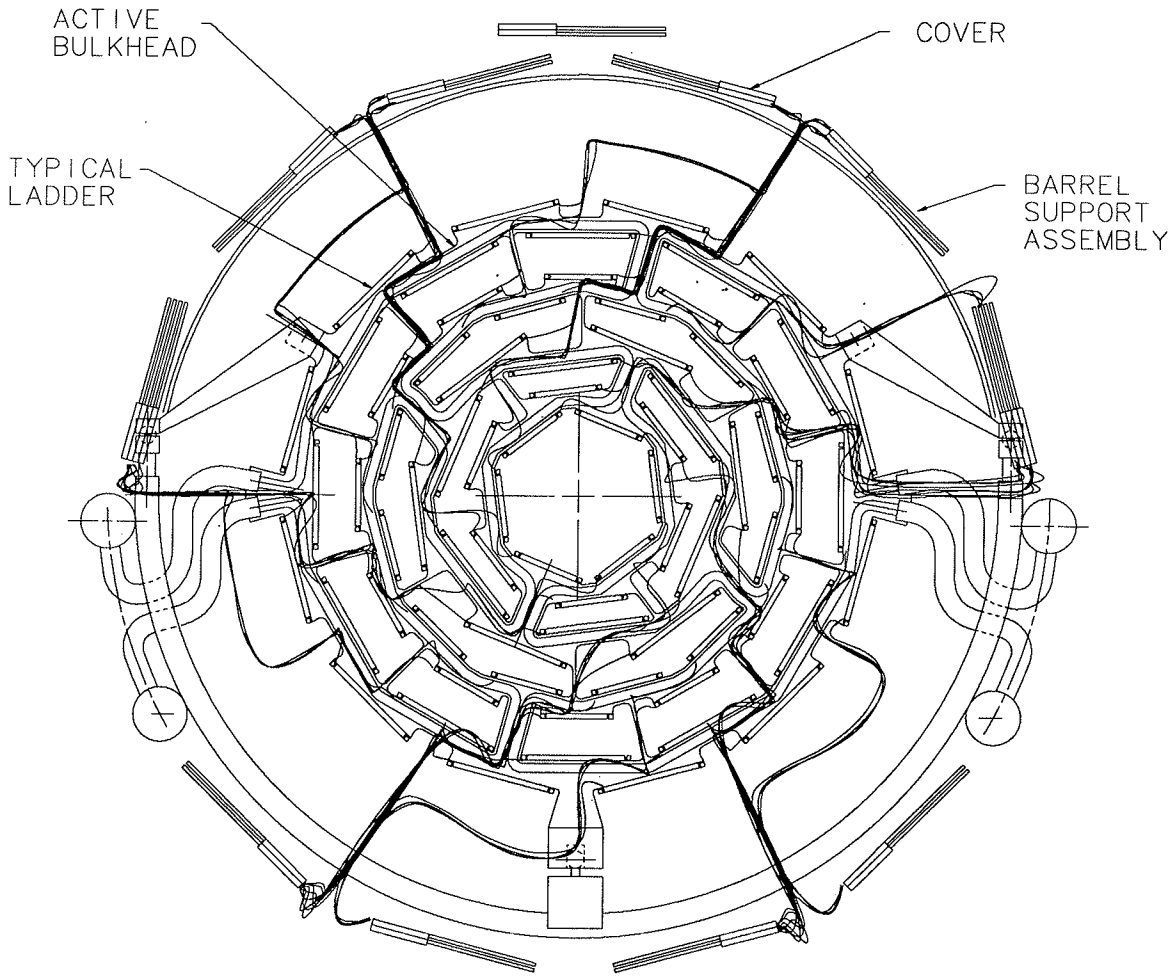


Figure 4.7: Barrel Cable Paths

4.3 Disks

4.3.1 Disk and Wedge Structure

Each disk (Fig. 4.8) contains 12 double-sided, wedge-shaped silicon detector wafers ("wedges"). The wedges alternate from one surface to the other of a beryllium, 15.7 mm × 2.5 mm cross-section, dodecagon support structure. A 7.5 mm × 1.0 mm channel in the beryllium provides a path for water flow to cool the wedges. An additional support ring, which we tentatively plan to make from a short cylinder of carbon fiber, locates wafers relative to each other in Z near the beam pipe; the inner tip of each wedge extends partially through the ring. Disks are oriented so that the wedges match the barrel towers.

A wedge detector and its readout package are shown in Fig. 4.9. Separate 8-chip-wide HDI's are used to read out the two sides of a wedge. Both HDI's of a wedge share a single beryllium substrate. The silicon wafer is bonded to the inner edge of the beryllium with epoxy. A thin (about 25 μm) layer of kapton between the beryllium and the wafer ensures that there will be no inadvertent electrical contact. Wire-bonds are made directly from the trace bond pads to the SVX-II chips on the silicon surface further from the cooling channel. A kapton/copper/kapton jumper with wire-bonds on either end connects the silicon to SVX-II chips on the surface closer to the cooling channel.

The disk thickness contributes to the Z-gap between adjacent barrels. To minimize this thickness, the HDI containing SVX-II chips, transceivers, and associated components, has been placed at the outer periphery of the wedge. The thickness of the structure is 4.850 mm at the detector wafers and 6.322 mm at the SVX-II chips (including 1 mm for two sets of wire-bonds). With additional clearance to avoid potential interferences and accommodate thickness variations, the interleaved disks fit within a barrel-to-barrel gap of about 8 mm.

The uncertainty in disk thickness depends upon the accumulation of tolerances in individual pieces and in the adhesive layers. Piece part tolerances are roughly $\pm 13\,\mu$m for the beryllium substrate, $\pm 10\,\mu$m for silicon wafers, $\pm 13\,\mu$m for the copper/kapton under the SVX-II chips, $\pm 13\,\mu$m for SVX-II chips, $\pm 10\,\mu$m for the kapton/copper/kapton jumper, and $\pm 50\,\mu$m for the beryllium cooling tube. The adhesive thickness varies $\pm 13\,\mu$m per layer. Taking into account the likelihood that a pair of wedges on opposite sides of the cooling channel is near the maximal limits leads to a maximum thickness uncertainty of about $\pm 200\,\mu$m. Lack of flatness of the wedges is expected to contribute $\pm 50\,\mu$m uncertainty per wedge for a total variation in disk thickness of $\pm 300\,\mu$m. The Z-distance between central planes of upstream and downstream wafers in a disk is expected to vary by not more than $\pm 190\,\mu$m.

Four holes in the beryllium substrate and matching holes in the support tube are used to hold and position each wedge on the support tube (Fig. 4.10). Double-ended inserts pressed into the support tube holes provide pins at locations "A" to position the wedge and threaded holes at locations "B" to hold the wedge. One of the "A" holes positions in both r and ϕ, the second only in r. The holes in the support structure will be located to $\pm 10\,\mu$m in the radial and ϕ directions. Wedge wafers will be positioned on the beryllium substrate using holes "A1" as references. The accuracy of this positioning is expected to be $\pm 10\,\mu$m. Thermally conductive grease provides a heat transfer path from the wedges to the cooling tube. An electrical connection is provided by the wedge mounting screws.

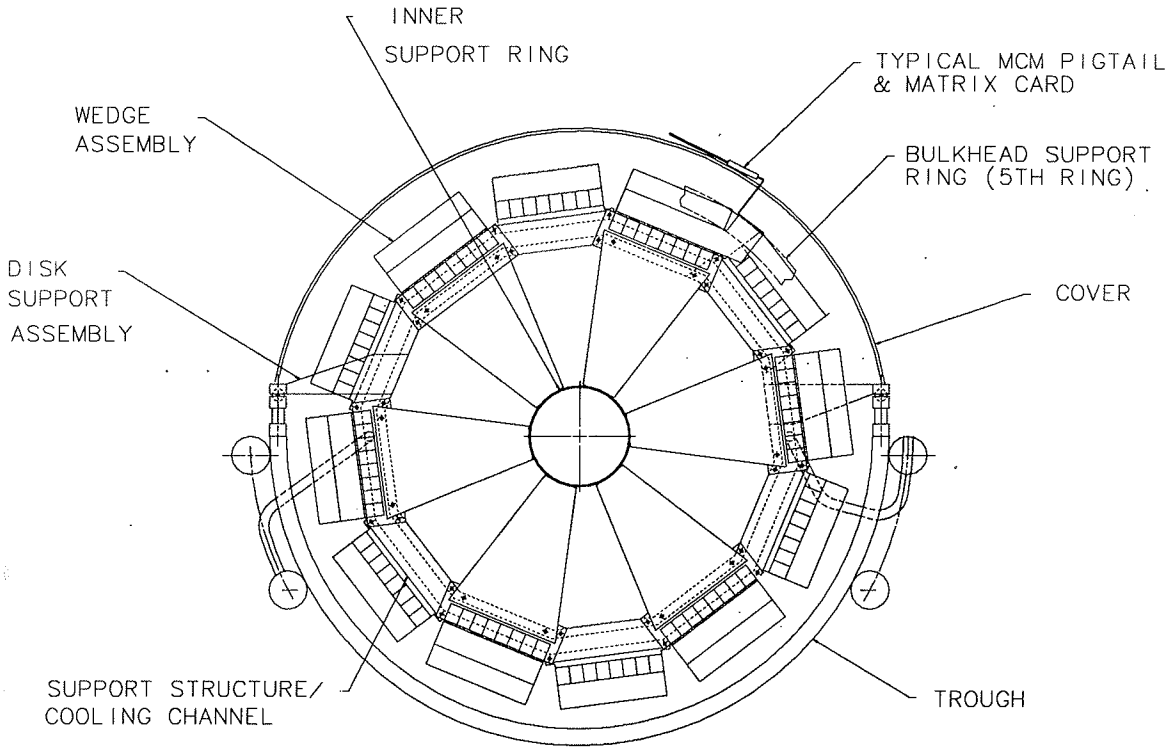


Figure 4.8: Disk Detectors

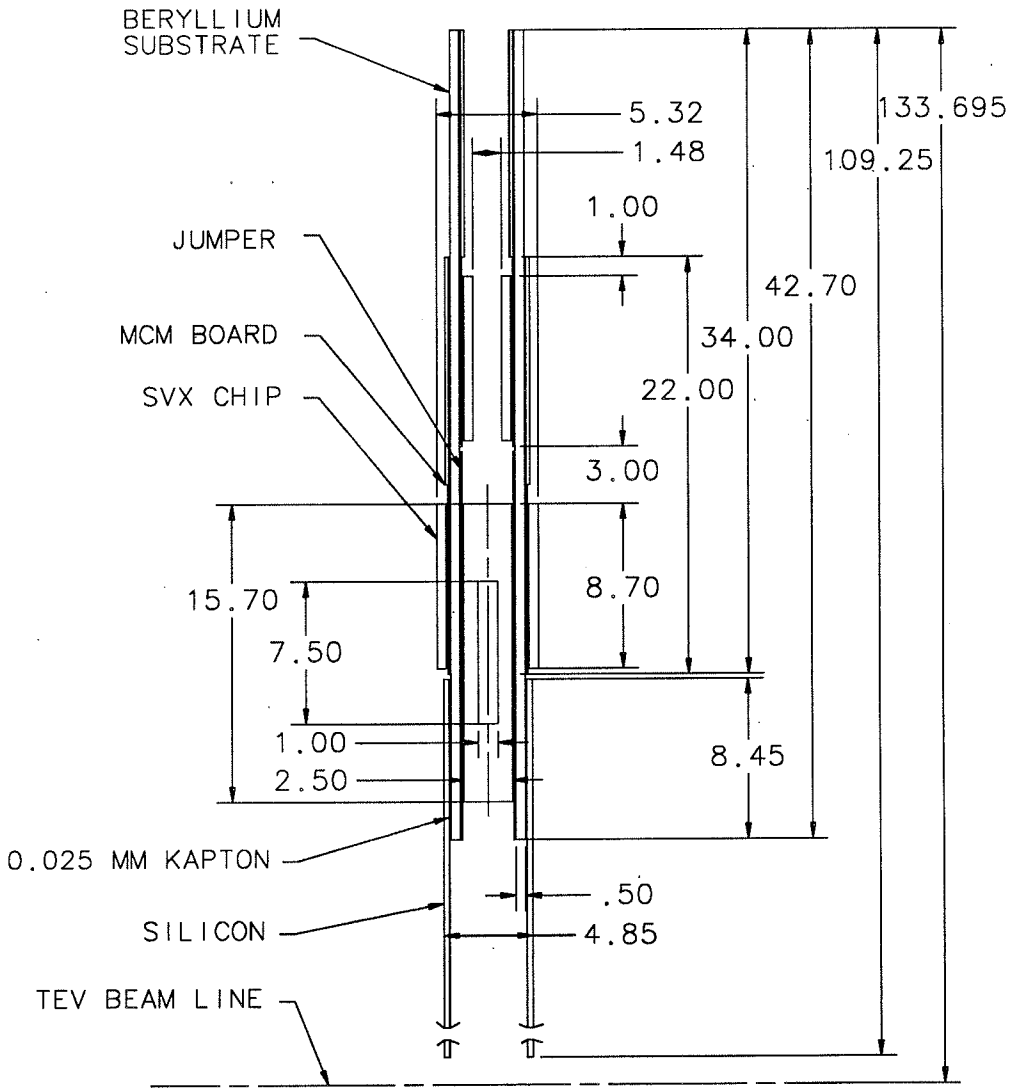
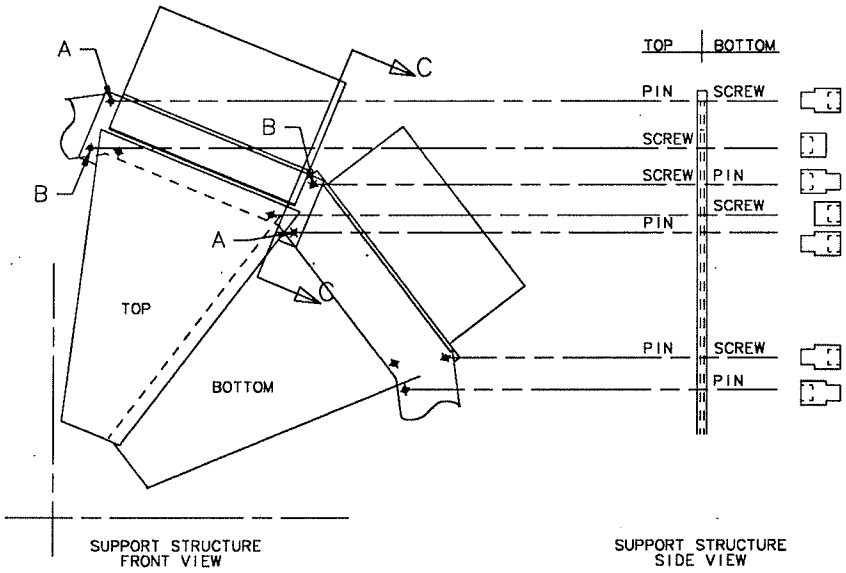


Figure 4.9: Cross-section of a Wedge Detector



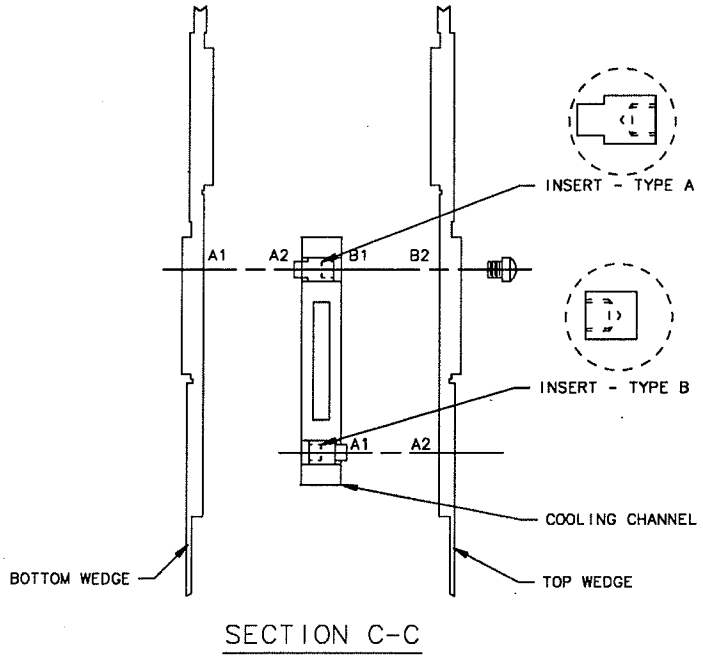


Figure 4.10: Method of wedge attachment

4.3.2 Disk/Barrel Modules

The six interleaved disks are each attached to the active bulkhead of a barrel to form a disk/barrel module. This permits the disk and barrel to be accurately matched and to be installed as a unit. Each of the interleaved disks is attached to a barrel at three points spaced evenly in ϕ. The connection is made via 9.525 mm OD GEC cylindrical posts and screws (Fig. 4.11). The posts will be permanently attached to inserts in the disk support tube. Final machining of the bulkhead end of the posts will be done with the posts attached to the disk structure to provide accurate alignment.

4.3.3 Disk Cabling

Signals from the HDI electronics are transmitted by flat "pigtail" cables which extend from the HDI edge. The pigtails are fabricated with an immediate 105° in-plane bend and follow a constant ϕ, constant Z path to the outer radius of the disk structure (Fig. 4.8). A clip at this radius redirects the pigtail in Z toward the fifth barrel ring in disk/barrel modules and toward a cable collection point in the end disks. The cables are fabricated with a 90° out-of-plane bend which reorients them so that they can penetrate the support half-cylinder (or its covers) and connect to matrix cards located on the outside surface.

4.4 Module Support

The disk/barrel modules and end disks must be mounted from the support half-cylinder in a way which adequately resists the known gravitational forces and the somewhat variable forces from cabling and water connections. Provided that temperature distributions are sufficiently independent of ϕ, thermal contraction effects should be predictable. The thermal contraction coefficient of beryllium, 11.6 ppm/°C, leads to a known radial contraction of 21 μm for a 100 mm radius structure which is cooled from 23°C (room temperature) to 5°C. Since the connections from disks and disk/barrel modules to the support half-cylinder are all nearly identical, the vertical centerlines of these structures should move together and good relative alignment should be maintained.

The support half-cylinder is described in Section 4.6. GEC extensions from the active bulkheads connect disk/barrel modules to the half-cylinder at 2:00, 6:00, and 10:00 as shown in Figs. 4.4 and 4.12. The 2:00 and 10:00 connections control Y and Z positions. Pairs of leaf springs allow motion in X but are stiff in Y and in Z. A sapphire ball between the half-cylinder portion of the coupling and the barrel portion of the coupling permits angular orientations to be matched during assembly; a screw through the ball locks the angular orientation once the module has been positioned. Adjustment in Y is provided by shimming. Adjustment in Z and pre-adjustment in X are provided via oversized holes and locking screws. The adjustment range is 1 mm total in X and in Z.

The 6:00 connection controls X and Z positions. This connection consists of a cylinder on the bulkhead and a ball on the support half-cylinder. A 1 mm total adjustment range in X and Z is provided in the ball mount to the half-cylinder.

Extensive compliance measurements have been made on an aluminum prototype bulkhead with an earlier 3-layer geometry [6]. Measured compliances were scaled by a factor

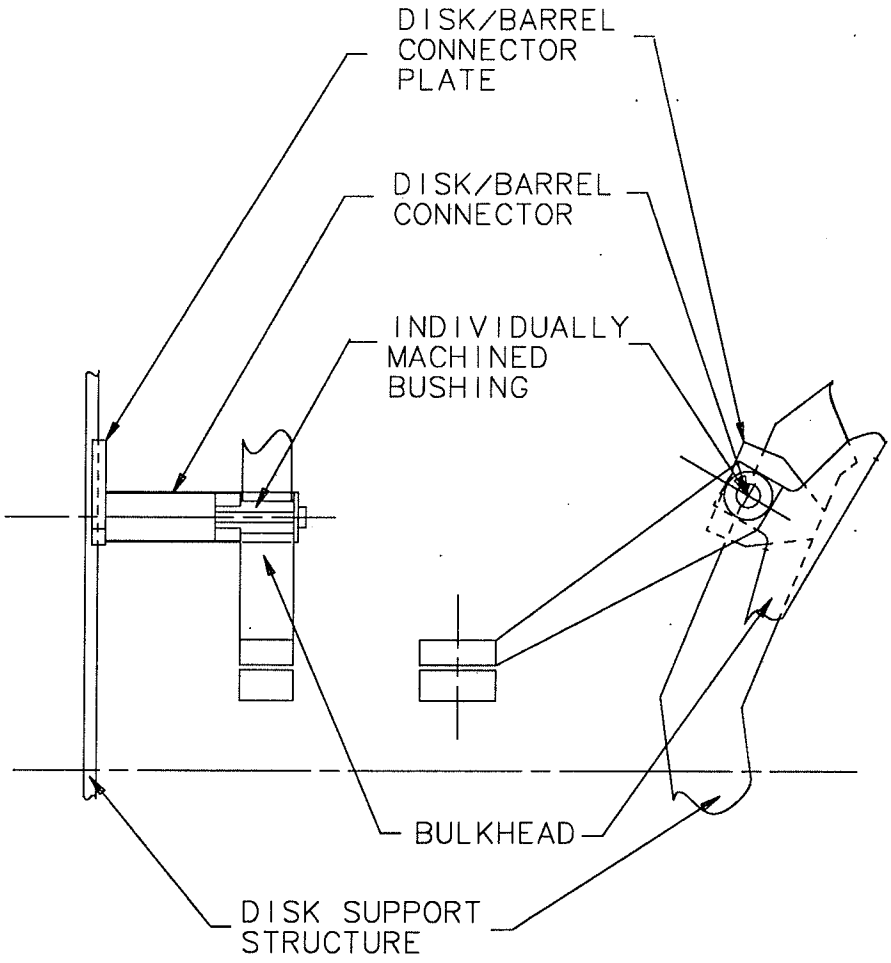


Figure 4.11: Disk/Barrel Connection

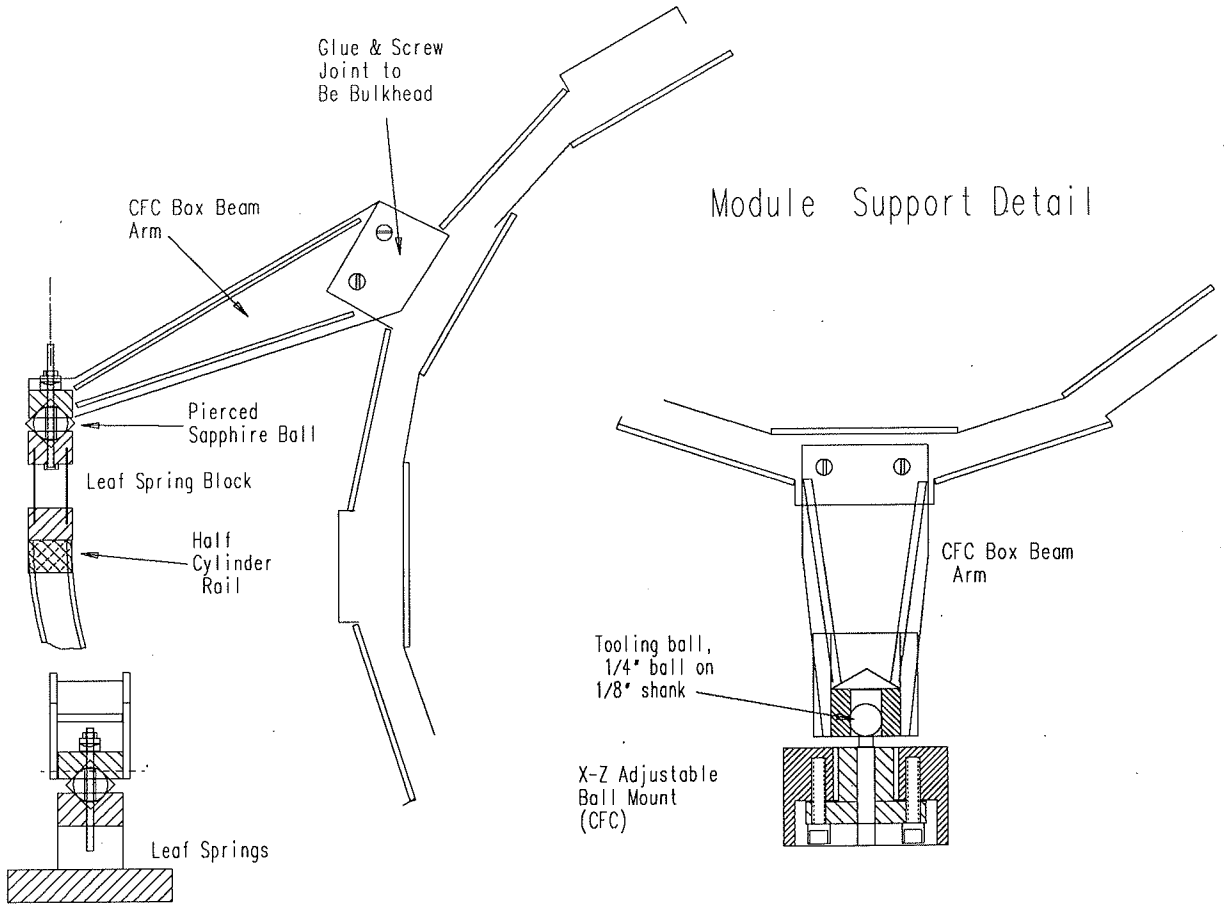


Figure 4.12: Disk/Barrel Module and Disk Support

of 0.2 to take into account differences in geometry and the higher elastic modulus of beryllium. Predicted beryllium bulkhead deflections are about 0.4 μm with the forces expected from the cables. Deflections related to the bulkhead mounting extensions depend on details of the bulkhead structure which are not well represented in the aluminum prototype. Layer-to-layer struts in the beryllium bulkhead design stiffen the bulkhead substantially; measurements remain to be made on a truly representative structure.

The maximum uncontrolled force acting upon a bulkhead is expected to be about 1 N if cables and water lines are carefully pre-formed. Measurements were made of the full barrel support structure with a solid aluminum disk substituted for the bulkhead. The measured Y compliance of 1.3 μm/N should be fully satisfactory. Z compliance was measured to be 3 μm/N near the 3 o'clock support and 5.5 μm/N near the top of the bulkhead.

The method of supporting end disks from the half-cylinder has not been fully determined. One option is to combine the sets of three end disks into end disk modules using GEC posts located every 120° in ϕ. The center disk of the three disks would be rotated 30° (preserving the ϕ tower structure) to achieve unobstructed access to the disk support tube. The module would be supported from the center of the three disks (Figs. 4.8 and 4.12) in a way similar to that used for barrel/disk modules.

4.5 Cooling

The heat to be removed from detector mounted readout electronics is summarized in Table 4.6. A combined power dissipation for the SVX-II chips, transceivers, and other HDI components of 5 mW per detector channel has been assumed. Dissipation in cabling is expected to bring the total power dissipation above 3600 W.

Elements	(Watts)		(Watts)
Barrel ladders	Dissipation per ladder	Ladders per barrel	Heat load per barrel
3 chip wide	1.92	36	69.12
5 chip wide	6.40	36	230.40
Total			299.52
Disks	Dissipation per wedge	Wedges per disk	Heat load per disk
	10.24	12	122.88
Barrels	299.52 per barrel	7 barrels	2096.64
Disks	122.88 per disk	12 disks	1474.56
Detector total			3571.20

Table 4.6: Detector Power Dissipation (Watts)

A variety of methods to remove heat were considered including the use of forced gas flow, forced liquid flow, and evaporative cooling. Water cooling has been chosen because of the favorable heat capacity of water and the simplicity of water systems. With pure water at a temperature of +5°C, a flow rate of 856.7 grams/second (13.58 gallons/minute) will limit the rise in water temperature to 1°C.

The flow diagram for the water cooling system is shown in Fig. 4.13. The system will consist of a reservoir, pump, flow control valve, deionizer, vacuum system, supply lines, return lines, and instrumentation. All of the major equipment will be located on the assembly hall south sidewalk. The pump will circulate approximately 20 gpm of coolant. At this flow rate, the barrels, disks, and manifolds produce an aggregate pressure drop of 5 psi. To prevent coolant from leaking onto the detector components if leaks occur, the coolant pressure of the supply manifold at the detector will be maintained at about 13.7 psia. This pressure can be easily achieved and controlled with a small vacuum pump and regulator. In addition, this pressure does not pose any cavitation problems. For a more complete discussion of the design, please refer to [7].

The system is expected to be operated initially with +5°C deionized water as the coolant. Cooling passage sizes have been chosen so that pressure drops are acceptable with a 24% ethylene glycol/water mixture, which has a freezing point of about −10°C. Materials have been chosen so that a 16% methanol/water mixture could be used, instead. Either of these coolants would allow silicon temperatures to be lowered at least 10°C below their operating temperatures with pure water (about 15°C).

4.5.1 Water Manifolds

Four water manifolds, two supply and two return, provide coolant flow to the barrels and disks. Each barrel requires two supply and two return connections, as shown in Fig. 4.14. The cooling channel of each layer of a barrel bulkhead is divided into equal left and right portions. The left portions of all layers are connected in series between the left supply and return manifolds. Similarly, the right portions are connected in series between the right supply and return manifolds. Layer-to-layer connections are machined as part of the bulkhead beryllium structure. The nominal flow per bulkhead half is 35.6 grams/second for 5°C water.

Disk water flow is divided between equal length upper and lower paths (Fig. 4.14). The two paths share water connections at 3:00 and 9:00. To equalize flow rates in the supply and return manifolds, the flow direction is reversed from one disk to the next. The nominal flow per disk is 29.2 grams/second for 5°C water.

Water connections from the disks and disk/barrel modules to the manifolds will be made with flexible tubing. The tubing material has not been determined, but silicone rubber is under consideration. An effort will be made either to orient the tubing so that its fabricated shape conforms reasonably to the desired path or to pre-form the tubing. Tubing connections have been located near the disk and disk/barrel module supports to minimize distortions the tubing might create in the detector structures.

The flow diagram for the manifolds and detectors is shown in Fig. 4.15. A set of supply and return manifolds is located on the outer surface of the half-cylinder near 3:30; a second set is located near 8:30. All water is supplied to the south end of the detector and returned from the north end. The two supply manifolds enter the half-cylinder region as 15.875 mm inside diameter lines. Approximately 700 mm along the half-cylinder, after supplying the end disks and the first barrel/disk module, both lines reduce to 12.7 mm. After 250 mm and two more modules, they reduce again to 9.525 mm, and then 7.938 mm. The return manifolds begin as 7.938 mm inside diameter lines at the same Z location as the last end

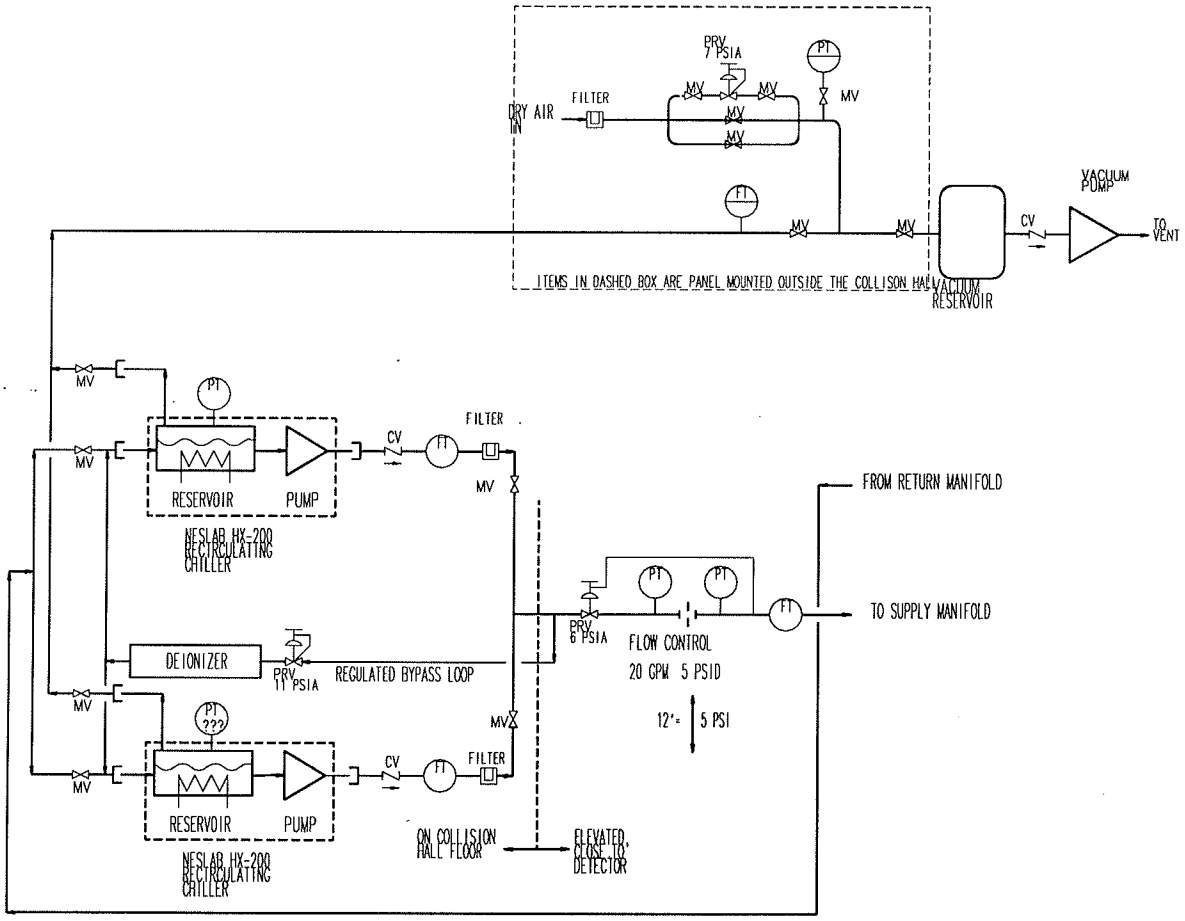


Figure 4.13: Cooling Water System

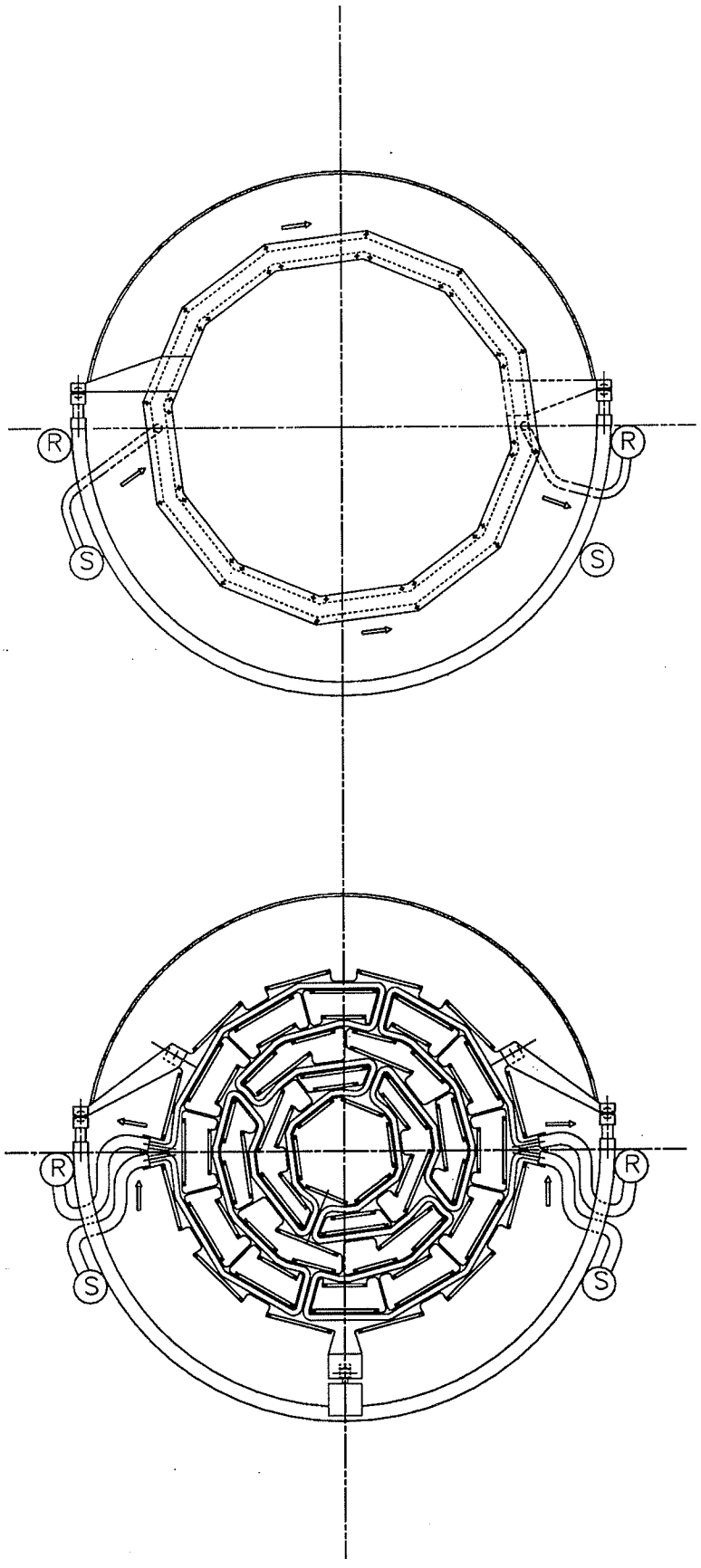


Figure 4.14: Detector Water Channels and Connections

disk. As the return manifolds progress in Z, they increase in size to 9.525 mm, 12.7 mm, and finally 15.875 mm. They exit the half-cylinder region as 15.875 mm lines. This configuration of reducing supply manifold size and increasing return manifold size produces evenly divided flow to the detectors. We expect to make the manifolds from either thin wall metal tubing or plastic tubing. Some portions of plastic tubing will be used in any case to satisfy a tentative specification of 3 MΩ or higher electrical isolation for all but the primary detector ground connections.

4.5.2 Ladder Temperatures

The temperature distributions in the HDI region of ladders have been studied using finite element analysis (FEA) (Zhijing Tang, Fermilab Analysis Group) and using analytic methods [8]. The double-sided ladder structure on which the FEA was based is shown in Fig. 4.16. The 0.3 mm thickness of the beryllium heat spreaders was chosen to minimize mass while still retaining acceptable thermal performance. Significantly lower (45%) adhesive thermal conductivities have been measured than the 1.6 W/(m-K) assumed in the analysis [9]; a portion of the thermal performance can be regained by reducing the adhesive thickness below the 75 μm upon which the analysis was based. Heat transfer by convection and radiation is small in comparison with that by conduction and was assumed to be negligible. The two dimensional analyses made assumed a heat flux of 8.359 mW/mm^2 at the SVX-II chips and 5.387 mW/mm^2 in the transceiver region. The maximum silicon and component temperatures were found to be 22.5°C and 26.5°C, respectively, for a cooling tube surface temperature corresponding to +5°C water.

Single-sided ladders have the same beryllium heat spreaders as double-sided ladders but no HDI is present on the surface closer to the cooling tube. As a result, temperatures in single-sided ladders will be noticeably lower than those in double-sided ladders. A complete thermal analysis of single-sided ladders remains to be done.

4.5.3 Wedge Temperatures

Finite element analyses for double-sided wedges were made with an earlier HDI geometry but have not been done with the latest geometry. Component temperatures are expected to be somewhat higher than those in the double-sided ladders. Because no portion of the silicon wedge extends beneath the HDI, however, maximum silicon temperatures should be only a few °C above the cooling tube metal temperature.

4.5.4 Ambient Temperature Analysis

The 5-chip ladder FEA solution was expanded to study the equilibrium gas temperature within the silicon detector volume [10]. A cooling channel surface temperature of 8.5°C was assumed, based on a bulk water temperature of 5°C and measurements of the metal-to-water temperature difference. Localized film coefficients were calculated on a per node basis as a function of temperature difference between the surface and the average gas temperature. Natural convection over the ladder and bulkhead surfaces was assumed. Iterations were performed to balance the calculated heat flow into the water and the power dissipated by

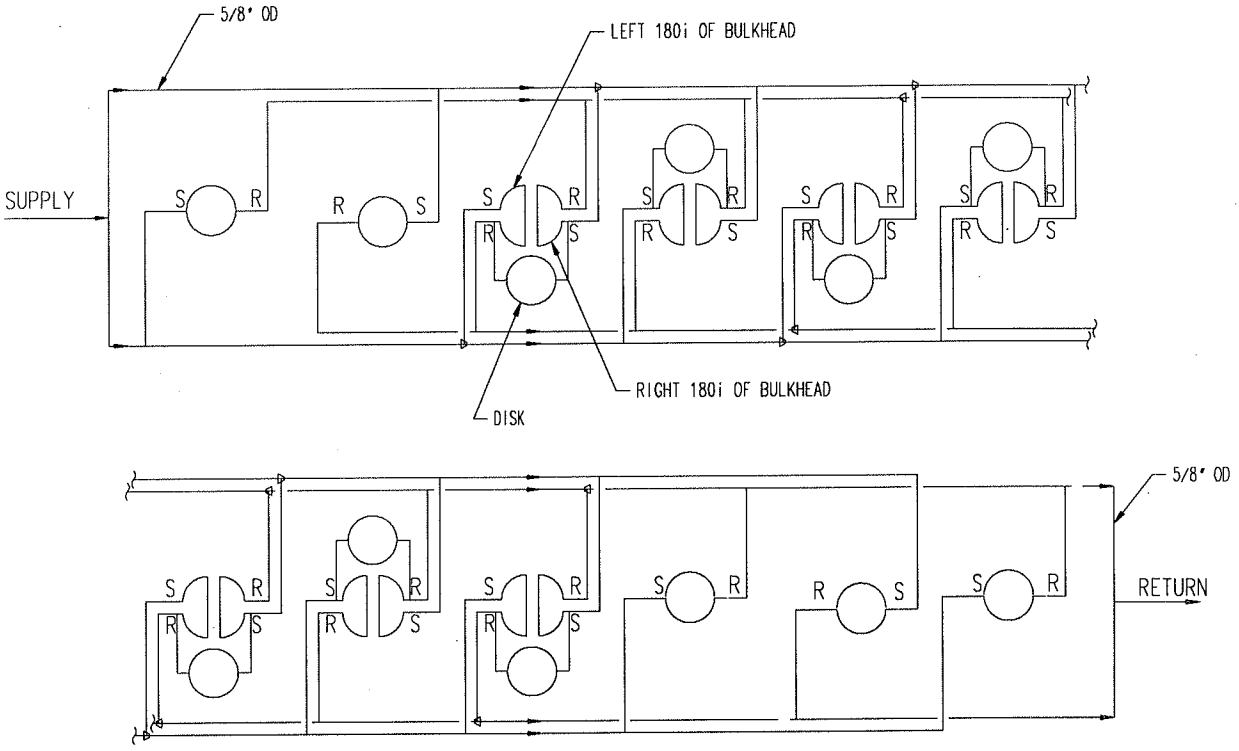


Figure 4.15: Water Manifolds

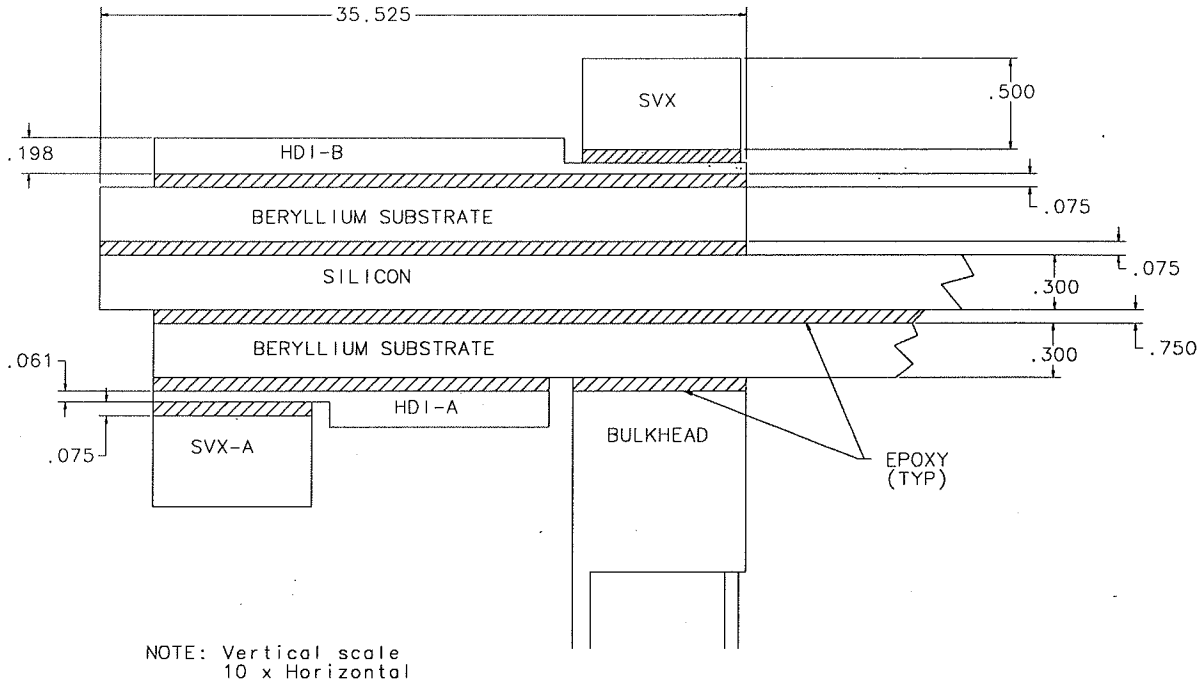


Figure 4.16: Ladder Thermal Structure

the ladder HDI components. An equilibrium gas temperature of 14.6°C was obtained. The silicon temperature distribution as a function of distance from the active bulkhead ladder end is shown in Fig. 4.17.

Heat transfer from the scintillating fibers and through the detector volume end closures and power dissipation on the outside of the support half-cylinder have been ignored in this calculation. About 2.5 W are expected to be transferred from the scintillating fibers assuming the scintillating fiber inner surface is at 23°C. Heat transfer via the end closures should be a small fraction of this value. Although the power dissipation in cabling is not fully understood, it has been estimated to be 30 W. Heat input to the gas from these sources is expected to raise the average gas temperature by 4 to 5°C. It should have a negligible effect on ladder temperatures.

4.6 Half-Cylinder

A carbon fiber half-cylinder (Fig. 4.18) provides accurate and stable support of detector elements. The half-cylinder is 2.206 m long, has an inside radius of 145 mm, and has an outside radius of 153 mm. The half-cylinder consists of 0.9 mm thick inner and outer shells joined by 0.4 mm thick webs. The webs are spaced every 25.65 mm in Z. The ends of the half-cylinder are closed by 2 mm thick full circular disks which have appropriate openings for the beam pipe, cables, and water manifolds.

The support half-cylinder is made from high modulus carbon fiber prepreg plies. The high modulus carbon fiber has a low thermal expansion coefficient, high stiffness to mass ratio, reasonable cost, and acceptable fabrication properties. A low coefficient of thermal expansion ensures that temperature gradients will not cause significant displacements of detector elements in the face of the large thermal gradients expected from the coexistence of cooled surfaces and hot electronic chip modules. The high modulus minimizes deflections caused by gravitational, cabling, and water connection forces. Multiple high modulus carbon fiber plies will be combined at specific angles to achieve a thermal expansion coefficient of approximately 0.5 ppm/°F. Beryllium, for comparison, has an expansion coefficient of 7 ppm/°F. The elastic modulus of the laminate is approximately 124 GPa (18×10^6 psi). This provides a stiffness to radiation length ratio which is 5 times that of steel and 3 times that of aluminum. The outer surface of the half-cylinder will be covered with 15 μm to 25 μm thick aluminum foil to provide electrostatic shielding and a ground connection between disks and disk/barrel modules.

Finite element analyses, confirmed by analytical calculations, predict [11] a maximum half-cylinder deflection of 100 μm and rotations about the X-axis of 70 μradians at the locations of the first and last barrels. Only a portion of this maximum deflection occurs over the length of the silicon tracker itself. Because simulated detector loadings will be applied to the half-cylinder as individual detector elements are positioned, the final detector alignment will reflect only a small fraction of this deflection and rotation.

The half-cylinder is expected to be fabricated at Fermilab. The shells and webs will be made as separate components from several layers of carbon fiber prepreg unidirectional tape. Each component will be formed and cured at an elevated temperature. The components will be assembled to form the half-cylinder structure using room temperature curing epoxy. The

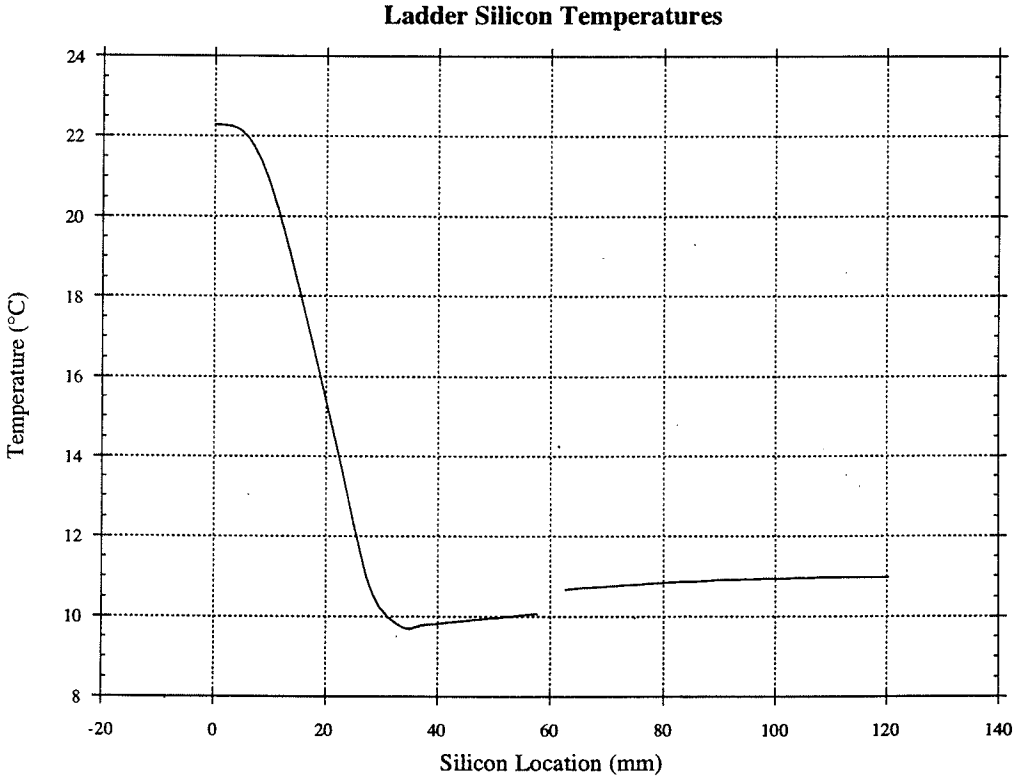


Figure 4.17: Ladder Temperature Distribution

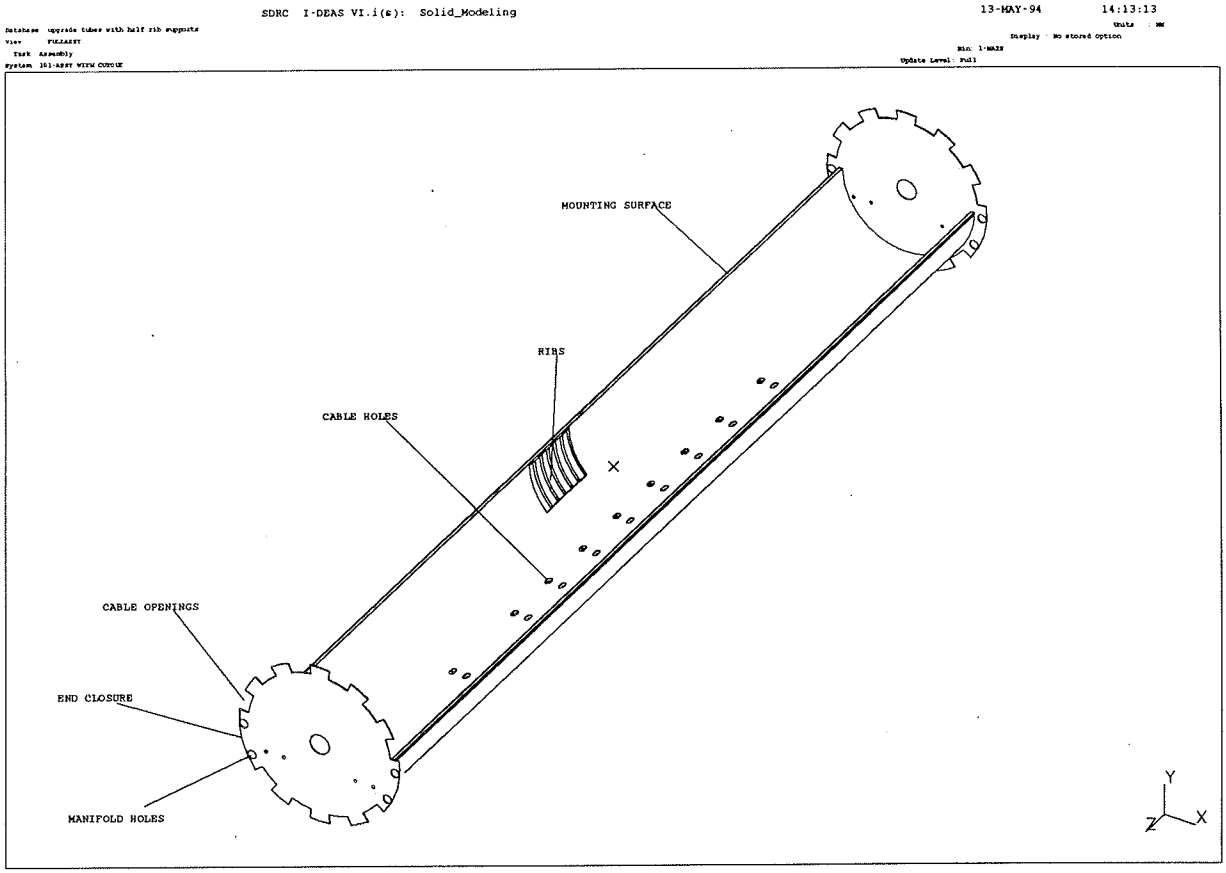


Figure 4.18: Support Half-Cylinder

completed structure will have all mounting surfaces machined, holes drilled, and openings for cables milled on a large CNC router in Lab 8.

The half-cylinder will be supported from the scintillating fiber tracker at two locations at each end. The supports will consist of vertical threaded rods rigidly fixed to the end flange of the inner layer of the scintillating fiber tracker. The tops of the rods will attach to the half-cylinder via mounts adjustable in X and Y.

4.6.1 Top Covers

Covers for the half-cylinder provide a thermal barrier, mechanical and light protection, electrostatic shielding, and a mounting surface for the matrix cards and long flat data cables. Eleven covers will be provided, seven for the barrel/disk modules, two for the two groups of end disks, and two for the remaining unoccupied half-cylinder regions. The covers will consist of a single 1.5 mm thick shell made from high modulus carbon fiber prepreg. Webs on the inner radius shell surface maintain the desired radial shape. The inner radius of the cover shells will match the inner radius of the half-cylinder. While the covers need to provide reasonably tight gas and light sealing, soft mountings will be used to avoid deforming forces on the support half-cylinder. Holes will be provided to allow alignment of the completed assembly to be checked. These holes will be covered with tape or plugged when not in use. The outer surface of the shell will be covered with 15 μm to 25 μm grounded aluminum foil to provide electrostatic shielding.

4.7 Matrix Cards and Cabling

The transitions from the HDI pigtail cables to the flat cables running to the platform are made in matrix cards which are mounted on the outer surface of the half-cylinder. Four pigtail cables are connected to each matrix card. This implies 24 matrix cards per disk/barrel module and 6 matrix cards per end disk. If all cables from a disk/barrel module run in Z to the same end of the detector, then the asymmetry inherent in a detector with seven barrels leads to 90 cables at one end of the detector and 108 cables at the other.

4.8 Beam Pipe

The portion of the Tevatron beam pipe through the silicon tracker will have a 38.100 mm outside diameter and a 0.5 mm thick wall. Bellows and quick-disconnect flanges are provided at each end of the 2.54 m long beam pipe assembly. The central 1.524 m portion will be made of beryllium; the remainder of the assembly will be made of stainless steel.

We expect the beryllium portion of the beam pipe to be fabricated by rolling a beryllium sheet into a round cylindrical shape and overlapping the edges to form a joint. This overlap is approximately 1.5 mm; for that circumferential distance the beam pipe thickness is 1 mm. All beryllium to beryllium, and beryllium to stainless steel joints will be brazed with an aluminum filler material.

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Chapter 5

Readout Electronics and Trigger

5.1 Readout Electronics

The goal of this section is to describe the operation of the readout system for the DØ Silicon Tracker. Cursory descriptions of the major blocks in the system will be given for completeness, but the reader is encouraged to obtain specific information from the component descriptions included in the references. This section is generated based on documentation and understanding of the system as proposed at this date, and is subject to change as documentation and understanding are updated. In some instances, more than one solution is indicated for a given section as more than one option is being investigated.

5.1.1 System Description

The primary function of the system is to move digitized data from the SVX-II chips, mounted on silicon strip detectors located in the central region of the DØ detector, to the Trigger Level-2 section of the Data Acquisition System located in the second floor of the fixed counting house in the DØ Assembly Building. There are two additional functions of the system: 1) provide a digital path to the SVX-II chips for the purpose of downloading parameters and 2) provide a path from the central region of the detector for the purpose of monitoring such things as temperatures, voltage levels and current levels.

The readout system for the DØ silicon tracker is depicted in the block diagram shown in Fig. 5.1. Charge deposited on each silicon strip is collected by an individual channel within a full custom, mixed analog and digital integrated circuit (SVX-II) which is wire-bonded directly to the detector. The charge, stored as a voltage across a capacitor, is digitized by the SVX-II to an 8-bit word. Up to ten SVX-II chips are connected to a kapton/copper flexible printed circuit. This flexible printed circuit, the High Density Interconnect (HDI), contains one 8-bit data bus, (common to all the SVX-II chips) clock and control line traces, bypass capacitors, resistors for chip biasing, and an 8-bit bidirectional cable interface circuit. At the outer radius of the silicon detector region, four HDI's are connected to one 28 ft metallic data path which in turn is connected to one section of a Port Card. Port Cards are mounted in one of eight 9U $\times$ 280 mm crates located in the platform region under the outer layer muon detector. A maximum of 111 Port Cards control the operation of all of the over 6500 SVX-II chips in the detector by sending clock pulses and control signals across over 200 metallic

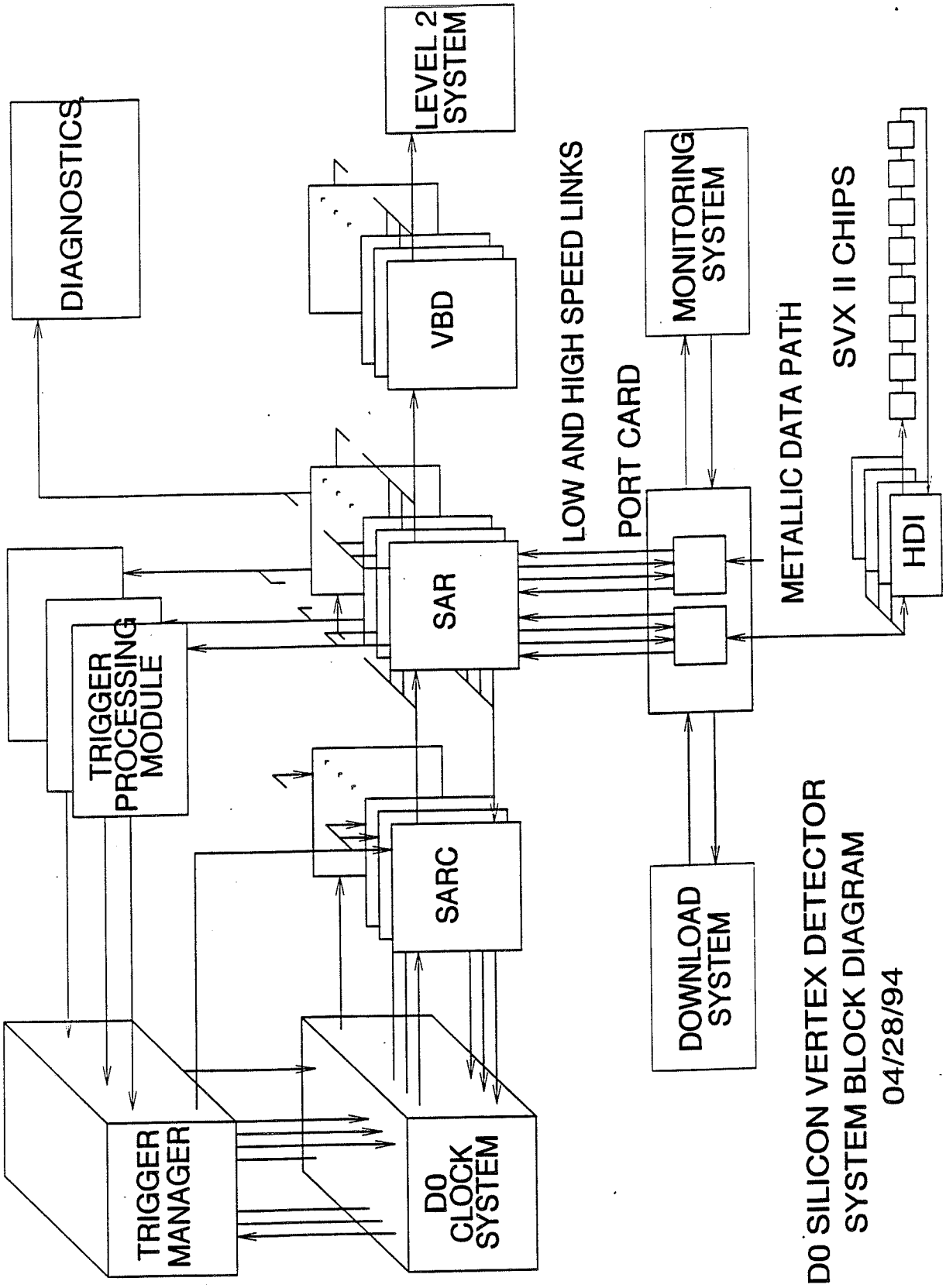

Figure 5.1: DØ Silicon Detector Readout System

data paths. The SVX-II chips respond by sending data and channel information back to the Port Cards at 53.104 MBytes/s. Each section of the Port Card routes the 8-bit data buses from two HDI's to one parallel-electrical to high-speed serial-optical converter circuit. At rates approaching 1 Gbit/s, data is sent through 150 ft of multi-mode fiber optic cable to one section of a Silicon Acquisition and Readout Module (SAR) located in the second floor of the Movable Counting House. Each SAR is connected to two Port Card sections. Up to 16 SAR's can be mounted in one 9U $\times$ 400 mm VME crate but the current design limits this number to eight to reduce event transfer time. Fourteen SAR crates are required. Each SAR crate contains one Silicon Acquisition and Readout Controller Card (SARC) which acts as the interface between the SAR modules and the rest of the data acquisition system. The SARC interprets signals from the DØ Clock System and the Trigger Manager to send commands to the SAR's in the crate which in turn send commands to the Port Cards via a low-speed (53.104 MHz) serial optical link. The transport of the commands from SARC to SAR is via a custom designed backplane in the VME crate. This backplane also distributes the clock and control signals required by the SAR's. The VME Buffer/Driver (VBD) module is also installed in the VME crate. Data collected by the SAR's is read into a dual ported memory in the VBD across the VME backplane and then transported to the Trigger Level-2 system via a 32-bit metallic data path. If the Silicon Vertex Detector is going to be used in formulating the Trigger Level-1.5 decision, then some number of additional VME modules will be designed to process trigger information provided by the SAR's.

A functional description of the major blocks in the system follows.

Trigger Manager

The Trigger Manager system generates the signals which initiate the movement of data from the SVX-II chips to the Trigger Level-2 system. The Trigger Manager also receives a signal back from the SARC indicating that the SVX-II chips are busy, and not capable of accepting additional triggers.

DØ Clock System

The DØ Clock System [1] generates and/or distributes all of the clock signals used by the DØ experiment. Specifically for the Silicon Vertex Detector, the DØ Clock System generates the clock and timing signals (correlated to accelerator operations) required to operate the SVX-II chips and move the generated data.

SVX-II

Designed by a collaboration of engineers at Fermilab and Lawrence Berkeley Laboratory, each SVX-II chip [2] contains 128 identical channels of analog-to-digital conversion/storage and required control circuitry. The SVX-II chip can operate in any one of four operational modes: Initialization, Acquisition, Digitization or Readout. A block diagram for a single SVX-II channel is shown in Fig. 5.2: During an Acquisition cycle, charge deposited on a silicon strip is integrated onto a capacitor in the preamplifier stage of each channel. A 32-stage analog pipeline stores the charge while Trigger Level-1 decisions are being made. Each channel in the chip contains a Wilkenson type analog to digital converter. In response to

SVXII Block Diagram

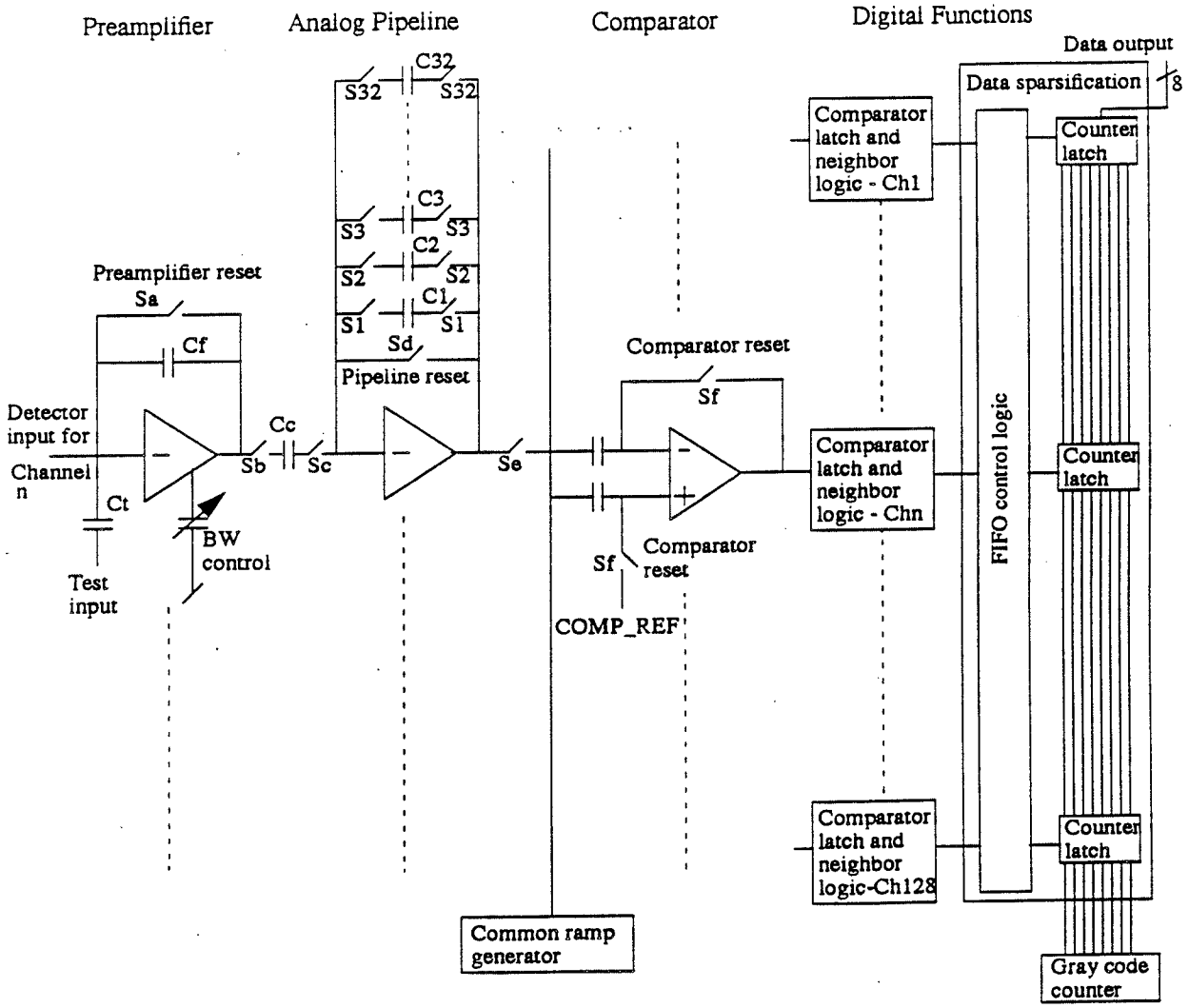

Figure 5.2: Simplified Single Channel Block Diagram

Operation	Frequency	Duty Cycle/Pulse Width
Initialize	1 MHz	50%
Acquisition	7.58 MHz	25 ns
Digitization	53.104 MHz	50%
Readout	26.552 MHz	50%

Table 5.1: Typical frequencies and duty cycles/pulse widths for SVX-II operation modes.

a Level-1 trigger, the charge stored in the pipeline capacitor for all channels in the entire detector is simultaneously digitized into 8-bit Gray-coded words. Each SVX-II chip contains a global digital threshold register. The chip can be set in sparsification mode where only the channels whose digitized voltage exceeds this threshold will be available for readout. This reduction in the number of channels to be read requires that individual channels have some sort of identification so that the location of the "hit" channel is known. Note that the SVX-II can also be instructed to force the readout of channels immediately adjacent (even across chip boundaries) to "hit" channels. During the Readout cycle, each channel participating in the readout will generate an 8-bit channel address word just prior to the generation of the 8-bit data word. At the beginning of the Readout cycle, the SVX-II generates an 8-bit Chip ID number so that channels in that chip can be differentiated from channels in other chips.

Because multiple SVX-II chips share the data bus on the HDI, they must take turns reading out. Readout control is accomplished by the use of a daisy-chain connection between the chips. As one chip finishes its readout, it uses the Top Neighbor pin to tell the next chip in the chain to begin reading out. Besides the 8-bit bidirectional data bus and the priority passing pins, each SVX-II chip has two input pins for the differentially driven clock signal, three input pins which control the operation of the chip and several analog input pins for detector and internal chip biasing and calibration.

The frequency and duty cycle of the input clock signal vary depending on the particular cycle in which the chip is being operated. Typical values for frequency and duty cycle/pulse width for the four modes of SVX-II operation are summarized in the Table 5.1.

During the Initialization or downloading cycle the SVX-II looks like a 182-bit serial shift register. The output of the shift register for one SVX-II is connected to the input of the shift register for the next chip through the Top and Bottom Neighbor pins used to control readout. Thus a serial bit stream of 1820 bits would be required to download an HDI with ten SVX-II chips.

High Density Interconnect

The High Density Interconnect (HDI) is a flexible printed circuit made of multiple layers of copper-clad kapton. Up to ten bare die SVX-II chips and their associated surface mount capacitors and resistors are attached. A bidirectional cable interface circuit receives and sends information on the 28 ft metallic data path connected to the Port Card. One HDI and its beryllium substrate are epoxied directly to one silicon detector. Because there are different types and widths of silicon detectors, there are at least four variations of the HDI.

All HDI's have the same characteristics: 1) one 8-bit data bus connecting all of the SVX-II chips to the data path interface circuit, 2) distribution of the differential input clock and single-ended mode control signals to all the SVX-II chips, 3) distribution of the various analog voltages required by the SVX-II chips and silicon detectors.

The HDI can be considered to be composed of two parts. The first part consists of all of the components (SVX-II chips, resistors, interface circuit) which are mounted in the area which will be in direct contact with the silicon detector. The second part (often called the "pigtail") is essentially an extension of the signal and power traces to the outer radius of the silicon detector region. The 28 ft metallic data path will connect to four HDI pigtails there via a passive interface circuit called the Matrix Card. The Matrix Card will also be a flexible copper/kapton printed circuit. The mechanical/electrical connections of the HDI pigtails to the Matrix Card will be made using "Fujipoly", an array of gold-plated wire stubs in a compressible dielectric. The metallic data path will be soldered to the Matrix Card.

Silicon Acquisition and Readout Controller Module

The Silicon Acquisition and Readout Controller (SARC) Module [3] is a 9U $\times$ 400 mm VME module which controls up to 16 SAR's in a single VME crate. The SARC is designed as a VME slave capable of A24/D32-D16-D08 read and write cycles.

The SARC operates as the interface between one SAR crate and the DØ Clock and Trigger Manager systems. Each SARC in the system receives the same clock, trigger, and control signals from the DØ Clock System at the same time. These signals are distributed or interpreted and propagated, as appropriate, to the SAR's in the crate. The SARC manages the memory buffer allocation in the crate. Each SAR can store events in up to 12 memory buffers. The SARC, using the Fill and Read buses on the J3 backplane, controls which buffers are waiting for Trigger Level-1.5 decisions, waiting for readout by the VME Buffer/Driver, or waiting to be filled with another event. If allocation of the memory buffers on the SAR's or current status of the SVX-II chips is such that additional Level-1 triggers cannot be accepted, then the SARC sends a Busy signal back to the Trigger Manager. In response to a Trigger Level-1-true indication, the SARC latches the current Trigger Acquisition Synchronization Number from the Trigger Manager. In response to a Trigger Level-1.5-true indication, the SARC latches a similar synchronization number associated with the event passed by the Trigger Manager. It is expected that the SARC can use this second trigger number to detect errors in synchronization with the Trigger Manager.

Error detection circuitry for the High- and Low-Speed Links exists in the Port Card and the SAR. Indication of the loss of synchronization in either of these optical links is forwarded to the SARC by the SAR. The SARC responds by issuing the appropriate command and all SAR's in the crate perform the necessary reset operation required to regain link synchronization. During these reset operations, the SARC generates a Busy signal back to the Trigger Manager. The SARC regains synchronization with the Trigger Manager by monitoring event numbers.

Silicon Acquisition and Readout Module

The Silicon Acquisition and Readout (SAR) Module [4] provides VME addressable memory capable of storing the data generated by the SVX-II chips. Multiple event buffers located on the SAR module are controlled by the SARC. In addition, the SAR module provides the path to direct control codes from the SARC to the Port Card. The data paths to and from the detector are envisioned to be optical; thus electrical-to-optical and optical-to-electrical conversion circuitry will be located on the SAR.

The SAR is a 9U $\times$ 400 mm VME module capable of storing 64 $\times$ 32 kbits of SVX-II readout information which can be accessed over the VMEbus. As a VME slave, the SAR is designed to participate in A24/D32 Block Transfer read cycles from memory and A24/D16 read and write cycles for control. The option of participating in A24/D64 Block Transfer read cycles is currently being investigated. Up to 16 SAR modules can be installed in one VME crate, but the current design reduces this number to eight to reduce event transfer time.

One SAR is associated with one Port Card, connected by a 150 ft long bundle of 12 fibers. The three main functions of the SAR are: 1) to generate serial optical commands to the Port Card for control of the SVX-II chips, 2) to store data generated by the SVX-II chips in dual ported memories accessible from the VMEbus and 3) to route data generated by the SVX-II chips to a Trigger Processor Module (if implemented for DØ).

A 53.104 MHz differential ECL clock signal is received from the Silicon Acquisition and Readout Controller (SARC) Module on the custom VME J3 backplane along with a differential ECL signal which is synchronous with the proton/anti-proton beam crossing. Both signals are routed to the Port Card Equivalents serviced by the SAR. Commands from the SARC are recognized on the 5-bit command bus found on the J3 backplane, and translated to 7-bit serial commands for transfer to the Port Card. Included in the 7-bit Port Card command is: a Framing Bit (used by the Port Card to detect synchronization errors), a Crossing bit (used by the Port Card to generate clock pulses during acquisition), a 4-bit command word, and a parity bit. For each HDI serviced by the SAR, there are up to 12 memory buffers which can store events while Trigger Level-1.5 decisions are being made or waiting for transfer to the Trigger Level-2 system. (The maximum number of available memory buffers is based on a maximum of ten SVX-II chips per HDI.) In this scheme, it is possible to accept Level-1 triggers while Level-1.5 triggers are pending. Buffer management is the job of the SARC, using two buses on the J3 backplane.

The SAR contains an interface circuit to the VME Subsystem Bus (VSB). This local bus, independent of the VMEbus, will allow a local processor to read event data for diagnostic purposes. Obtaining the event data through the VSB for the generation of channel-by-channel histograms will not affect event transfer time.

VME Buffer/Driver

The VME Buffer/Driver (VBD) is a holdover from the current Data Acquisition System, used to read out data from the DØ Central Tracking System. Its use is assumed for the Silicon Vertex Readout System. Under control of the SARC, the VBD reads an event from the SAR modules in a VME crate into one of two internal memory buffers, then independent of action within the VME crate, moves the data to the Trigger Level-2 system.

The VBD operates by reading data from VME addresses stored in a list in the VBD into one of two sections in a dual ported memory. Under control of the data acquisition system, data from specific events are requested from the VBD's. This data is read from the dual port memory onto a 32-bit twisted pair cable for transport to the Trigger Level-2 system.

For use in the SAR crate, the VBD will be programmed to operate in the Central Tracking mode. In response to a signal from the SARC on the J3 backplane, it will read the Trigger Acquisition Synchronization Number and some additional header information stored in the SARC and read the crate number from the Crate ID module. Then for each SAR in the crate, the following sequence is repeated: ask the SAR how many bytes of data are to be read out, then read out that amount of data using VME Longword Block Transfer (A24/D32) cycles. After reading the data from the last SAR in the crate, the VBD informs the SARC that it is ready to read out another event. The use of the dual port memory permits the VBD to read data from the crate while data from a previous event is being transferred out on the data cable.

Trigger Processing Module

This VME based module acts as a local extension of the Trigger Level-1.5 decision making process. As a SAR module receives data from the Port Card, the same data is routed to the Trigger Processing Module via connectors on the front panel. The format of this data is undetermined at this time. The DØ version of the Trigger Processing Module is only conceptual at this time.

Port Card

The Port Card [5] translates the control codes received from the SAR module (originating in the SARC) into control line transitions that the SVX-II chips can respond to. In addition, the Port Card will redirect serial information from the Download System to the SVX-II chips for the purpose of chip setup. Electrical-to-optical and optical-to-electrical conversion circuitry will be located on the Port Card to provide the communication path to and from the SAR module. The various analog monitoring signals will be collated on the Port Card for connection with the 1553 System.

Port Cards are 9U $\times$ 280 mm printed circuit boards mounted in eight crates located in the platform area below the detector. Each Port Card contains two Port Card Equivalent sections. Each Port Card Equivalent is connected to four HDI's by one metallic data path.

A 53.104 MHz clock signal and serial control commands are sent to the Port Card from the SAR across the Low-Speed Optical Link. Optical-to-electrical circuitry on the Port Card regenerates the clock for use on the Port Card and decodes the serial bit stream to operate and control the SVX-II chips. All four SVX-II modes of operation are controlled via the Low-Speed Link. However, initialization of the SVX-II chips requires additional operation of the Download System. Voltage, current, and other analog system information is sent to the Monitoring System.

In response to the command codes received on the low-speed link, a Complex Programmable Logic Device (CPLD) on the Port Card Equivalent generates appropriate clock, control, and data bus patterns into the metallic data path to operate the SVX-II chips on

HDI 0	HDI 1	HDI 2	HDI 3
BUS[7..0]	BUS[7..0]	BUS[7..0]	BUS[7..0]
CLK	CLK	CLK	CLK
CLKB	CLKB	CLKB	CLKB
CHANGE MODE	CHANGE MODE	CHANGE MODE	CHANGE MODE
MODE[1..0]	MODE[1..0]	MODE[1..0]	MODE[1..0]
TOP NEIGHBOR	TOP NEIGHBOR	TOP NEIGHBOR	TOP NEIGHBOR
BOTTOM NEBR.	BOTTOM NEBR.	BOTTOM NEBR.	BOTTOM NEBR.
CALIBRATE	CALIBRATE	CALIBRATE	CALIBRATE

Table 5.2: Conductors in metallic data path between one Port Card Equivalent and Matrix Card.

the HDI's. If the operation is Acquisition or Digitization, then no response from the SVX-II chips is expected. If the operation is Initialization, then the Port Card expects to see previous serial information shifted out of the HDI's as new serial information is shifted in. If the operation is Readout, then the Port Card Equivalent expects to see Chip ID and Status words from the first SVX-II chip in the chain (on a given HDI) followed by the address and data pairs for each channel within that chip participating in the readout. The Port Card Equivalent continues to receive data from the HDI until the last chip in the chain indicates that it has finished reading out (indicated by the assertion of its Top Neighbor output).

Metallic Data Path

The metallic data path provides a connection between one Port Card Equivalent and the Matrix card connected to four HDI pigtails. The current number of conductors in this data path is 80, as described in Table 5.2.

BUS[7..0] is the 8-bit bidirectional data bus. CLK and CLKB are the differential clock signals. MODE[1..0] is the 2-bit mode control bus, which is qualified by transitions of the CHANGE MODE signal. TOP and BOTTOM NEIGHBOR signals are used to: transfer serial data to and from the HDI, control the readout of the SVX-II chips, and to indicate the end of the readout cycle. CALIBRATE is a logical signal which controls the operation of the internal SVX-II Test Pulse circuitry.

The remaining 16 conductors carry analog bias and control voltages. In addition to the 80 conductors, the metallic data path will carry the operating voltages required by the circuitry on the HDI's.

VME Crate/Custom Backplane

Standard VMEbus protocol will be used for intra-crate communication. The VME J1 and J2 backplanes are implemented on a single monolithic backplane which has been modified for custom location of the power buses. To distribute the various clock and control signals required by the SAR's of the SARC, a custom 3U high backplane extension to the 6U high VME backplane has been designed [6]. Two unique differential ECL signals are routed to

each of the 16 SAR slots as impedance specified transmission lines. Control lines are bused across the backplane, and are common to all SAR slots. Lines for communication between the SARC and the VBD are included. The backplane also contains a power bus for accepting the non-VME standard -5.2 V required for ECL logic operation.

Low-Speed Optical Link

The function of the Low-Speed Optical Link [7] is to transport a clock signal and command instructions from the SAR to the Port Card. It consists of two, 150 ft, 62.5/125 μm multi-mode graded-index fiber optic cables and associated driving and receiving circuitry. One of the fibers will carry a 53.104 MHz clock signal. The other fiber will carry a 53.104 Mbit/s Non-Return to Zero (NRZ) serial data stream. The transmitting circuitry located on the SAR consists of two LEDs and associated current drivers. The receiving circuitry located on the Port Card uses PIN photodiodes and transimpedance amplifiers to recover the signals.

High-Speed Optical Link

Each High-Speed Optical Link [8] connects one Port Card Equivalent to one half of one SAR. It consists of one, 150 ft 62.5/125 μm multi-mode graded-index fiber optic cable and associated driving and receiving circuitry. Commercially available laser drivers and diodes are used due to the high (approximately 1 Gbit/s) rates of data transfer. On the Port Card, 16-bits of data from two HDI's are latched at 53.104 MWords/s into a parallel to high-speed serial converter manufactured by Hewlett Packard. The converter adds bits for error detection and correction and sends the encoded serial bit stream to a Finisar Laser module. The optical serial bit stream is received by a Finisar PIN Diode module on the SAR and converted to electrical. A decoder, also manufactured by Hewlett Packard, decodes the serial data to 16-bit parallel and reconstructs the clock.

A total of eight optical fibers connect the Port Card and the SAR. The eight fibers are contained in a jacketed bundle of 12 fibers sold by AT&T under the Accuribbon name. The connection to the SAR module is through a optical backplane connector also sold by AT&T under the MAC-II name.

Download System

The function of the Download System is to provide the serial bit stream required to set up the SVX-II chips located on the HDI. Currently, two systems are being considered. One is based on the 1553 system currently being used by the DØ experiment. One of the parallel output signals is routed to a Port Card Equivalent as a serial bit stream. This bit stream is routed to the four HDI's via the Metallic Data Path. Serial data generated by the SVX-II chips is routed back to the 1553 system for download verification. The second option being considered for the download system is a VME based system. In such a system, the Port Card crate in the platform will contain a VME backplane. The Port Card would exist as a VME slave module, and each data line entering the Port Card would become a serial bit stream for SVX-II downloading. One of the reasons multiple download systems are being considered is that the 1553-controller chips required for system operation are no longer being produced.

While DØ owns a number 1553-based rack monitors, the number required to control the Silicon Vertex System leaves few spares.

Monitoring System

The 1553 system currently in use in the DØ experiment consists of a VME based controller card communicating across a serial data bus to some number of remote terminals. Each remote terminal is capable of transmitting and receiving digital data. The 1553 system contains a Digital-to-Analog Converter circuit which is used to set the Test Pulse Reference Voltage. In addition, each remote terminal is capable of reading analog voltage levels. The analog inputs to the remote terminal are used to monitor slowly changing voltage levels such as the output of temperature sensors, the voltage levels of the power supplied to the HDI and the current drawn by the Port Card, and local environmental monitoring. It is envisioned that the analog read back capabilities of the 1553 system will be used for the monitoring system. The number of 1553-based rack monitors required just to perform the job of analog monitoring is small.

5.1.2 System Operation

In an attempt to keep things understandable, the operation of the entire system as required to put the SVX-II chips through each of their four operation cycles will be described. The required control of the SVX-II chip will be described first, then control and data flow beginning at the Trigger Manager or DØ Clock System, as appropriate, to the SVX-II and back to the SAR, if necessary, will be described. Note that the operation of the system as described here assumes 132 ns inter-bunch spacing. If the accelerator operates at bunch spacing greater than this, then minor modifications to the programmable logic contained in the SARC will be required. Timing diagrams for each of the four SVX-II operation cycles are shown in Fig. 5.3.

Initialization

During the Initialization cycle, parameters for SVX-II chip operation are loaded into the chip serially through the Bottom Neighbor input pin. A 50% duty cycle clock, phased with the serial data, is used to shift the data into the SVX-II chip. SVX-II chips are daisy-chained together, so as serial information is shifted into one SVX-II, data previously in the chip is shifted into the next SVX-II. The last SVX-II chip in the chain shifts its data back to the Port Card.

The SARC in each crate contains a VME addressable register. The Data Acquisition System writes to this register to indicate that the SVX-II chips are to be loaded. The SARC generates commands to the SAR's in the crate indicating that downloading is imminent, which in turn send download commands to their associated Port Cards. The Port Card, recognizing that a download cycle is beginning, changes the operating mode of the SVX-II chips to accept serial data and routes one of the parallel data lines from the Download System (either from the 1553 system or the VME system) to the Bottom Neighbor input of the first SVX-II. In addition, a clock signal, phased with the serial data, is generated and sent to the

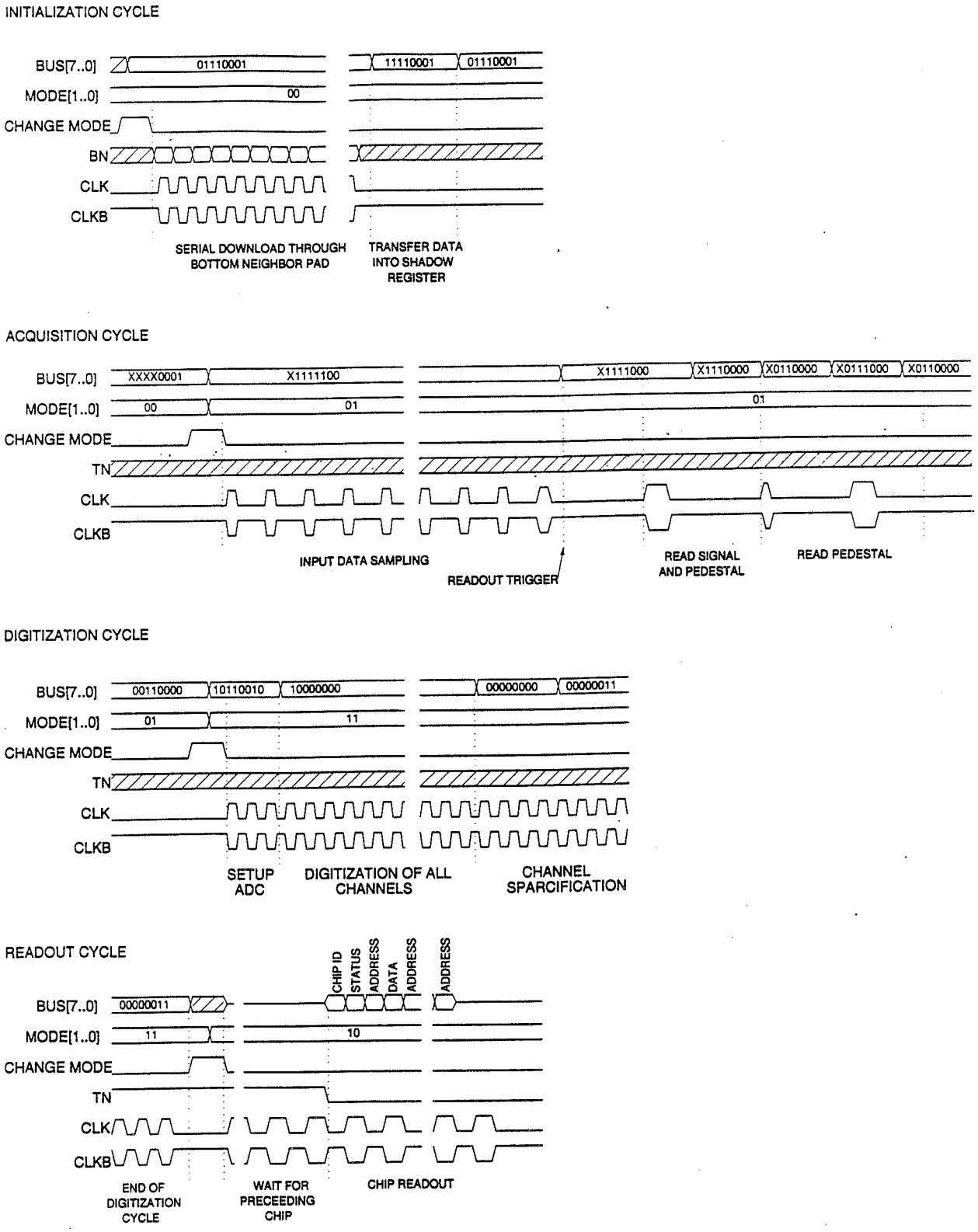

Figure 5.3: SVX-II Timing Diagrams

first SVX-II. The Download System generates data until the SVX-II chips on the HDI are fully loaded. Note that the software controlling the Download System will need to count the number of cycles generated, as the SVX-II chips do not indicate when they are loaded. When the download process is complete, the Data Acquisition System informs the SARC's, which remove the download command from the SAR control bus. The SAR's inform their Port Cards, which manipulate the signals in the 8-bit data bus to force the SVX-II chips to latch the contents of the shift register, completing the Initialization cycle.

Acquisition

During the Acquisition cycle, charge being deposited on the Silicon Detector strips is being stored on the 32-stage capacitor pipeline. Just prior to charge storage, a given pipeline capacitor needs to have any previous charge removed. During the Acquisition cycle, the SVX-II chips require an input clock pulse to perform this discharging. During the interval between clock pulses (which are phased with proton/anti-proton collisions) the pipeline capacitor is available to store charge. The width of the clock pulse during acquisition is critical: it needs to be long enough to discharge the pipeline capacitor, but also needs to be short enough to allow the capacitor to fully charge before the next clock pulse. Preliminary indications show the clock pulse to be between 25 and 30 ns. The clock pulse during the Acquisition cycle also increments the pointer to the next capacitor in the pipeline.

The DØ Clock System Sequencer Module will be programmed to generate a pulse every 132 ns. The SARC receives and distributes these pulses to the SAR's in the crate. The SAR's use these pulses to frame the 7-bit serial packets sent to the Port Card over the Low-Speed Link. One of the seven bits is the Crossing bit. Under normal operating conditions, the default command on the command bus from the SARC to the SAR's is the acquisition command. The SAR's transmit the acquisition command and the asserted Crossing bit to the Port Cards, which manipulate the Mode and data bus lines to put the SVX-II chips in Acquisition mode. Recognizing the acquisition command and the asserted Crossing bit, the Port Card generates the 25 to 30 ns pulse required to discharge the pipeline capacitor. The arrival time of this clock pulse with respect to actual beam crossing will need to be phased for optimal operation of the SVX-II in acquisition mode. The fine adjustment of the phasing of the 7-bit packet, including the Crossing bit, is done on the SAR.

When the Trigger Manager determines that a Trigger Level-1 event (based on Calorimeter, Muon detector, or Scintillating Fiber inputs) has occurred, an indication is sent to all of the SARC's. The SARC's change the instruction on the command bus to halt acquisition. The SAR's interpret this command and stop sending the Crossing bit. The Port Card, sensing the missing Crossing bit, stops sending clock pulses to the SVX-II chips. When the SVX-II chip is not being clocked in Acquisition mode, the capacitor pipeline is stopped. At this point, one of the capacitors in the pipeline (based on the value of the SVX-II pipeline depth register, downloaded in the Initialization cycle) is selected for readout. The propagation delay from the generation of the Trigger Level-1 accept by the Trigger Manager to the cessation of clock signals at the SVX-II chips is expected to be constant and the same for all SVX-II chips. Because of this, the SAR continues to generate the acquisition command with the Crossing bit asserted even through the expected large gaps in the beam.

Before the SVX-II chip can begin the Digitization cycle, the charge stored on the pipeline

capacitor needs to be corrected for the effects of charge injection. Currently, the Port Card manipulates bits on the 8-bit data bus and sends clock pulses at the appropriate times to control this pipeline readout. It is expected that in a final version of the SVX-II chip, this pipeline readout operation will be performed internally, requiring minimal control from the Port Card.

Digitization

During the Digitization cycle, the voltage representing the charge read from each capacitor pipeline is digitized to 8-bit (maximum size; minimum size is six bits) words. Once the SVX-II chips are placed in Digitization mode a common voltage ramp is applied to all channels in a chip. Coincident with the voltage ramp, a Gray code counter increments from its initial value of 0 to the value specified in the Counter register. The counter increments on both edges of the 50% duty cycle clock input signal. For each channel, voltage due to charge stored in the capacitor pipeline and the ramp voltage are applied to a voltage comparator. As the ramp voltage exceeds the voltage due to charge, the comparator fires, latching the current value of the Gray code counter (an indication of the voltage amplitude) into an 8-bit register. A digital comparator for each channel compares the register value with the digital threshold value (common to all channels in a chip, loaded during the Initialization cycle). Those channels which exceed threshold (and the neighbors of such channels if the SVX-II is set in nearest neighbor mode) are eligible for readout. After digitization is complete (the number of clock pulses times two is greater than the Gray counter maximum value loaded in the Counter register), the FIFO structure which controls which channels are going to participate in the readout must be allowed a period of time to form the readout sequence.

The SARC recognizes the Trigger Level-1 accept from the Trigger Manager, and changes the command bus from acquisition to digitization. The SAR's respond by turning off the Crossing bit and sending the digitize command to the Port Card. The Port Card, however, must wait until the pipeline is read out until setting the SVX-II chips into Digitize mode. A counter on the Port Card determines the waiting time. The Port Card manipulates the Mode and data bus bits to put the SVX-II chips into Digitize mode. The actual digitization occurs when the Port Card instructs the SVX-II chips to release the voltage ramp and sends a 53.104 MHz clock pulse train. Assuming that all eight bits were used for digitization, the Port Card will send 128 clock pulses (both clock edges are used for digitization) taking 2.41 μs. Prior to the generation of the instruction to begin reading the SVX-II, the Port Card must allow the readout FIFO in the chip time to collapse so that only the channels which have been "tagged" (by values in excess of threshold or forced by nearest neighbor hits) are available for readout. Currently, this time is about 1.3 μs. Adding to this time are the digitization time (2.41 μs) and the waiting time required between Acquisition and Digitization (about 0.56 μs) so that the total time after the Trigger Level-1 indication arrives at the SVX-II until readout can begin is about 4.27 μs.

Readout

Once in Readout mode, the SVX-II chip responds to the 50% duty cycle clock by generating an 8-bit word on each (low-to-high and high-to-low) transition of the clock. The first thing

any SVX-II chip generates is an 7-bit Chip ID number (loaded during the initialization cycle) The number of bits in the Chip ID register is large enough so that each SVX-II chip connected to one Port Card Equivalent can be assigned a unique value. Immediately following the Chip ID, the SVX-II chip generates the 8-bit Chip Status word. As a minimum, this Chip ID/Status pair is generated even if no channels in the chip are tagged for readout. Then, for each channel in the chip which is to be read out, the 7-bit Channel Number is followed by the 8-bit data value (regardless of the number of bits digitized). Address/Data pairs continue to be generated until all required channels have been read out. The assertion of the Bottom Neighbor pin (connected to the Top Neighbor pin on the adjacent chip) forces the next chip in the chain to read out.

The Port Card requires no input from the SAR or the SARC to force the SVX-II chips into the Readout cycle. The Port Card simply waits the required time (1.3 μs) after the Digitization cycle is completed and then manipulates the Mode lines to put all the SVX-II chips into readout mode. By generating a 26.552 MHz clock signal, information starts to flow back from the SVX-II chips (after twice the propagation delay in the metallic data path). The Port Card continues to generate the clock until the last SVX-II chip on the HDI asserts its Bottom Neighbor output, which is monitored by the Port Card. The data from the HDI's are routed in parallel to high-speed serial converters, then converted to optical for the trip to the SAR modules 150 ft away. Recall that four HDI's are connected to one Port Card Equivalent by the Metallic Data Path. When one Port Card Equivalent finds that all SVX-II chips on the four HDI's have finished reading out it stops sending the clock.

The high-speed serial optical data stream is first converted to electrical, then to parallel on the SAR. The output of each high speed link is the 8-bit data buses from two HDI's. The SAR interleaves the 8-bit data words to a 32-bit wide word which moves at a more manageable rate. The Gray coded data from the SVX-II chips is converted to binary on the fly by circuitry on the SAR. The data for each HDI is stored into one section of a dual ported memory for possible transfer to the VBD. Each section of the dual port memory is capable of holding the data from one event for one HDI. The control of which section of memory is used for a given event is the responsibility of the SARC. As data is routed to the dual port, a copy of the same data (in a different format) is routed to a multiplexing circuit which drives the front panel connector. The front panel connector is provided for sending SVX-II data to a Level-1.5 Trigger Processing Module. Note that due to the expected propagation delay in the Metallic Data Path, some number of words from the last SVX-II on an HDI will be generated (some before the Bottom Neighbor signal is recognized, and more before the last SVX-II stops seeing clock pulses). To allow the SAR to recognize the end of valid data, the two most significant bits on the bus between the SVX-II chips and the cable interface circuit on the HDI will be pulled up. The structure of the data generated by the SVX-II and the assignment of Chip ID's will guarantee that these two bits are not set for the leading word of either Chip ID/Status or Address/Data pairs. The SAR recognizes this 2-bit pattern as the End of Readout indication and ignores any extra data. Once the SAR has received an End of Readout indication from both Port Card Equivalents, it releases the End of Readout open collector signal on the J3 backplane. When all SAR's in the crate have released this line and a Trigger Level-1.5 decision is true, the SARC instructs the VBD to begin its function of reading the event. The VBD reads the data from all SAR's in the crate, from the section of the dual ported memory dictated by the SARC. When all the data has been read the VBD

informs the SARC that it is finished. Under control of the Data Acquisition System, VBD's in all crates are instructed to transfer the data to the Trigger Level-2 system.

5.2 DØ Tracking Triggers

Triggers based on tracks found in the scintillating fiber detector and silicon strip detector barrels are required to increase the efficiency of the DØ experiment for

- finding decays from top
- studying final states containing b quarks and CP violation
- discovering new physics (*e.g.* Higgs, supersymmetry) associated with b's in the final state.

A trigger based on tracks in the scintillating fibers has been devised to select particles with momenta above $\sim 1.5\,\mathrm{GeV}/c$. The scintillating fiber trigger can also provide a road in the silicon detector to search for tracks originating from a secondary decay (displaced vertex trigger) at Level 1.5.

The time for this is quite limited: of order $10\,\mu$s. It must also be efficient and not introduce significant dead time.

5.2.1 Scintillating Fiber Trigger

The fiber barrels are divided into 80 sectors in ϕ for the scintillating fiber trigger (SFT) [9]. The mechanical design of such a sector is shown in Fig. 5.4. The trigger is formed using field-programmable gate arrays (FPGA's) which compare fiber hits in the four axial fiber superlayers (eight layers of axial doublets) with predetermined patterns representing valid tracks. This choice of 80 segments is a "magic number" in a very real sense, representing an optimization of the spacing of the fibers in the four barrel superlayers and the interconnection of the fibers from these layers to the VLPC cassettes to form appropriate ϕ trigger towers. Entering into the optimization are the number of different kinds of fiber ribbons required for the detector barrels, the number of fibers per connector when the fibers from the different layers are sorted into towers, the capacity of the FPGA's which form the trigger and the number of channels which must be routed from neighboring towers to eliminate cracks.

The trigger assumes a loose beam constraint and searches in $r-\phi$ projection. Centroids are found for valid track segments in each superlayer and binned into 16 cells per sector for input to the FPGA. Additional cells from neighboring sectors are included to allow for curvature of tracks at the lowest momentum of interest. The entering ϕ angle and p_t bin are used in the muon and other systems at Level 1. The pattern from a valid track could also be transferred at full accuracy of the digital information from the trigger by using the encoded location of the track segments in the outer and inner layers. The characteristics of a valid track from anywhere in the fiber tracker could be held in a 16 bit track code.

The trigger system will produce outputs for multiple valid tracks within each sector. The resulting track data will need to be pipelined.

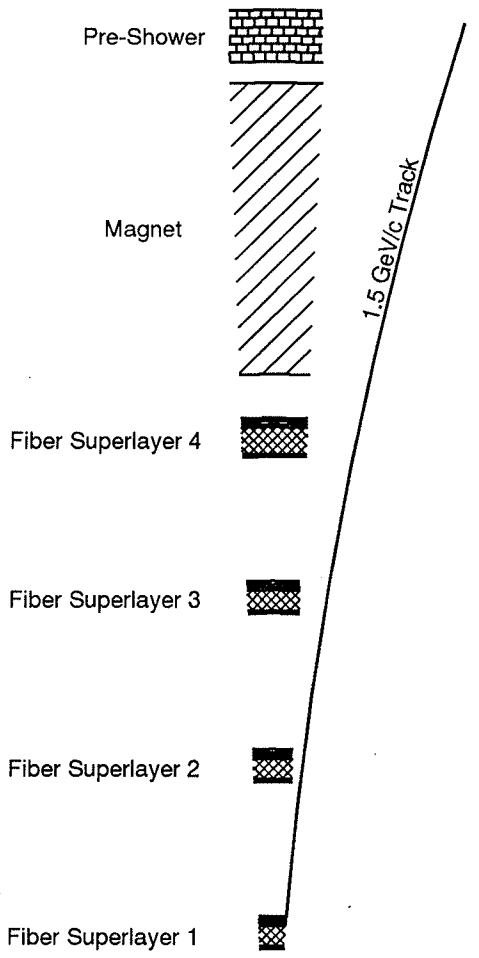

Figure 5.4: Fiber Tracker ϕ Sector (shown in $r - \phi$ cross-section). The fiber tracker is divided into 80 such ϕ sectors to form triggers for tracks down to $\sim 1.5\,\mathrm{GeV}/c$ p_t. Each fiber superlayer is supported by a composite cylinder (shown cross-hatched). Two pairs of axial scintillating fiber ribbons below and above the support cylinder are used for the trigger in each superlayer. Signals from two neighboring sectors are included as required in the trigger logic. A $1.5\,\mathrm{GeV}/c$ p_t track originating at the beam line is shown for reference. The inner two layers of the pre-shower scintillator may also be used in the trigger.

The rate from this trigger will be too high for use by itself at Level 1. It must be combined with other information such as muon stubs in the A layer or electron candidates in the preshower detectors. To get a significant b sample, we must still allow for a Level 1 accept rate of at least 10 KHz, which represents a major increase over the current limit.

5.2.2 Output to Silicon Trigger

The track code itself can be used to estimate ϕ_0, p_t and the location of a relatively broad ($\sim$ 2 mm) search road in the silicon tracker for an impact parameter trigger at Level 1.5. Alternatively, more detailed information can be transmitted. This could be in the form of accurate centroid information for an eight-point track fit (four silicon measurements and four scintillating fiber centroids). Or a fit without beam constraint could be made to the fiber information alone during the silicon readout. This would have two advantages: the search road could be narrower ($\sim 500\,\mu$m) since allowance is no longer necessary for the secondary decay radius; and rather accurate values for ϕ_0 and p_t would be available for the fit in the silicon (see below).

5.3 The Level 1.5 Silicon Trigger

We saw above that the Level 1 accept rate must be increased considerably to collect a useful b sample. Conversely, before writing to tape, as much additional information as possible must be used to select events of interest. A key ingredient is the silicon impact parameter trigger at Level 1.5. This decision must be made in a time of order 10 μs or dead time will become unacceptable.

5.3.1 CDF Plans as Baseline

As a point of reference, we describe current CDF plans. CDF proposes to make an impact parameter trigger in a 10 μs interval based on information from the CDF silicon vertex tracker (SVT) and the central tracking chamber (CTC) [10].

Since the CDF impact parameter trigger requires strict tower geometry, the planned SVT is divided azimuthally into 12 distinct towers of four parallel silicon planes. Layers of adjacent towers are staggered in radius to provide for overlap to eliminate dead cracks yet leaving room for readout chips on double-sided detectors. The center of each silicon layer is tangential rather than tilted—no mechanical compensation is planned for Lorentz forces on charge carriers in the detector. The SVT is divided longitudinally into three 32 cm long barrel sections separated by 2 cm gaps for cables, fiber optic lines and cooling water feeds. There are no disks interleaved between the barrel sections although silicon disks are used in the forward region.

CDF proposes to use a pipelined, deadtimeless front-end for SVT (SVX-III). Tracks are digitized in 2.5 μs on average following a Level 1 trigger. The digitizations are fed to hit finders which recognize the typically 3–4 adjacent strips corresponding to a track and calculate the centroid. These hit centroids are then distributed to the event buffer and to associative memory (AM) modules, along with ϕ measurements of tracks found in the

CTC. The AM is a custom VLSI device designed to compare these hits (organized as five planes, four from SVT layers and the fifth from the CTC ϕ measurement) with valid roads stored in memory. All coordinates from a ϕ tower are compared in parallel, producing a stream of addresses of all found roads on completion of the SVT readout. This process is analogous to the operation of the DØ SFT trigger, except that in the SFT, road finding is implemented with FPGA units. There is a tradeoff between the road width and the number of fake tracks as well as the number of hit combinations to consider within a given road. Narrower roads require more AM chips but yield fewer fakes and hit combinations, resulting in reduced processing time per event at Level 1.5. CDF finds that a road width of 250 μm is a reasonable compromise.

Tracks would be found for each road using farms of track-fitting processors. The track fitter (TF) receives the roads from the AM, gets the silicon hits within the road in the four silicon planes from the event buffer and performs a constrained fit to eliminate extra hits and find the parameters (ϕ_0, p_t and impact parameter) of valid tracks. Input to the TF as well are the ϕ_0 and p_t estimates from the CTC, hence there are three constraints in the fit.

The track fitting algorithm is optimized for fast DSP calculation. The equations are reduced to scalar products by expanding about the road center (linearized fit). In general, one would expect that the expansion parameters would be different for different roads in a given tower, depending perhaps on lateral position and track curvature. In fact, with the SVT geometry, the parameters are found to be sufficiently independent of the road that only one set is needed for an entire tower. This speeds the calculation further by avoiding additional memory references. It is estimated that a processor with a 50 ns multiply+add cycle would complete the calculation in 3.5 μs.

The expected accuracy of the resulting impact parameter fit is $\sigma = 35\,\mu$m above 2 Gev/c p_t. The width (σ) of the Tevatron beam is roughly 30 μm. CDF has studied the improvement in signal to background as a function of minimum impact parameter and has found that a cut at 200 μm is optimum. In a simulation using actual SVX data [11], the linearized fit to impact parameter done by the TF farm was nearly identical to the full offline fit.

Since the longitudinal position of the primary interaction vertex is not known or fitted, this technique requires the beam to be accurately aligned parallel to the SVT axis (within 100 μrad).

The overall SVT trigger cycle thus begins with digitization of the silicon signals (requiring 2.5 μs) overlapped with CTC track finding (5 μs). Following silicon digitization, readout, hit finding and track finding proceed in parallel for 3 μs. The input data are presented to the track fitting farm approximately 6 μs after the Level 1 trigger. The operation is completed within 10 μs.

5.3.2 DØ Impact Parameter Trigger

In contrast to the CDF design, the silicon detector geometry proposed for DØ is not segmented into independent towers with parallel silicon planes. Nonetheless, 12 independent sectors and 24 effective towers can be formed, as shown in Fig. 5.5. Note that the two inner silicon planes are shared in two effective towers. When subdivided in this way, the silicon planes are sufficiently parallel to allow use of the linearized fit technique if desired.

In place of the central tracking chamber and associative memory road finders of CDF,

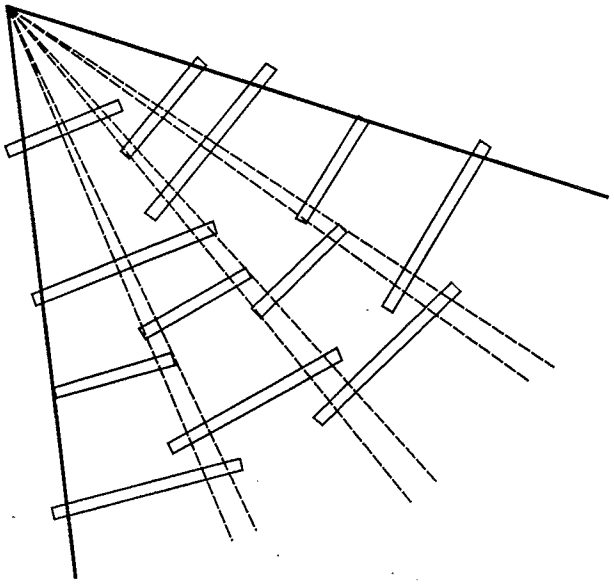

Figure 5.5: Silicon Effective Towers. A 60° sector of a silicon barrel is shown schematically in cross section illustrating how four effective towers can be formed for triggering.

the DØ scintillating fiber trigger is proposed for providing roads and estimates of ϕ_0 and p_t for the silicon tracker Level 1.5 trigger.

Preliminary simulation results using the linearized fit technique using the DØ geometry and centroid information from the fiber tracker give confidence that sufficient accuracy can be achieved [12]. As was the case for CDF, the linearized fitting parameters are found to be sufficiently independent of the road that only one set is needed for an effective tower.

Again, as with CDF, a key requirement is that the beam be accurately aligned with the silicon tracker axis.

DØ Silicon Track Processing

As described earlier in the electronics section 5.1 of this chapter, data from the detectors entering the Level 1.5 trigger will be digitized locally after a Level 1 trigger and sent to the Movable Counting House in serial form for further processing. The Level 1.5 trigger processors, mounted on VME cards, would receive the silicon data from the barrel SAR units. The main features of a potential Level 1.5 trigger card are indicated in the block diagram of Fig. 5.6. Key design elements are use of:

- buffers to smooth out data flow at all stages of processing
- static-RAM based FPGA's so the trigger can be upgraded in place
- an efficient high-speed data switching architecture to assemble tracks from hits based on road information
- fast digital signal processors (DSP's) to fit tracks.

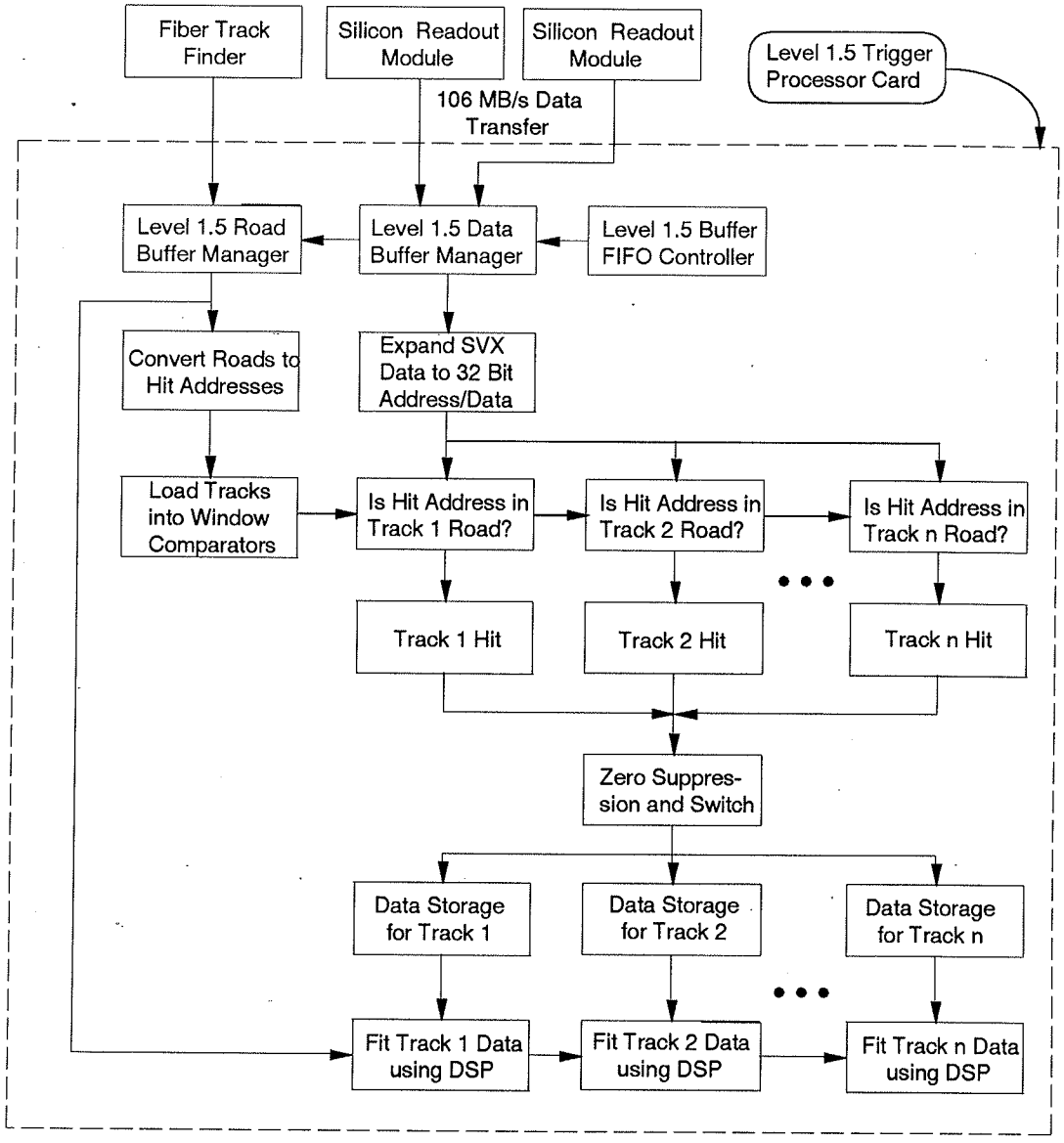

Figure 5.6: Block Diagram of a Potential Level 1.5 Trigger Card

To avoid overloading the various processing and switching elements, each card receives data from an independent ϕ sector (perhaps one fourth of the silicon tracker barrel sections) rather than the full array. This implies that all the SVX output cables from a sector must be arranged to connect to the SAR units feeding the trigger card for that sector.

The Level 1.5 trigger card also receives track data from the corresponding scintillating fiber towers. For towers at the boundary between silicon sectors, information will have to be sent to both adjacent Level 1.5 trigger cards.

After each Level 1 trigger, the scintillating fiber track finder provides information for tracks above the minimum p_t threshold ($\sim 1.5\,\mathrm{GeV}/c$). In this design, digital window comparators are used to find hits corresponding to tracks within the roads. The valid road addresses corresponding to the supplied fiber tracks are loaded from a table in local memory into a parallel array of comparators. As the stream of SVX data flows through these comparators, valid hits are sorted into buffers corresponding to each road using a cross-bar switch (or an equivalent, more efficient architecture).

Coordinate centroids would be found for adjacent hits in the silicon detector planes. These would then be fitted utilizing additional track parameter information from the fiber tracker. Spurious hits within the road would be rejected and track parameters found, resulting in an accurate impact parameter measurement for use in the Level 1.5 trigger.

Much work remains to complete the Level 1.5 tracking trigger design for DØ and verify that it can produce the desired results in the time available. Nonetheless, the proposed design of the DØ silicon tracker appears to be compatible with such a trigger as long as the cabling provides the necessary segmentation and the readout has adequate buffering.

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Chapter 6

High Density Interconnect and Cables

Figure 6.1 is a block diagram showing relationships among the silicon system components discussed in this section. The high density interconnect or *HDI* is a flexible circuit mounted on the silicon detector. It supports the SVX-II readout chips as well as the transceivers and passive components. A ≈20 cm extension of this circuit, the *HDI tail*, carries power and signals outward to a radius beyond the active silicon. By means of an unmateable *Fujipoly connection*, the HDI tails interface through a passive *matrix card* to a *strip cable* ≈1.5 m long. The strip cable carries signals and power to the end of the silicon detector. There a passive *transition card* connects the strip cable to a *coax cable* ≈10 m long. The coax cable terminates at the *port card* located in VME crates on the detector platform. This card is discussed in Section 5.1.1.

The key system design decisions involved in this layout are:

- The HDI is mounted inboard of the detector end in order to minimize dead area. Its integral tail eliminates the mass and avoids the unreliability and crowding associated with connections near the end of the detector. The thin flexible tail also minimizes the required path area to larger radius.
- The port cards are located on the platform to ensure serviceability and to remove their mass from the detector.
- For connection to these port cards, the cable is divided into a low mass stripline for the first ≈1.5 m and a high quality multi-coax for the remaining ≈10 m of the run. They join at the transition card.
- Each cable (stripline or coax) serves four HDI's in order to reduce cable count, and each set of HDI signals is carried in parallel in order to preserve readout speed. The matrix cards join four HDI tails to one stripline.
- Unmateable connections between the HDI tails and the matrix card are provided to minimize the length (≈20 cm) of permanent attachments to the HDI. The matrix and transition cards are soldered to the strip cable.

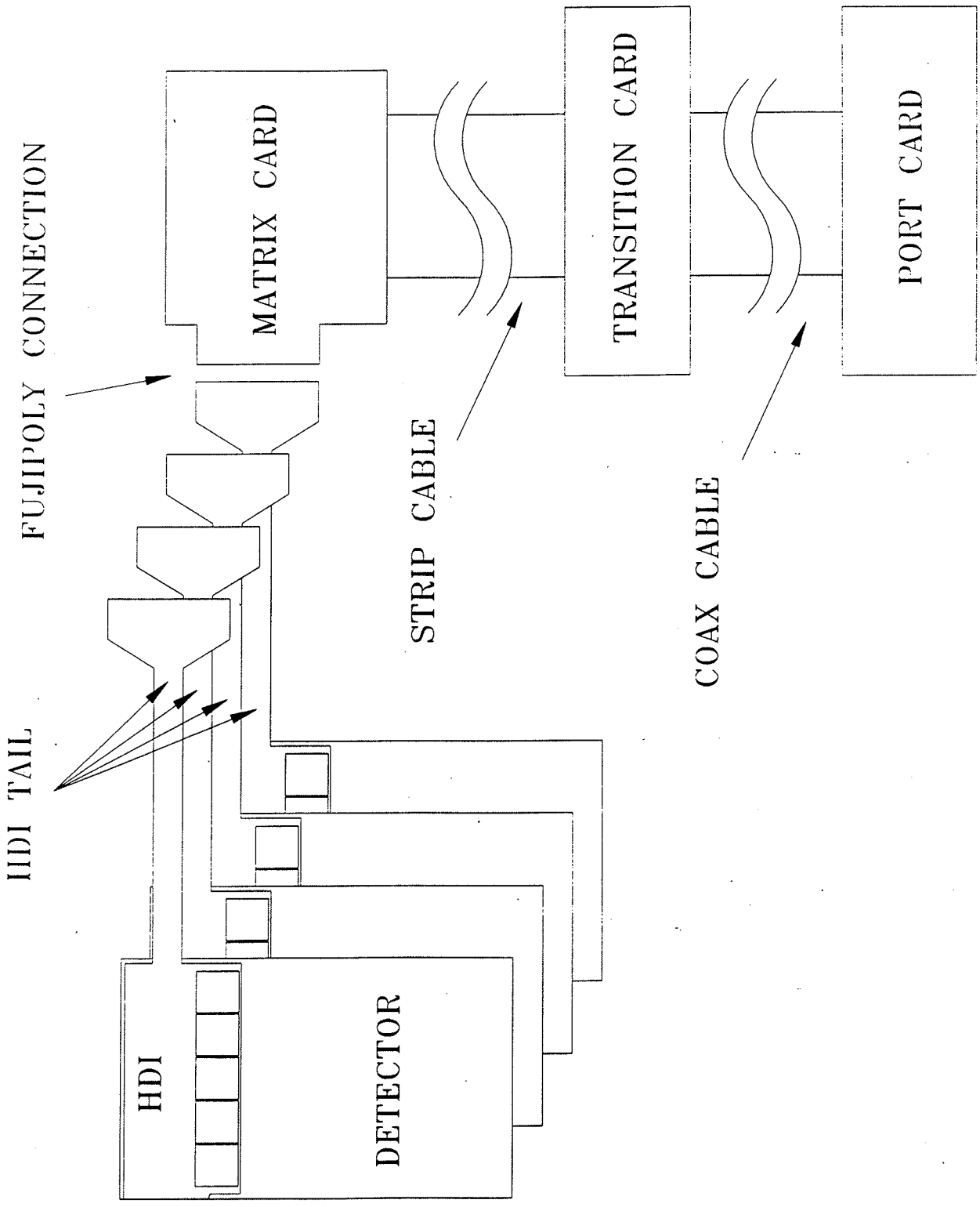

Figure 6.1: Silicon system components.

6.1 High Density Interconnect and Tail

As discussed in Sections 1.4.1 and 4.2, the HDI is located inboard of the detector end to minimize dead area. A schematic view is provided by Fig. 6.2. The HDI consists of a compact circuit on a flexible polyimid substrate. It is glued to a Be plate which in turn is glued to the detector. Pictured is a double-sided detector in which both sides are served by the same HDI, which wraps around the edge as shown. For a single-sided detector, only the top portion of the HDI is provided.

A model HDI layout is shown in Fig. 6.3. Its parts list appears in Table 6.1. Among the key parts to be carried by a double-sided (single-sided) barrel HDI are up to 10 (5) SVX-II readout chips, 2 transceivers, 10 termination resistors, and the various capacitive and resistive components required by the SVX-II chips. The disk HDI's, mounted outboard to reduce mass at small radius, serve only one detector side and support 8 SVX-II chips. From top to bottom, the four HDI layers consist of: components and short traces ($\perp$ to the long HDI axis); long traces; ground; and power. For improved heat transfer and reduced mass, the trace layers under the SVX-II chips are cut away. The HDI tail preserves this structure except that no short trace layer is required.

The key HDI design decisions are:

- The substrate is a thin (typically 1 mil/layer) flexible polyimid in order to reduce mass and wrap around the detector edge. A conventional thick film circuit would be much too massive.
- The characteristic trace pitch (8 mil) is set by the SVX-II channel spacing, and the via diameter (15 mil) on the model HDI is set by current vendor capability.
- To further reduce mass, $\frac{1}{4}$ oz Cu conductor layers are specified together with minimum dielectric thickness. A model circuit with these specifications has been ordered from one vendor.
- To reduce mass at small radius, large power supply bypass capacitors are removed to the matrix card.
- The circuit layout is driven by locating the bypass capacitors required for each SVX-II chip as close to the SVX-II as possible.
- Differential clock signals will be received directly by the SVX-II chips in order to optimize waveform symmetry and minimize mass. Bidirectional signals are transceived by TI 053 chips in die form to minimize mass.

An early "HDI1", constructed for use with the SVX-I chip, shared many of the same design parameters including a similar substrate, trace pitch, and via diameter. It was tested extensively. Figure 6.4 compares the noise observed in a test Si detector (left) as read out by a test board; (center) same readout after the HDI1 was glued to the detector; (right) as read out by the HDI1. The pulse heights from an IR laser signal were the same for all three conditions, and, as seen in the figure, the noise levels were also equivalent. This confirms that gluing the HDI1 to the detector and reading out the detector with a low-mass HDI1 do not increase the system noise.

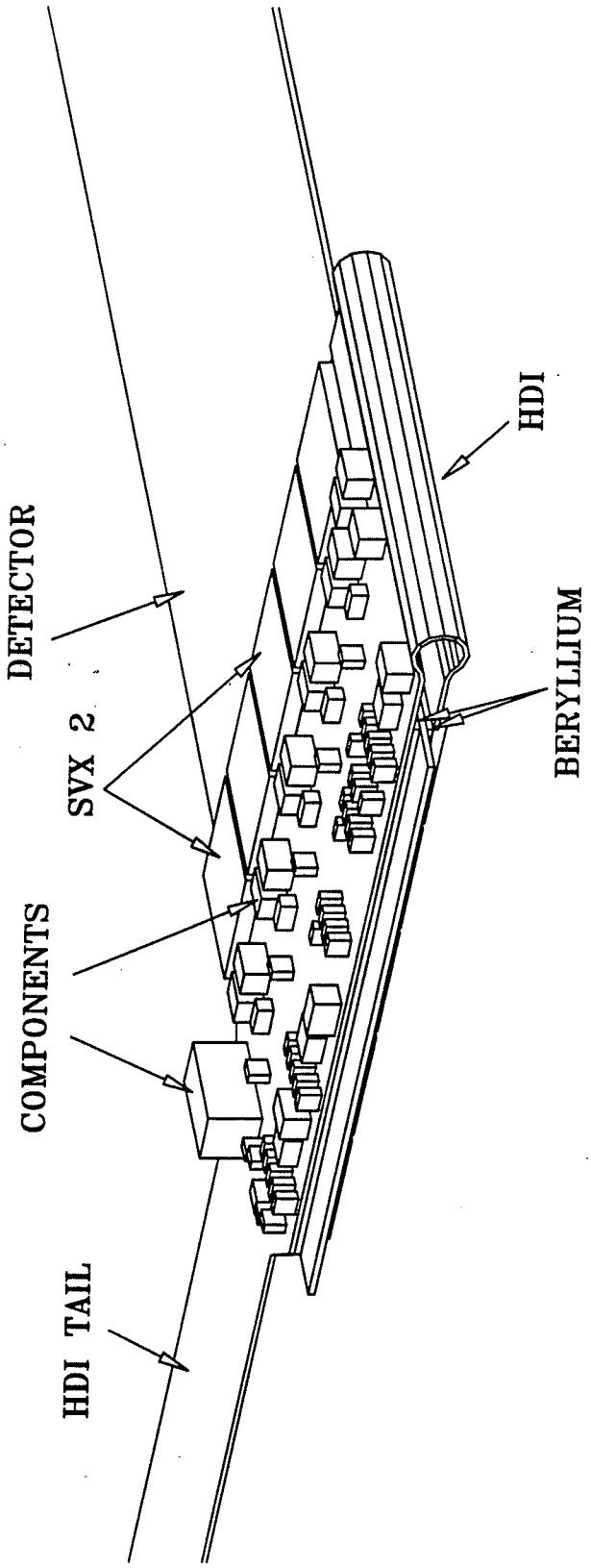

Figure 6.2: The high density interconnect (HDI).

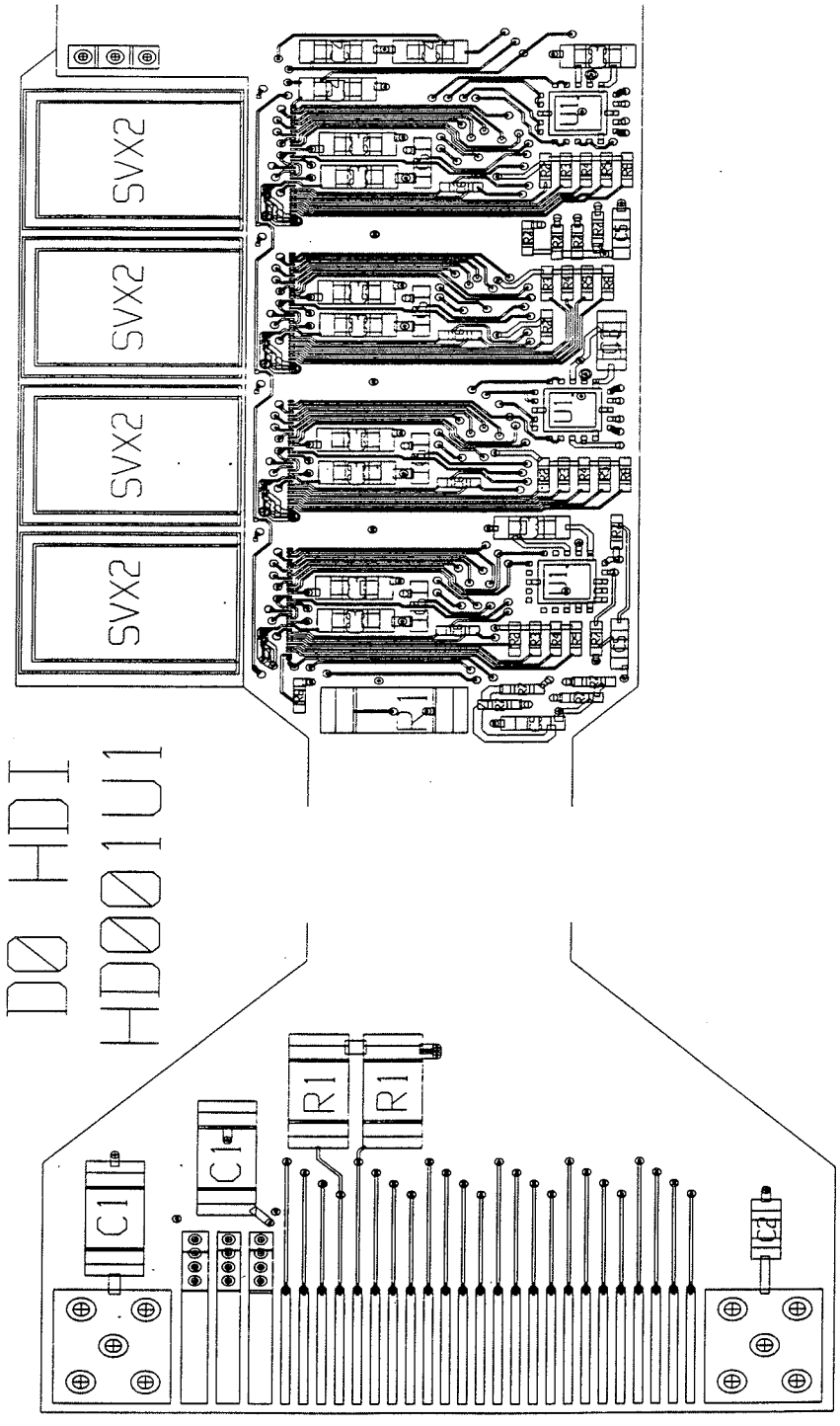

Figure 6.3: A model HDI layout.

Parts List for D0 Model HDI

Designation	# per HDI	value	size	type
C1	2	0.56uF 16V	1812	X7R ceramic (nominal)
		10 uF 16V	2010	Tantalum (option)
C2	1	0.15 uF 16V	0805	X7R ceramic
C3	19	0.15 uF 16V	0805	X7R ceramic (nominal)
		0.027 uF 16V	0603	X7R ceramic (option)
C4	4-6	0.015 uF 100V	0805	X7R ceramic (4 nominal for detector bias bypassing)
C5	11	0.027 uF 16V	0603	X7R ceramic
C6	8	0.01 uF 16V	0402	X7R ceramic
R1	0-3	50 ohm 1/2 W	2010	5% (50 ohm nominal match to cable impedance)
R2	8	18k ohm 63 mW	0402	5%
R3	8	370k ohm 63 mW	0402	5%
R4	8	1k ohm 63 mW	0402	5%
R5	8	68k ohm 63 mW	0402	5%
R6	8	27k ohm 63 mW	0402	5%
R7	8-10	100 ohm 63 mW	0402	5% (100 ohm nominal match to cable for differential signals)
SVX2	8		die	readout ASIC
U1	3	TI SN75ALS053	die	transceiver

Table 6.1: Parts list for model HDI layout.

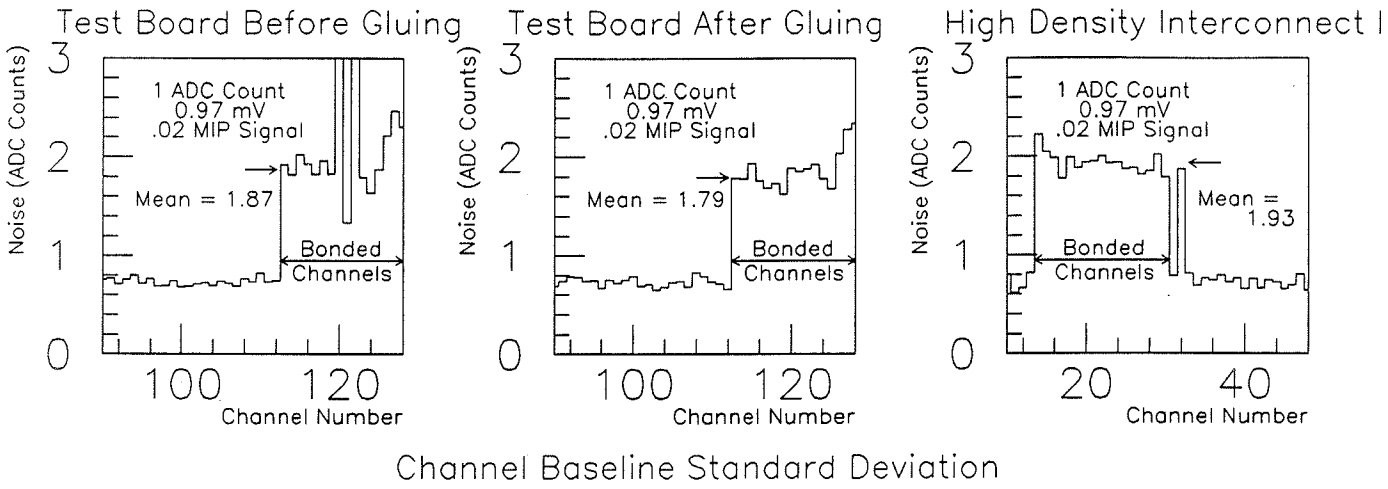

Figure 6.4: Si detector noise observations.

6.2 Fujipoly Connection

The connection between the HDI tails and the matrix card is made using Fujipoly technology. The principle is shown in Fig. 6.5. The silicone rubber layer contains a pattern of short Au plated conductors oriented perpendicular to the plane. These make contact with Au plated conductors on the HDI and the matrix card.

We have adopted this technology because of its low mass and reliability. Figure 6.6 illustrates the use of a single low-mass clip to make Fujipoly connections between four HDI tails and the matrix card. We have tested this connection method using several models under a variety of conditions, including multiple layers and 2 Mrad radiation exposures, and we have found it to be reliable.

6.3 Matrix Card

The matrix card is a 12-layer circuit illustrated in Fig. 6.7. In addition to connecting the HDI tails to the strip cable, the matrix card accomplishes the right-angle bend in cable flow direction needed as that direction changes to axial. On the HDI tail side, the matrix card separates into four 2-layer parts to integrate with the four-stacked Fujipoly connector. On the strip cable side, the matrix card is soldered to the strip cable.

6.4 Strip cable

The strip cable is a logical extension of the multiple coax cable leading to the port card. It runs axially along the outside of the silicon detector from the matrix cards to the end of the silicon. We have incorporated it in order to reduce the cable mass in the detector region. The strip cable consists of an etched Cu trace layer (80 conductors at 10 mil pitch) on a

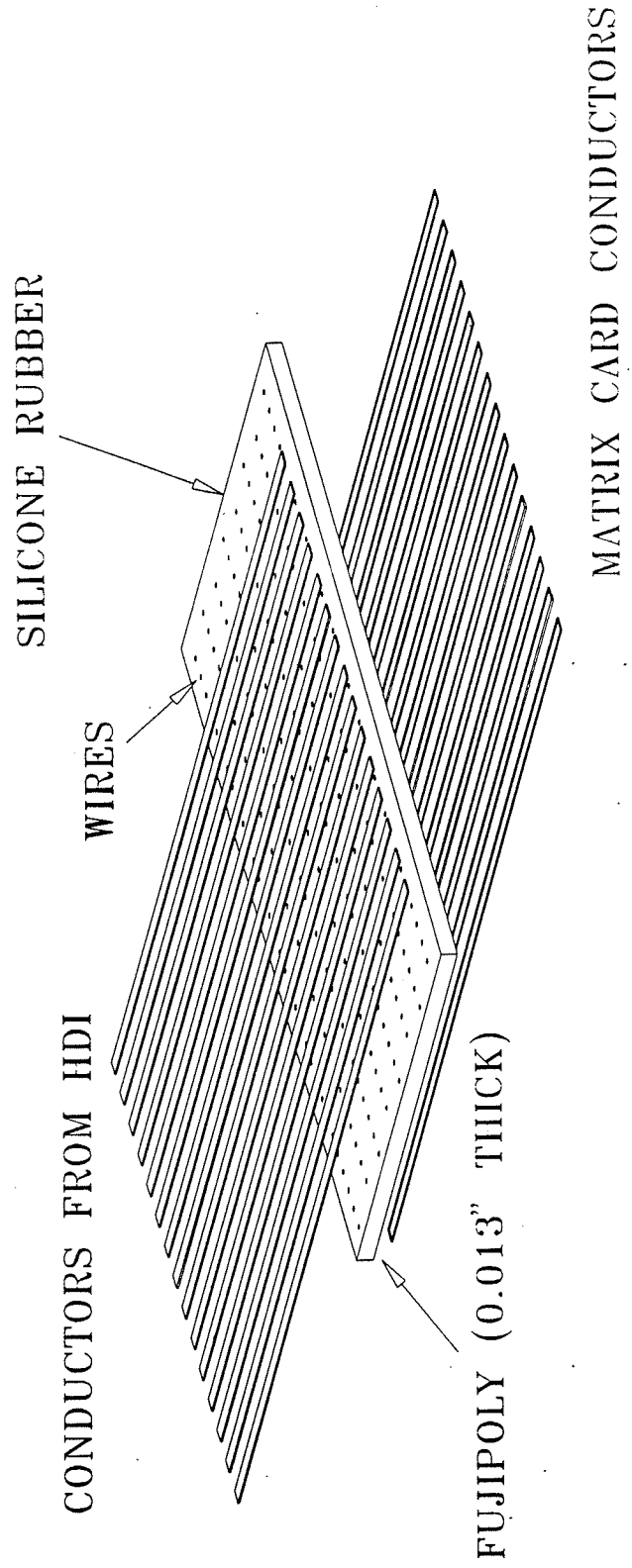

Figure 6.5: Fujipoly technology connection between HDI tails and matrix card.

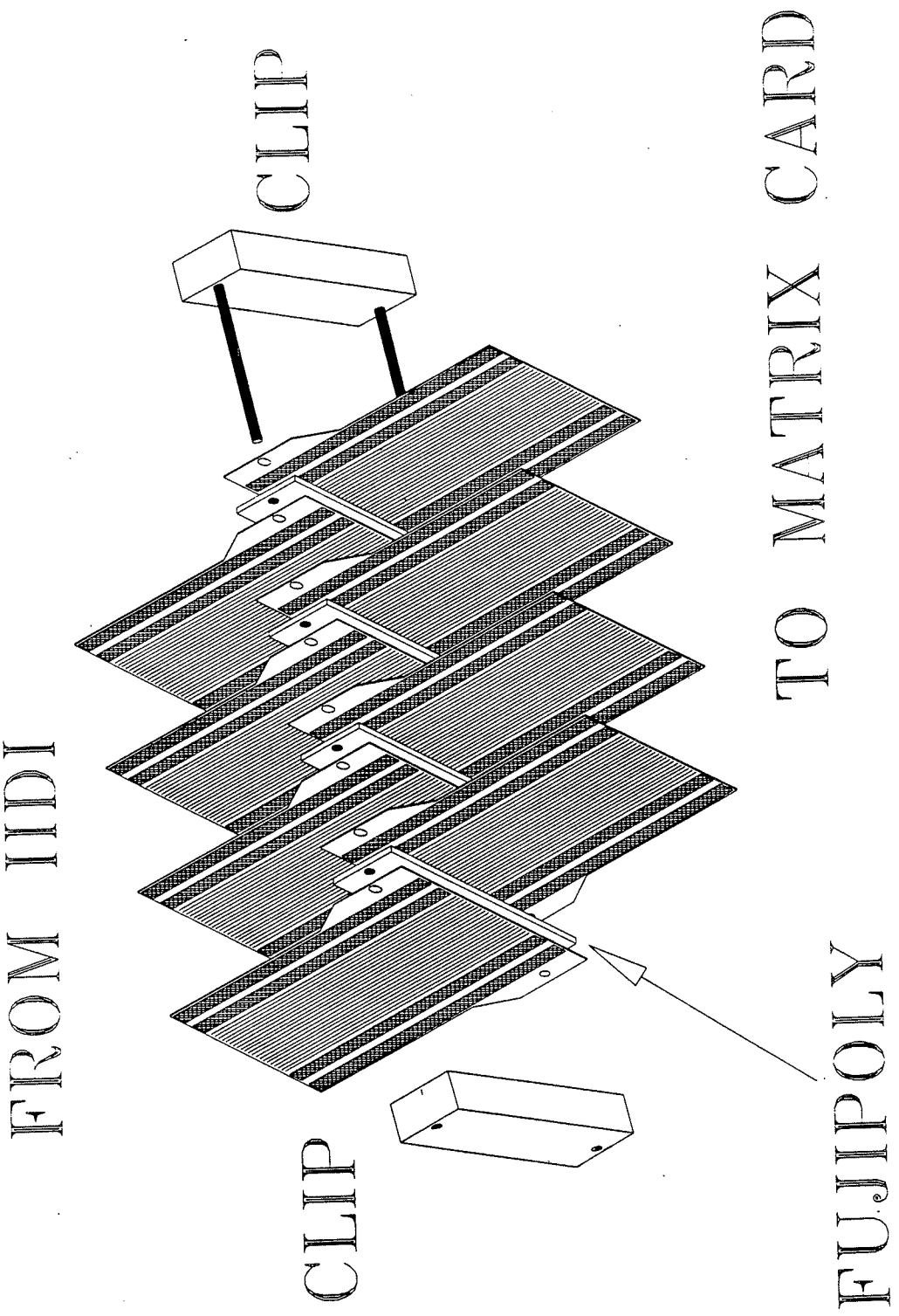

Figure 6.6: Single low-mass clip used to make the Fujipoly connections.

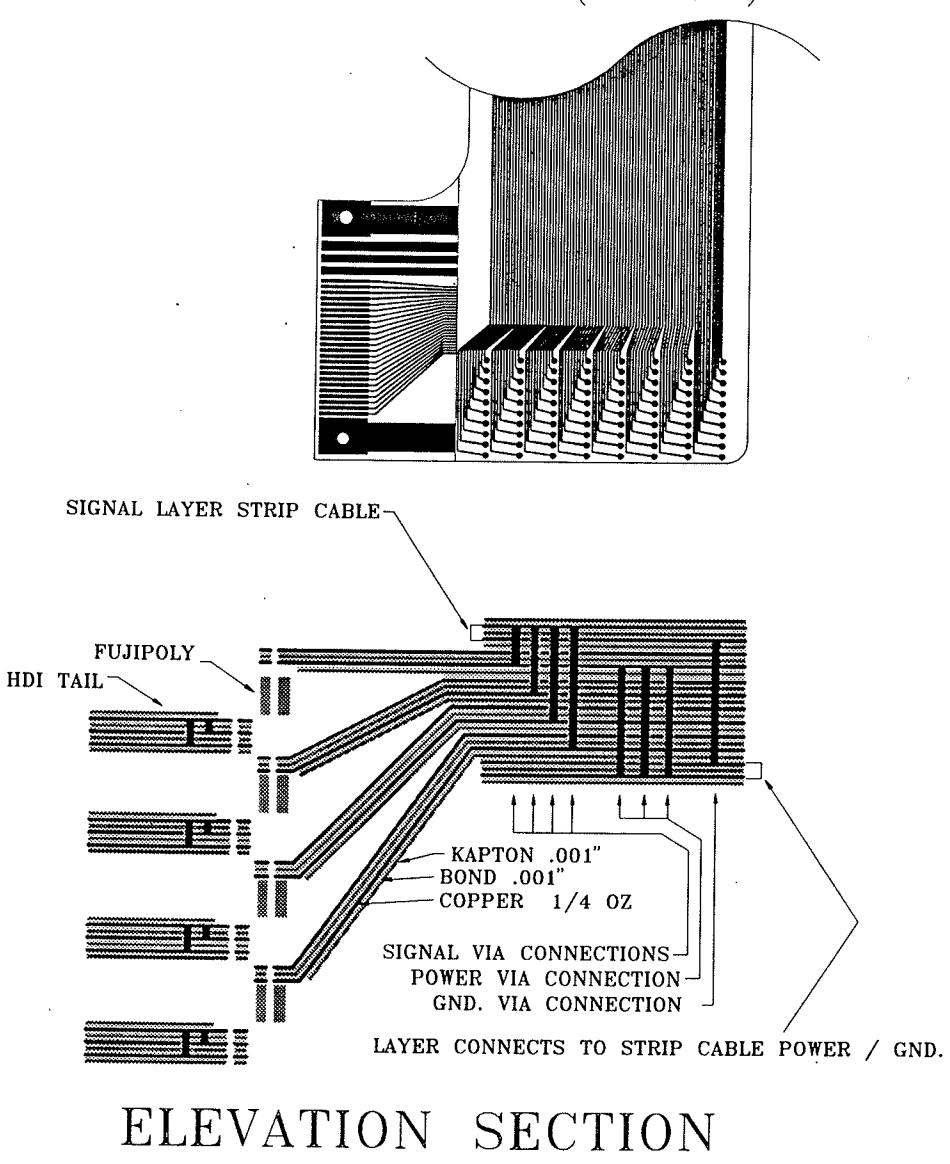

Figure 6.7: The matrix card.

polyimid substrate, bonded to Al power and ground foils on one side. For soldering to the matrix and transition cards, the traces flare out at either end.

The characteristic impedance of the strip cable, interpolated from model measurements, is 50 Ω. Using the TI 053 transceivers, we have driven and received a 65 MHz square wave over 1.5 m of model strip cable with acceptable noise margin and symmetry. At present we have three model strip cables corresponding to the most recent design parameters under construction by one vendor.

6.5 Transition Card and Coax Cable

The transition card, shown in Fig. 6.8, is a 2-layer circuit connecting the strip cable to the multi-coax cable and power cables. On the strip cable side it resembles the matrix card and, like the matrix card, it is soldered to the strip cable. On the coax side it accepts standard multi-pin connectors to which the multi-coax and power cables are soldered. The multi-coax cable is a high bandwidth miniature 50 Ω multi-coaxial cable on 50 mil centers. It is commercially available.

6.6 System Mass

Within limits imposed by practicality and acceptable performance, the overriding design consideration for the HDI and cable subsystem has been its mass. The mass of the HDI, HDI tail, Fujipoly connector, matrix card, and strip cable are tabulated in Table 6.2. The relevant quantity is the Si-radiation-length-equivalent azimuthal-average mass, weighted by the ratio of the inverse radius of the mass increment to the average inverse radius of the active silicon (next-to-rightmost column in table). The silicon, HDI, HDI tails, matrix cards, and strip cables correspond, respectively, to 1.44, 1.42, 0.55, 0.66, and 1.35 kg of silicon equivalent, for a total of 5.42 kg including the Si. Therefore these categories of inert mass on average amount to 2.76× the active silicon radiation length, or 0.041 X_0.

We continue to study an alternative design ("low mass design" in Table 6.2) in which the HDI tail, matrix card, and strip cable are replaced by one cable in which the signals are carried by parallel 3 mil diameter Al wires. We do not yet understand how to connect these wires to the HDI. If it proves to be practical, such a design could reduce these categories of inert mass to 2.26× the active silicon.

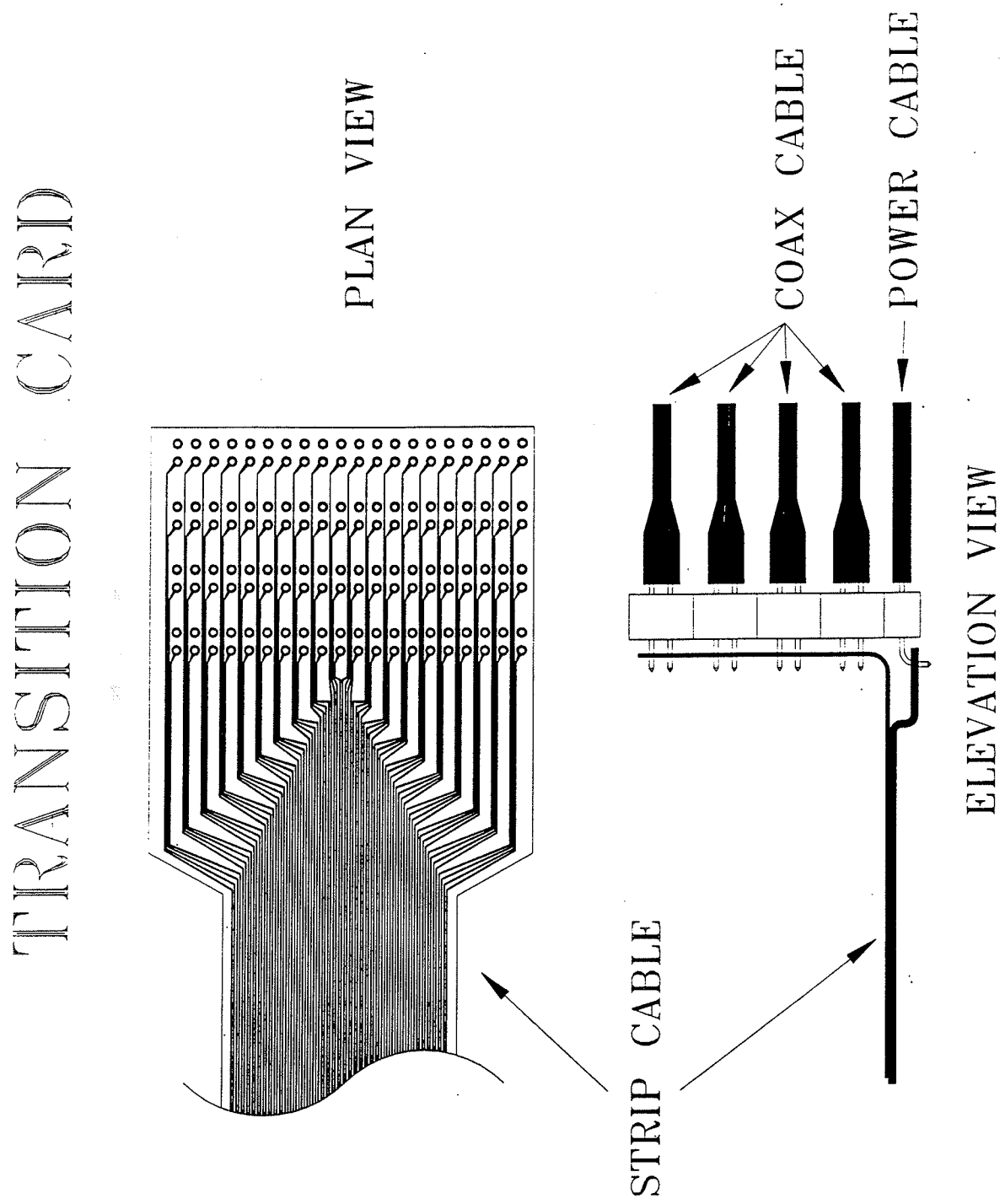

Figure 6.8: The transition card.

Baseline Design:

	Mass (kg)	Mass (Si eq kg)	R^{-1}-Weighted Mass (Si eq kg)	Radiation Length (%)
Silicon	1.44	1.44	1.44	1.4
HDI	1.57	1.61	1.42	1.4
Tails	1.25	1.16	0.55	0.6
Matrix cards	2.31	1.68	0.66	0.7
Cables	4.69	3.43	1.35	1.4
Total	**11.26**	**9.32**	**5.42**	**5.5**

Low-Mass Design:

	Mass (kg)	Mass (Si eq kg)	R^{-1}-Weighted Mass (Si eq kg)	Radiation Length (%)
Silicon	1.44	1.44	1.44	1.4
HDI	1.83	1.90	1.69	1.7
Tails/cables	4.55	3.75	1.57	1.6
Total	**7.82**	**7.09**	**4.70**	**4.8**

Masses for two possible designs. The baseline design is that detailed in the text, consisting of HDI, tails, matrix cards, and strip cables extending to z = 150 cm. The low-mass design has a single cable with aluminum conductors running from the HDI to z = 150 cm. This option would be significantly more difficult to build than the baseline. The radiation lengths quoted are at normal incidence, assuming the inverse-radius weighted mass is concentrated in a cylinder at the typical silicon radius (6.1 cm).

Table 6.2: Mass of the HDI and cable.

Chapter 7

Assembly, Production, and Testing

7.1 Overview

7.1.1 Sub-Assemblies

The silicon vertex detector is assembled in a modular fashion. The basic building blocks are the 12 cm long ladders and the 30° wedges. Seventy-two ladders are arrayed in eight cylindrical concentric sub-layers to form a "barrel module". Beryllium bulkheads of a dodecagonal pattern at the ends of the barrels provide the major structural and aligning elements of the barrels; one of the two bulkheads incorporates the water cooling channel. Twelve wedges are mounted on a dodecagonal channel to form a planar "disk module".

Seven barrel sub-assemblies (six with an attached disk) are mounted inside a 2.2 m long carbon-fiber half-cylinder which is the primary structural element of the detector. Two special sub-assemblies, each consisting of three disk modules, complete the detector and are mounted at the ends of the seven barrel structure.

Bringing this whole assembly together in a fashion that leads to a reliable, functioning, accurate, and surveyable detector is the major task of the silicon vertex detector project. The complications introduced by the large number of signal carrying cables, and the water manifold connections make this formidable task even harder.

7.1.2 Assembly and Testing

Thorough testing of each ladder and wedge is required to avoid costly or even impossible back-tracking during the detector assembly. The silicon detectors themselves are tested in a probe station as described in Section 2.4. The HDI is a multilayer printed circuit board made of thin kapton; it will carry the SVX-II digitization IC's, FutureBus transceiver chips, and associated discrete components. Discrete components will be mounted on the HDI before it is glued to the beryllium heat spreader and support plates. Then the remaining components are mounted and wire-bonds are made between the SVX-II chips and the HDI. At this time, burn-in and extensive electrical tests are carried out using the test features incorporated into the SVX-II IC design. Strip detectors and HDI's on beryllium plates are glued together, on two support rails, and the wire-bonds between the two strip detectors as well as the SVX-II to strip detector bonds are made. Testing of the completed ladder is carried out utilizing an

x-y movable table and a pulsed IR light source with a spot size ($\sim 30\,\mu$m) less than the strip pitch. Each and every strip is thus tested in a functional setting. The same assembly and testing procedure applies, *mutatis mutandis*, to the wedge detectors. A similar, but more complicated process, applies to the assembly of the double-sided detectors.

Barrels are built by assembling ladders onto the two bulkheads. The bulkheads are held in proper registry with each other by appropriate fixturing. Detailed design of this fixturing has not yet been carried out, but we envision a rotatable fixture that will allow ladders to be mounted using always the same, vertical, orientation. Ladders, with their approximately 20 cm long HDI stripline extension (the "tail"), held with a proper guiding fixture are brought in and mounted on these bulkheads. This mounting takes place under a coordinate measuring machine (CMM), which allows the immediate checking of the proper placement of each component. Ladders are glued onto the bulkheads to ensure a good thermal conduction path, but the non-reversible aspect of gluing imposes stringent requirements on timely testing. Past experience with the CDF silicon vertex detector and at other laboratories shows that a significant number of defects get introduced at this time, presumably as the result of stressing during handling. Lacking actual experience we envision that within a day, or less, of the mounting of a ladder extensive electrical testing takes place; in this way, defective ladders can be removed before the glue sets completely.

7.2 Barrel Component Fabrication

7.2.1 Construction

Ladder silicon will be supported by two "rails", each of which is composed of boron/carbon unidirectional fibers glued to rohacell foam. The foam will be sealed from moisture absorption with the use of an epoxy. The combination of carbon and boron fiber has been selected based on its thermal performance. Boron fiber (a Textron product with an expansion coefficient of 4.5 ppm/°C) is mixed with two plies of carbon fiber (roughly 0.0 ppm/°C) to produce a composite expansion coefficient of 2.6 ppm/°C, the same as for silicon. Temperature changes within the detector volume, different from the assembly and inspection temperature, will result in a uniform contraction of the ladder, minimizing out of plane motion that would otherwise result from a mismatch of the fiber/silicon contraction coefficients.

The silicon will be glued to the support rails using Hexcel 5313 epoxy. Preliminary tests have been performed on this material to determine adverse effects on the silicon detector performance. This epoxy has also been tested for high ion impurity content (ppm concentrations of Cl, Na, and K) which could poison the active silicon detector on which the rails are mounted (in the case of double-sided detectors).

Final selection of adhesives for other bonds in the ladder structure remains to be made. A silver-filled epoxy, such as TraCon 2902, has been considered for SVX-II chip attachment and for the attachment of ladders to the beryllium bulkheads. Measurements made on this epoxy reveal a bulk conductivity of roughly 1.1 W/m-K. Copper-filled and nickel-filled epoxies are under consideration as alternatives which might have a significantly lower equivalent silicon mass. Beryllium has been chosen as the substrate material because of its high stiffness to weight ratio and its long radiation length. In order to limit equivalent silicon mass, only local

electrical connections will be made between the HDI kapton structures and the beryllium heat spreaders; the remaining regions of these joints will be made with an electrically insulating, thermally conductive epoxy.

Certain fixturing will be required during the ladder construction steps. Molds will be used to form the required rails. These rails are not an item with very tight tolerances, and a simple mold fixture is more than adequate. On the other hand, the assembly of the silicon, the rails, and the HDI's into a ladder is a delicate and precise operation. In principle, the ladders will all be constructed by aligning the two silicon detectors using the ϕ side strips. This will be achieved by laying out the detectors between micrometers and optically positioning them using fiducials on the silicon detectors. The single-sided ladders have their ϕ strips opposite the side where the rails are mounted. Detectors will be aligned "dry", then glued to the rail support with the ϕ side up. A set of reference notches in the beryllium, used in mounting the ladder to the active bulkhead, will provide the beryllium reference for aligning the silicon traces. The HDI, on its beryllium plate, will then be mounted onto the silicon surface referenced to the ϕ strips. Wire-bonding will be done after the adhesive cures.

The double-sided ladders, on the other hand, present more difficult assembly problems. Again, alignment of the two silicon detectors must be done from the ϕ side. However, for these ladders the ϕ side will be on the same side as the cooling channel. The beryllium plate used to align ladders to the bulkhead will be placed on top of the silicon with a tested HDI already in place. The detectors must be aligned on a fixture on which they are held down by vacuum chucks. This fixture must enable the two detectors to be moved to the wire-bonding machine while the suction needed for holding the detectors down is maintained. ϕ-side wire-bonding is accomplished and the support rails are epoxied in place, on the ϕ-side. Interference between the rails and the wire-bonds is avoided by the introduction of a 0.5 mm cutout in the rail support which spans the wire-bond region. Once cured, this structure can be removed from the vacuum chuck, and then it will be flipped over for the stereo side HDI gluing and stereo side wire-bonding.

The outlined procedure implies that during this part of the assembly half-built ladders are being moved around, and even may be temporarily stored, using vacuum chucks. This implies that we will need a fail-safe and mobile suction system.

7.2.2 Testing

At this point, each completed ladder will be tested using a short IR light pulse with a tight light spot. The testing setup is already functioning and has been described in reference [1]. A setup at UC Riverside using a high quality commercial collimator and a microscope for back projection has produced a spot of 10 μm diameter as shown in Fig. 7.1. A much simpler setup at Fermilab using only two lenses, shown in Fig. 7.2, and with no collimation has produced a spot approximately 70μm in diameter. This laser can be pulsed at a very high rate (100 kHz) and with a very short pulse (10 ns), thus a lot of data can be accumulated over a very short time. In a few minutes all strips of a detector can be probed at three different locations, as the detector gets moved underneath the luminous spot. With a small spot (as in the UC Riverside setup) one can study the pulse height of each individual strip and create a "gain curve" file. The bigger spot of the Fermilab setup allows for a good functional test, but not as good a "gain" measurement. We will try to modify the Fermilab setup to produce

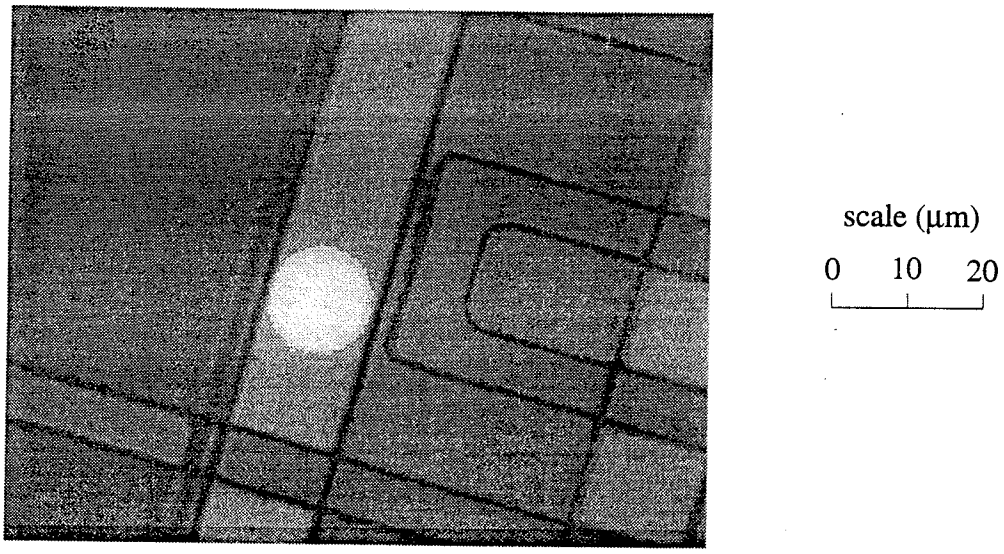

Figure 7.1: UC Riverside IR Test. Photomicrograph of the laser spot image on the surface of a silicon detector. A visible light source was used to take the photograph.

smaller spot size too.

The solid state laser used operates at a wavelength of 1064 nm, a wavelength chosen because the high resistivity silicon used in the detectors is partially transparent to it. Fig. 7.3 shows the attenuation as a function of silicon thickness as measured with the UC Riverside setup. We see that the attenuation length is 206 μm, and so this laser testing will test the whole depth of the 300 μm thick detector and not just a surface layer.

The laser test stand which will be used to exercise the electronics will require a relatively fast readout system, an x-y moving table to shuttle the completed ladders underneath the laser head, and its own water cooling system. Completed ladders will be mounted onto a test structure which will provide this cooling. The test structure will be mounted onto the x-y moving table, and the whole setup must be in a dark and dry environment.

7.3 Barrel Module Fabrication

Barrel bulkheads, both active and passive, will be precision machined objects with reference features built into them. Reference features will likely be the outer circular surface of the bulkheads or the hexagonal outer ledges, and appropriately placed holes. Bulkhead ladder mounting features and references will be surveyed and software corrections will be used to determine the bulkhead best fit center, using ledge locations, relative to the reference features. A CMM machine will be used to properly rotate and offset the active and passive

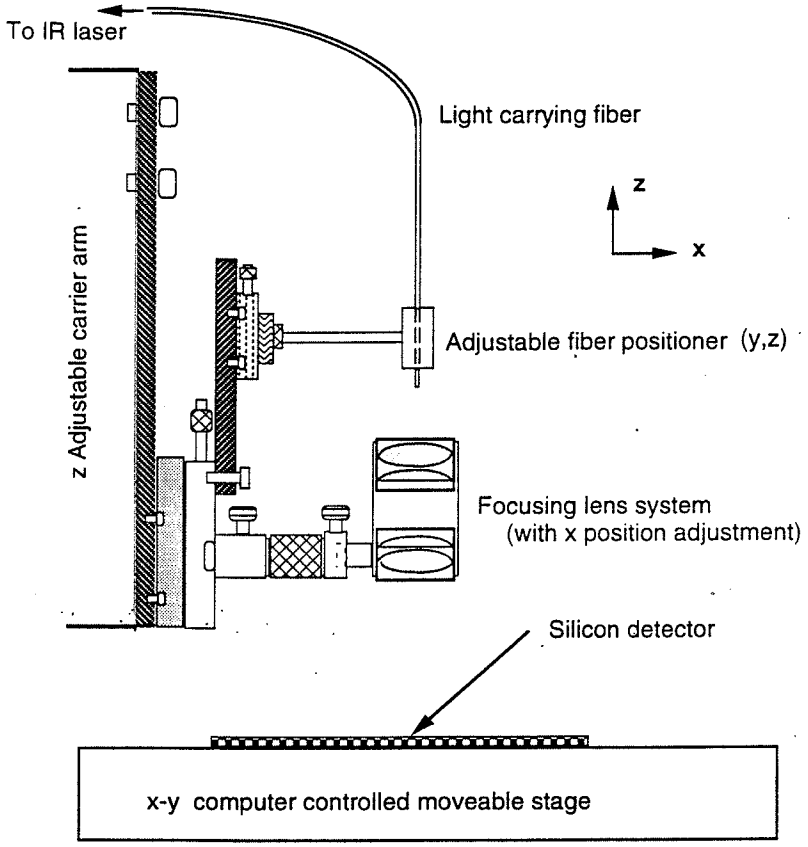

Figure 7.2: FNAL Laser Test.

bulkheads, based on the best fit centers, relative to one another in a fixture (see Fig. 7.4).

Two options are under consideration to achieve the bulkhead to bulkhead alignment. In the first option, which is shown in Fig. 7.4, bulkheads would be mounted in circular rings, each of which have a known center of rotation. The bulkheads would be mounted in the ring such that the best fit center would coincide with the rotation center of the support ring. Two support rings, each with an active and a passive bulkhead, will then be mounted into the fixture and affixed to one another with connections near the outer radius. This alignment mechanism requires that the rollers on which the two bulkheads are mounted and rotated each have their rotation axes collinear.

The second alignment option follows the technique used in the CDF SVX and SVX′ construction. In this case the two bulkheads are mounted on wheels, each of which has the rotation center placed at the best fit center of the bulkhead. The wheels are mounted on a shaft which extends through the barrel region. Rotation of the shaft then ensures the two bulkheads rotate properly, relative to one another. The spokes of the two wheels of this kind of fixture will very likely interfere with the tails of the HDI's during assembly, and such a scheme may prove unworkable.

Ladder installation needs to be further studied. Ladders will be installed starting at the inner layer and working outward. The long HDI tails will need to be wound on their paths such that they do not interfere with ladder positions in other locations. Full scale G-10 models of the bulkheads and the ladders are presently being fabricated. These models will be used with realistic HDI tails to study the cable routing and installation procedures.

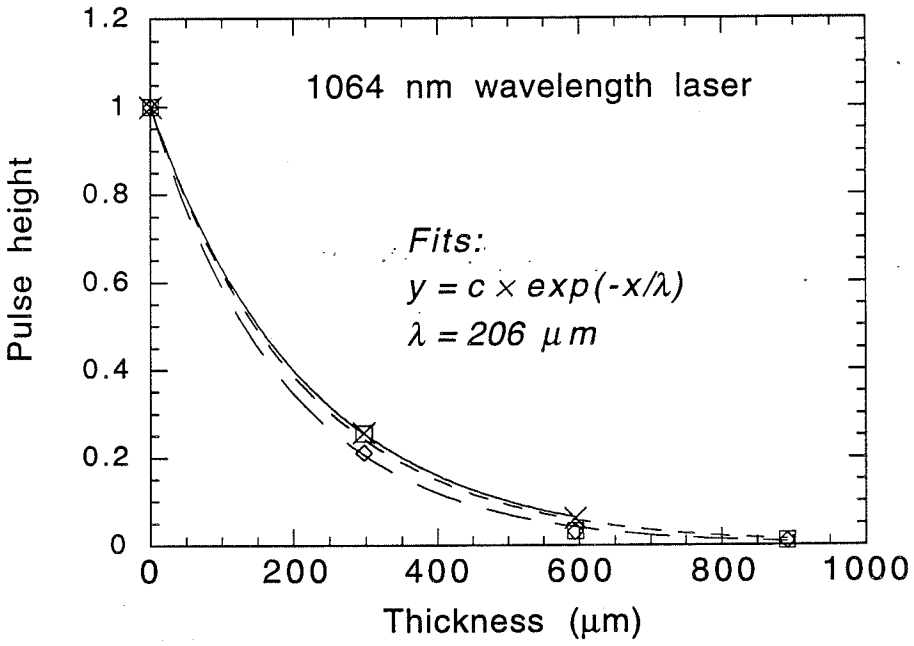

Figure 7.3: Attenuation of laser light. $\lambda \geq 206\,\mu$m is a lower limit because the effects of reflection were neglected. This shows that the laser probes the whole thickness ($300\,\mu$m) of a silicon detector.

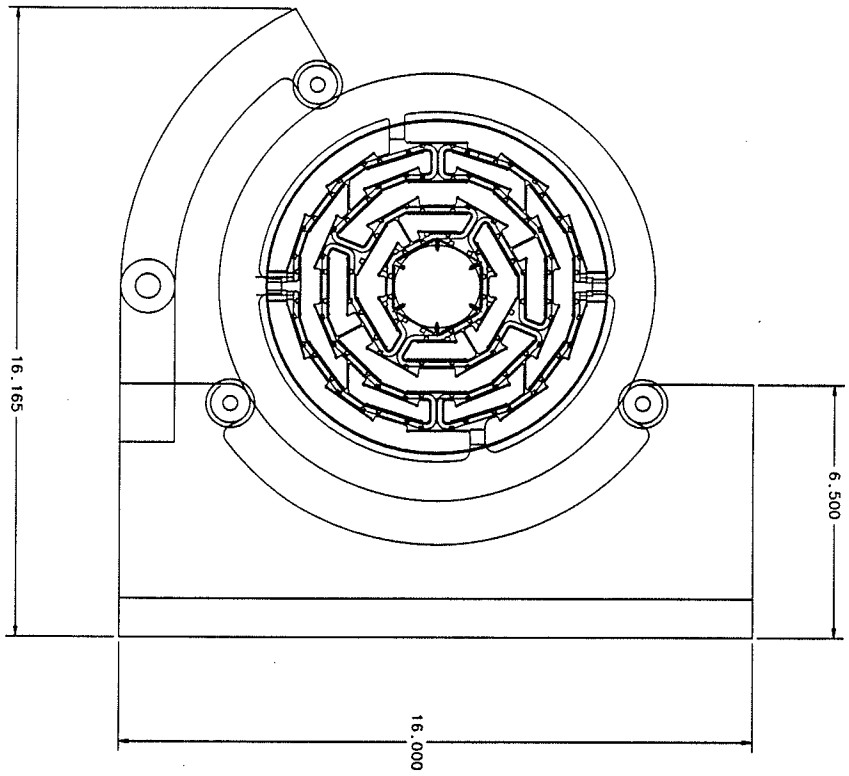

Figure 7.4: Bulkhead Rotation Fixture

Ladders will be installed through the bulkhead layers. Double-sided ladders have a stack height of 2.3 mm above the active bulkhead (see Tables 4.4 and 4.5). With a layer to layer clearance of 10.25 mm ladders must be installed with 3.5 mm total clearance, in the worst case clearance location. Ladder handling during installation will require a fixture which holds the HDI tail and enables manipulation of the ladder through the tight clearance. With the ladder design being finalized we can now devote our design effort to this fixture which will need to have vertical and lateral movements, as well as ladder tilt and yaw movements. Various ladder styles, lengths of tails, and widths of ladders will need to be accommodated; all these requirements translate to a rather sophisticated handling fixture. We also expect that the lessons to be gained from our modeling efforts will guide the design of this fixture.

Ladders will be optically surveyed once mounted into position on the bulkhead. Access must be maintained such that reference features on the ladders can be seen during barrel assembly. Ladders will be glued to the bulkhead ledge and pinned into place on both ladder ends. When possible, ladders will be tested on the bulkhead before the glue sets so that they can be removed easily and repaired.

7.4 Disk Module Fabrication

Wedge components of the disk will be built individually, with the mask of the silicon referenced optically to the holes in the beryllium mounting plate. The wedges will be connected

onto the dodecagonal ring structure which contains the water cooling channel, six per side. Wedges will be screwed to the ring structure eliminating the need for adhesive in the contact region. A thermally conducting grease will be used here, and this will allow for an easier removal of defective wedges. Planarity of the wedges will be dependent on the machining tolerance of the beryllium ring, with correction near the beam pipe using a carbon fiber support ring. This assembly will be carried out under a planar CMM machine that will allow for immediate surveying of the location of each wedge.

The long HDI pigtail must be held in place during construction of the individual wedges and during installation of the wedges onto the ring using an auxiliary support fixture in the shape of a ring with legs in the z-direction on both sides. Wedges will be surveyed in place once installed onto the ring structure and electrically tested.

The testing procedure will be similar to the one used for the ladders and the barrel modules. The laser test will also be a major part of the overall testing sequence.

7.5 Barrel Sub-Assembly Construction

Once barrel and disk modules have been constructed, surveyed, and tested they will be brought together into sub-assemblies. The disks will be mounted from the barrel active bulkheads. Control of the relative z locations and the relative ϕ rotations of the two components of the module will be done using posts permanently attached to the disk. No adjustment will be possible since final machining of the bulkhead end of the posts will be done with the posts attached to the disk structure (see Section 4.3.2)

The cables of both the barrels and disks will be merged into common bundles for the whole sub-assembly. Adequate allowance must be made for them to be held until the module is installed into the support half-cylinder. Again proper handling, support, and storage fixturing for the various components of the sub-assemblies and the completed sub-assemblies remain to be designed.

Sub-assemblies will be thoroughly tested prior to being installed into the support half-cylinder. This testing will be done using a readout station near the assembly location. The test station must have a chiller to supply fluid to cool the electronics during testing. A dark and dry box for this test and a relatively elaborate data acquisition system will be required.

7.6 End Disk Modules

Two end disk modules are required, in addition to the barrel sub-assemblies, to complete the silicon vertex detector. Each end disk module will contain three disks. Control of the z-offset of the disks and their relative ϕ orientations will be provided in a manner similar to that used in the barrel/disk modules. Disks will be assembled into modules, tested, and installed onto the detector ends once the seven barrel sub-assemblies are installed into the support half-cylinder.

7.7 Final Assembly and Installation

"Kinematic" mounts hold the barrel and disk sub-assemblies in the semi-cylindrical support at approximately the 3, 6, and 9 o'clock positions. The task faced at this point is to insert all the sub-assemblies in a controlled and accurate fashion into the half-cylinder support. Certain considerations jump immediately to one's attention:

A large CMM is desirable at this stage: a machine that can accommodate the whole 2.2 m long structure. Such a machine is not readily available at this time.

Pre-loading will be required. Since we want to know the exact position at which each sub-assembly comes to rest, we will have to simulate the loading of the rest of the modules (including the weight of the external cables) by appropriate use of ballast weights. In a similar fashion, the support of the GEC cylinder will have to simulate the one to be used in the DØ detector proper.

The assembly sequence has to be thought out in detail. At this time it seems that cabling would suggest that one builds from the outermost (*i.e.* at large values of $\pm z$) sub-assemblies towards the middle. Ease of movement and positioning of the last sub-assembly argues towards a scheme where sub-assemblies are put in sequentially starting from one end. Nevertheless externalities, such as the availability of the requisite sub-assemblies at certain points in the assembly, may force us to assume a more flexible sequence of operations. The delicacy of this operation is illustrated by the fact that we wish to have clearances of 1 mm between barrel sub-assemblies! Special moving devices and fixturing will be required at this stage.

The tails of the HDI's will be bundled together at the 1, 3, 5, 7, 9, and 11 o'clock azimuthal locations. These bundles will have to be threaded through appropriate slots in the semicylindrical support, and through similar slots in the semicylindrical covers as well. This requirement also imposes its own constraints on the handling fixture to be used.

Connections to the external cabling (via the so called matrix card) as well as to the water cooling manifolds is the next step. This will allow one more chance to test the integrity of the newly installed sub-assemblies. Again the requirements of cooling water, electronics for data readout and testing, darkness, and dry atmosphere have to be met – but this time for the whole 2.2 m long structure!

With the design of the various sub-assemblies now beyond the conceptual design stage, serious consideration can now be given to this final – and crucial step. In addition questions of surveying, incorporation of fiducial monuments, and the chain of measurements that will be required for an accurate transfer of these measurements to the outside world remain to be answered.

Installation of the beam pipe through the completed detector and the installation of an outer skin and end covers to form a dark quasi-hermetic enclosure are the two last steps at this stage.

The scheme to be used to support the completed detector from the scintillating fiber tracker and the solenoid has to be worked out in unison with the mounting of the other components of the DØ upgrade tracker. We are in the process of initiating this design effort. In addition, the fixtures and equipment that will be required to transport this beast into the collision hall and slide it into the detector remain to be designed.

Many of these uncertainties will be resolved naturally as the design matures, as models

get built, and as experience accumulates. At this point we are confident that we can carry out the envisioned operations.

Bibliography

[1] M. Vaz, S. Cihangir, and P. Rapidis, *Pulsed LASER for Testing Silicon Strip Detectors*, Fermilab-TM-1849 (July 1993).

Chapter 8

Software

8.1 Long Range Plans

8.1.1 Motivation

The long range silicon software plans have been driven by the need to provide capability for monitoring detector performance, calibration, and diagnostics. With the large number of channels in the silicon detector ($\sim$ 900k channels in the full installation) it is no longer feasible to think of controlling these operations from a single central processor node as is done in the present detector. The storage requirements for histogramming 900k channels is overwhelming. With 256 bins per histogram (8-bit ADC) plus additional overhead for overflow/underflow bins, title, and so forth the total exceeds 0.5 GBytes.

8.1.2 Proposal

To meet these needs we plan to install a VME processor board in each SAR crate. Processing events in the SAR crates has very obvious advantages; however, there is the potential drawback of impacting the data acquisition system by competing for events on the VME backplane. To avoid any contention for the VME bus with the data acquisition system we propose to install VSB (VME Supplemental Bus) in each SAR crate and use this as a separate data bus. By requiring that all VME transactions take absolute precedence over VSB transactions in the SAR cards, this parallel data bus remains totally independent of the VME and free of any problems of contention. The bottom line is that this will cause zero deadtime in the data acquisition system. The processor board we will use is a Motorola MVME166 which is based on the 68040 processor chip and has both VME and VSB interfaces. These processor boards have ethernet interfaces for communication with the outside world thus removing our dependence on the Token Ring.

Since we will be doing data acquisition completely independent of the normal readout system we opt for a real-time operating system for our MVME166 processors. The system we are presently evaluating is VxWorks from Wind River Systems. We have several reasons for choosing VxWorks over its many competitors. The Online Support Group in the Computing Division at Fermilab uses VxWorks in both the Sloan Digital Sky Survey (SDSS) project as well as the DART project, which is the data acquisition system for the next fixed-target run

at Fermilab. One offshoot of these two projects is the development of a tool kit to supplement VxWorks, VxTools. There are two features of VxWorks that are a great advantage for the programmer: the ability to do all code development in the C programming language and VxGDB, the symbolic debugger. Both of these will figure prominently in developing our code in a timely fashion. In addition to the front-end processor code we will also develop a user interface for communicating with these processors. This represents a step toward using commercially available hardware to replace "homegrown" electronics and gives us a more flexible system with regard to any future upgrades.

We find many advantages to this proposal, several of which trace their origins to the fact that we will use distributed processing. This gives us a system which is highly parallel thus making each crate independent of all other crates. By analyzing the data locally to the crate, we minimize the distance over which the data must be transported resulting in a system which is operationally fast. Not moving the data out of the local crate also makes this system independent of the DØ DAQ system. One final point we stress about our design is that we will be fully integrated into the DØ environment; that is, we will communicate with the DØ Alarm Server, database servers, and the COORdinate process which maintains a global list of crate ownership (a necessary function to assure that there is no contention for the electronics), to name a few.

Like any new proposal, we also see a few disadvantages as well. Foremost among these is that installation of the requisite number of front-end processors (1 per SAR crate) and the investment of time to develop the code represents a not inconsequential investment. One of the largest investments of time results from replacing the Token Ring interface with an ethernet connection. This means that we must write our software to respond to the protocols of the DØ Controls System. It also means replacing a part of the DØ Controls System which uses the "Goodwin system", a proven workhorse in the present DØ detector; however, the "Goodwin system" has one major flaw in that it is not easy to accommodate new applications. When all is considered, we strongly feel that the advantages far outweigh the disadvantages.

8.1.3 Functionality

The detector performance monitoring task will run during data taking. This has the very nice feature that we can use the Level 1 accept rate rather than the Level 2 accept rate which is a few orders of magnitude lower; it provides us with the necessary statistics in a much shorter period of time. We do not plan on reading all the data from each SAR for each event to accomplish this task; instead, we propose to read 1 HDI/SAR/event. This significantly reduces the demands on the VSB for reading the data which is important because we will use a simple polling technique for reading the data rather than responding to interrupts on VSB. All of the histograms will be stored in the local processor, this being a manageable subset of the total number required for the entire detector, from which we will compare with certified standards to flag channels as possibly being bad. We will alarm on any bad channels found. In fact, the definition of what constitutes a bad channel and what to do about it is completely unspecified at present; this will evolve over time as we acquire experience with the working detector. Through the user interface, all information stored by this task will be uploadable if requested.

For detector calibration we will use the front-end processor for control of the procedure. This includes all configuration tasks, including necessary downloading, data acquisition and analysis, and reporting of results. Since we will be implementing the DØ Controls System protocol, we will also be able to communicate with the hardware database servers and make appropriate updates. We will communicate with the COORdinate process to assure exclusive ownership of the crate. By placing full control in the front-end node we will be completely independent of and in parallel with the other SAR crates. In addition, this will no longer require the DAQ system as the data will remain in the front-end crate. This is an important aspect of the proposal as it results in maximum speed. Despite not utilizing the DAQ system for reading the data, all information collected will be uploadable to the user; this includes a mode whereby events can be individually uploaded if requested.

To provide diagnostics for troubleshooting potential problems in the readout electronics, we will develop code to run in the front-end processor. Full testing of the data flow across both the VME bus and the VSB bus will be implemented. In addition, code to test all the electronics modules in the crate will be written. A preliminary development of this code will be utilized in the test stands that will be outfitted. The user will have full dynamic control of this system allowing for the tests to be reconfigured "on the fly". As in all of the other procedures we will write, all information will be uploadable to the user. We will communicate with the COORdinate process to assure exclusive ownership of the SAR crate.

The user will need to communicate with the local processor in order to send control messages, to download standardized histograms, to request data histograms to be uploaded, and to display results from these histograms (either raw or possibly processed in some way). This communication will be via a user interface program running on the user's workstation or PC, sending messages and data via ethernet to the local processors. The likely users of this interface are experts and shift takers, so it should be both flexible and easy to use. We intend to create a graphical user interface and are exploring the use of Motif or some alternative, such as Tcl/Tk. Our final choice will permit the user to run from either VMS or UNIX, and we will explore running the user interface on a PC, as well. It will be possible to request histograms for specific channels of interest and to store these in HBOOK format. The program will include a displayed summary of the general performance and status of the detector.

8.1.4 Schedule

It is clear from the proposal that this is an ambitious project and no small undertaking. It is difficult to provide time estimates until a more complete specification is realized, but we list below some guesses for some of the components.

Complete specification	~6-12 months
VxWorks local program:	
• communication with the DØ world (including CDAQ protocol)	~1 man-year
• master control process	~1 man-year
• histogramming/statistics process	~6 man-months
• local alarms process	~6 man-months
• additional	?
User interface:	
• GUI	~3 man-months
• communication with local processor	~3 man-months
• histogram/graphics displays	~3 man-months

8.2 Test Bench Plans

8.2.1 Motivation

Engineers and physicists need a way to test electronics as it is developed. Ideally, the test bench setup which is used for debugging will be the same one used for production line testing. The software that is developed is also expected to be used for diagnostics and calibration periodically while the experiment is running.

8.2.2 Proposal

The long-range plan describes using VxWorks as a real-time embedded operating system running on a Motorola 68K CPU. The test bench does not necessarily require VxWorks, but can be run on any computer with a VME interface. The test bench VME hardware starts at the back-end of the readout chain with the silicon acquisition readout (SAR) board and then supports the additional hardware necessary to reach the actual silicon microstrips (*i.e.* the port card, HDI, SVX-II, and microstrip detector). The computer can be any machine supporting VME bus access, most likely a PC with a Bit3 card or a local UNIX host managing a VxWorks MVME166.

Two existing programs are already available for debugging the electronics, PCPLOT and Multi. PCPLOT has been developed by several Fermilab employees and is currently supported by Bob Angstadt. Multi is the old Fermilab data acquisition program which was ported to C and made to work on a PC by Scott Buchholz. It has been extended to support VME interfacing via a Bit3 module. Both programs have already been used to test the first prototypes. Our main concern at the moment is the low speed of communication over the Bit3 interface. It is felt that the prototype should be tested under realistic conditions, including readout at the full VME backplane speed.

Our goal in producing a test bench system is to make a program where it is easy to edit a command file and execute it, and which runs at the final VME CPU speed. It should have an easily comprehensible control structure, and the resulting data should be available for later analysis, if necessary. There are many more desirable features, but these are of secondary importance to producing a system that operates at full CPU speed.

To meet the two main goals, we have developed a system called TE. TE is a mini-language with a structure which is a cross between Basic and C (the grammar can be modified to assume any other structure.)

TE can compile or interpret TE script files. The TE compiler will input a script file and output C code which is then compiled and run on the target platform. This is relatively inconvenient, but allows the test bench to run at full CPU speed. The TE interpreter is primarily for debugging. It will run the TE scripts $\sim 10\times$ slower than the compiled TE programs, but allows for quick and easy updates to script files.

TE can be easily extended to provide more functionality by writing C routines and adding them to the procedure table. TE is also very portable. It will run on any computer which has an ANSI C compiler. It is currently running on IBM PC's (using the Bit-3 VME interface) and runs on various Unix machines without VME support. VME support could be added if Unix VME cards were available locally. A VxWorks version will be available soon.

8.2.3 Functionality

TE is designed for readout to the local screen and to a local file. The screen provides quick feedback to the user but slows execution down. The data saved to a file is available for later analysis by whatever program is desired. The analysis platform is not the TE program but rather some other program on a workstation. Since it is important to make execution speed on the VME as fast as possible, we have shifted analysis to the offline computers. We can use many more tools for the analysis that would not be trivial to incorporate into TE. We are looking into using TE run control with graphical interfaces on the workstation. This is not essential but does make it easier to use. The offline analysis program will have graphical interfaces. The user interface is not yet fully developed but most likely it will follow the same form envisioned for the monitoring program, namely TCL/TK as the platform to build analysis programs and a graphical user interface for ease of use.

8.2.4 Schedule

A first version of TE has already been demonstrated to run on several UNIX platforms and on a DOS based PC. It has controlled VME hardware using a Bit3 interface. Until we have available a 68K MVME166 board running under VxWorks, we will not be able to demonstrate its fully functionality. Compatibility with VxWorks can be tested without the 166 board. Within one month almost all of the functionality of TE should have been demonstrated. The framework for the offline analysis on the workstations should be in place within two months. This includes the graphical user interface. It is expected that the actual analysis programs will continue to be honed for as long as physicists are willing to inspect the operation of the hardware.

Chapter 9

Silicon Tracker Beam Test Proposal

9.1 Motivation

The DØ Silicon Tracker will have 900k readout channels in its final configuration. An exposure to a beam of a small partition with 8000 readout channels will allow a minimal system test combined with collection of data on the beam response of the various detector types used in the Silicon Tracker. Identified electrons and pions with momentum 5–150 GeV/c will be used as beam particles. They will traverse the Silicon Tracker Test Array at a wide range of incident angles thus imitating as closely as possible the conditions expected in the colliding beam experiment. In addition, the large statistics beam data will be used to debug and optimize the cluster, track, and vertex finding algorithms.

We propose to conduct a beam test with the Silicon Tracker Test Array immersed in a magnetic field. Most of the parameters defining the response of the silicon detectors depend rather strongly on the strength of the magnetic field. In Figs. 9.1, 9.2, 9.3, and 9.4 we show some results from refs. [1, 2] of beam tests of silicon strip detectors with and without magnetic fields.

In ref. [1] the 200 GeV/c beam particle trajectories were perpendicular to the magnetic field and parallel to the detector electric field. The silicon detector array was made of 20 μm pitch strips. It was observed that increasing the magnetic field from 0 to 1.68 T significantly broadened the cluster size distribution. With no magnetic field the ionization charge was deposited on a single strip in about 50% of events, while with the magnetic field only 20% of events have charge deposited within one strip and 80% of events shared two or more strips. The extrapolated distribution of ionization charge within the 20 μm wide strip is shown in Fig. 9.1 for: (a) no magnetic field, (b) magnetic field of +1.68 T, and (c) magnetic field of −1.68 T. The change in the charge distribution in the presence of the magnetic field resulted in about a 6.5 μm systematic shift in the measured beam coordinate. One should note, however, that in the arrangement of the experiment [1] the holes were used as carriers of the signal. In the DØ Silicon Tracker design, both holes and electrons are used as carriers of the signal. As the Hall mobilities for electrons are about 5.3 times higher than for the holes, the expected systematic shift of the beam coordinate measured with the DØ Silicon Tracker may be as high as 40 μm with the 2 T magnetic field.

In ref. [2] the detector efficiency, the multi-strip hit fraction, and the position resolution were measured as a function of the ϕ angle of the incident beam. The measurements were

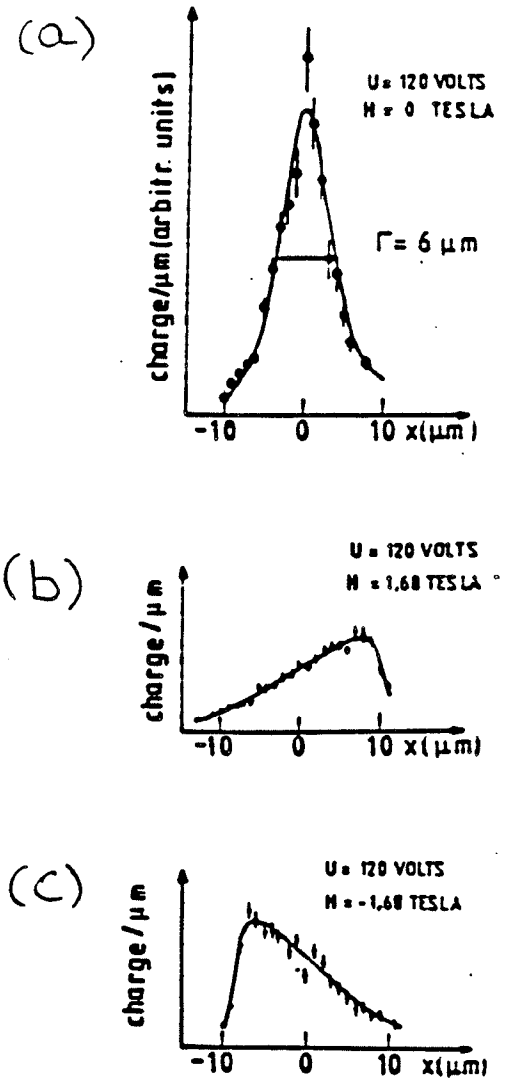

Figure 9.1: Spatial charge distribution in the silicon microstrip detector: (a) without magnetic field, (b) with +1.68 T and (c) with −1.68 T magnetic field.

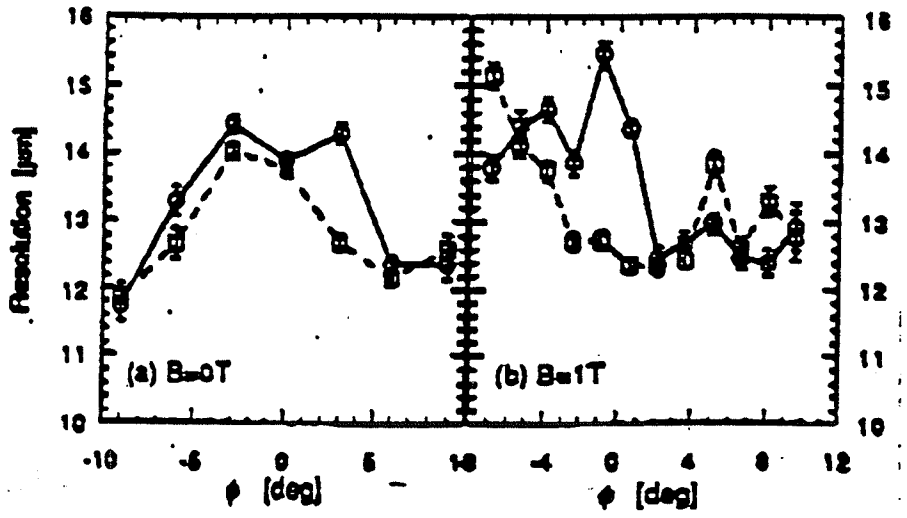

Figure 9.2: Position resolution of the silicon strip detector as a function of the incident beam ϕ angle: (a) without magnetic field, and (b) with 1 T magnetic field.

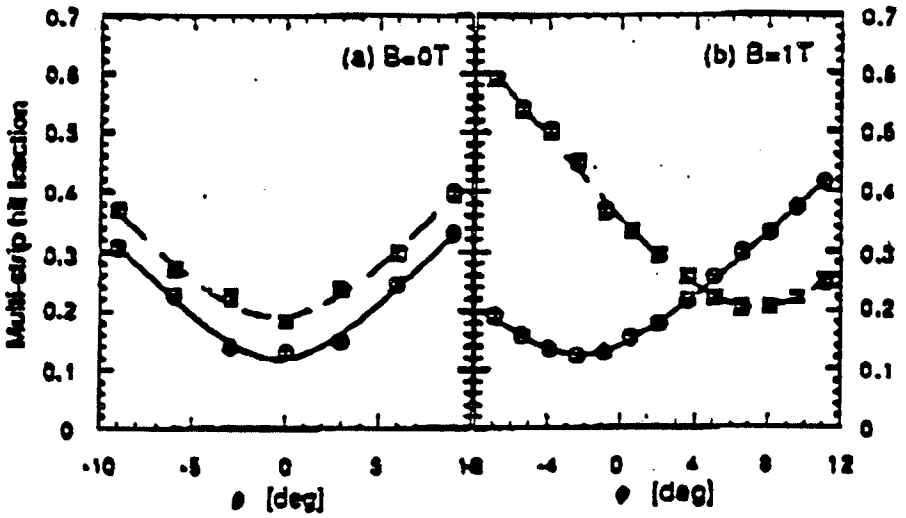

Figure 9.3: Multi-strip hit fraction in a silicon strip detector as a function of the ϕ angle: (a) without magnetic field, and (b) with 1 T magnetic field.

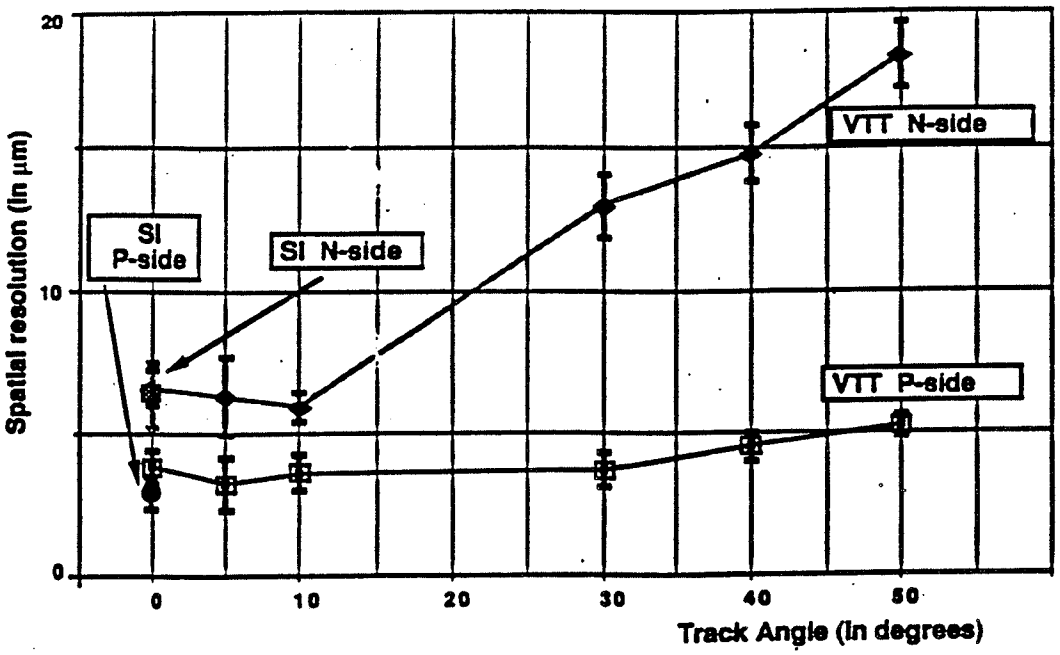

Figure 9.4: Spatial resolution of a silicon strip detector as a function of the beam incident angle.

made using a 4 GeV/c pion beam and both with and without a 1 T magnetic field. As shown in Figs. 9.2 and 9.3, a rather strong dependence on the incident beam ϕ angle was found for all the above variables. The variations in the observed distributions depend on the value of the Hall angle of the charge carrier. The changes of all measured variables were much more dramatic with the magnetic field turned on.

The dependence of the spatial resolution of the silicon strip detectors on the particle incident angle was measured in ref. [3] using a 70 GeV/c hadron beam. The change in the spatial resolution was found to be particularly strong for the n-side readout. As shown in Fig. 9.4 the spatial resolution of such detectors decreases by about a factor of 2 as the beam incident angle changes from 0 to 50°. No magnetic field was used in this study.

In a practical design of the silicon tracker the material used in the silicon detectors, adjacent electronics, signal and HV cables, and mechanical support with cooling system constitutes of the order of 5% radiation length. This gives rise to considerable multiple scattering and may affect the spatial resolution and efficiency for finding tracks and vertices. The beam study will allow us to determine precisely the effect of multiple scattering in the detectors and other material as a function of the rapidity and the ϕ angle of beam particles with various known momenta. This is very useful information for the reconstruction program.

All the above examples of the silicon strip detector response to beam particles indicate strongly the necessity of a beam test. Practically none of the above tests can be reproduced using cosmic-ray data. In addition, the proposed beam tests should be conducted with the silicon detectors in a magnetic field to reproduce as closely as possible the conditions in the colliding beam experiment. The DØ Silicon Tracker will operate in a 2 T magnetic field. In order to reduce the cost of the test-beam experiment we propose to apply a maximum field of 1 T. Measurements at intermediate values of the magnetic field should allow us to extrapolate the results to the full 2 T field.

9.2 Proposed Measurements

We propose to study the response of the various silicon detector types used in the disks and barrels of the DØ Silicon Tracker to beam particles (electrons and pions) in the momentum range 5–150 GeV/c. The measured variables will be the signal height and cluster size as a function of:

- beam momentum,
- type of beam particle,
- beam incident angle, both in θ and ϕ.

These measurements will be made at several values of the magnetic field between 0 and 1.0 T.

We shall also gather large statistics data samples with low and high intensity beams both with and without the magnetic field. These data samples will be used in debugging and optimizing the cluster, track, and vertex finding algorithms. The Silicon Tracker Test Array should be put into the DØ Monte Carlo with the same level of detail as the actual Silicon Tracker.

The addition of one layer of the Fiber Tracker to the Silicon Tracker Test Array would allow for a full test of a partition of the DØ Tracking System. It is of the utmost importance to determine the track and the vertex projections from the two tracking detectors, and their relative sensitivity to beam particles. Some of these measurements do not require a magnetic field so a larger assembly with preshower scintillators added to the silicon and fiber test array could be beam tested.

9.3 The Silicon Tracker Test-Beam Setup

9.3.1 Counter Arrangement

The proposed partitions of the Silicon Tracker to be used in the test-beam are shown in Fig. 9.5a,b. Assuming that the number of the readout channels will be limited by use of only two SAR cards (8192 channels), the test-beam assembly may consist of either one wedge with two ladders (maximum 8704 channels, Fig. 9.5a) or two wedges with one ladder (maximum 7424 channels, Fig. 9.5b). In the first case not all available silicon strips will be instrumented for readout.

The Test Array will not exceed 25 cm in length and 15 cm in diameter in order to fit inside a 1 ft long and 6 inch diameter standard solenoid magnet. A conceptual arrangement of the Test Array and solenoid magnet with a supporting turn-table is shown in Fig. 9.6. The Test Array position with respect to the beam will be set by using the four remotely controlled movements (horizontal, vertical, rotations in ϕ and θ) of the turn-table. The other option would be to move only the Test Array on a turn-table inside a fixed magnet. This solution, however, would require much larger aperture magnet leading to a significant cost increase.

The beam trigger will be provided by two pairs of the scintillation counters (S1-S2, S3-S4) and the beam trajectories will be defined by two sets of the silicon detector arrays (SiB(1), SiB(2)). The beam defining detectors will be placed on supporting tables separate from that of the Test Array and magnet.

9.3.2 Magnet

We propose to use a standard magnet based on a solenoid coil operating at liquid helium temperature. Such magnets are produced industrially. For the Silicon Tracker beam test we propose a magnet with a warm bore of about 15 cm diameter and a length of about 30 cm.

The arrangement of the 1 T magnet with a horizontal room temperature access (as required for the beam test) and a typical superconducting cryogenic system is shown in Fig. 9.7. Some portions of the supply and vent cryo-lines for both the liquid nitrogen and the liquid helium flow would be flexible to allow for limited magnet movements and rotations.

The addition of a Fiber Tracker Array to the Silicon Tracker Test Array would require use of a magnet with a larger warm bore diameter (minimum 24 cm). It should be noted that the larger bore diameter magnet would allow for vertical movement of the Silicon Tracker Test Array within the magnet, thereby considerably increasing the range of beam incident angles within the magnet aperture as the magnet and Test Array are rotated by the turn-table.

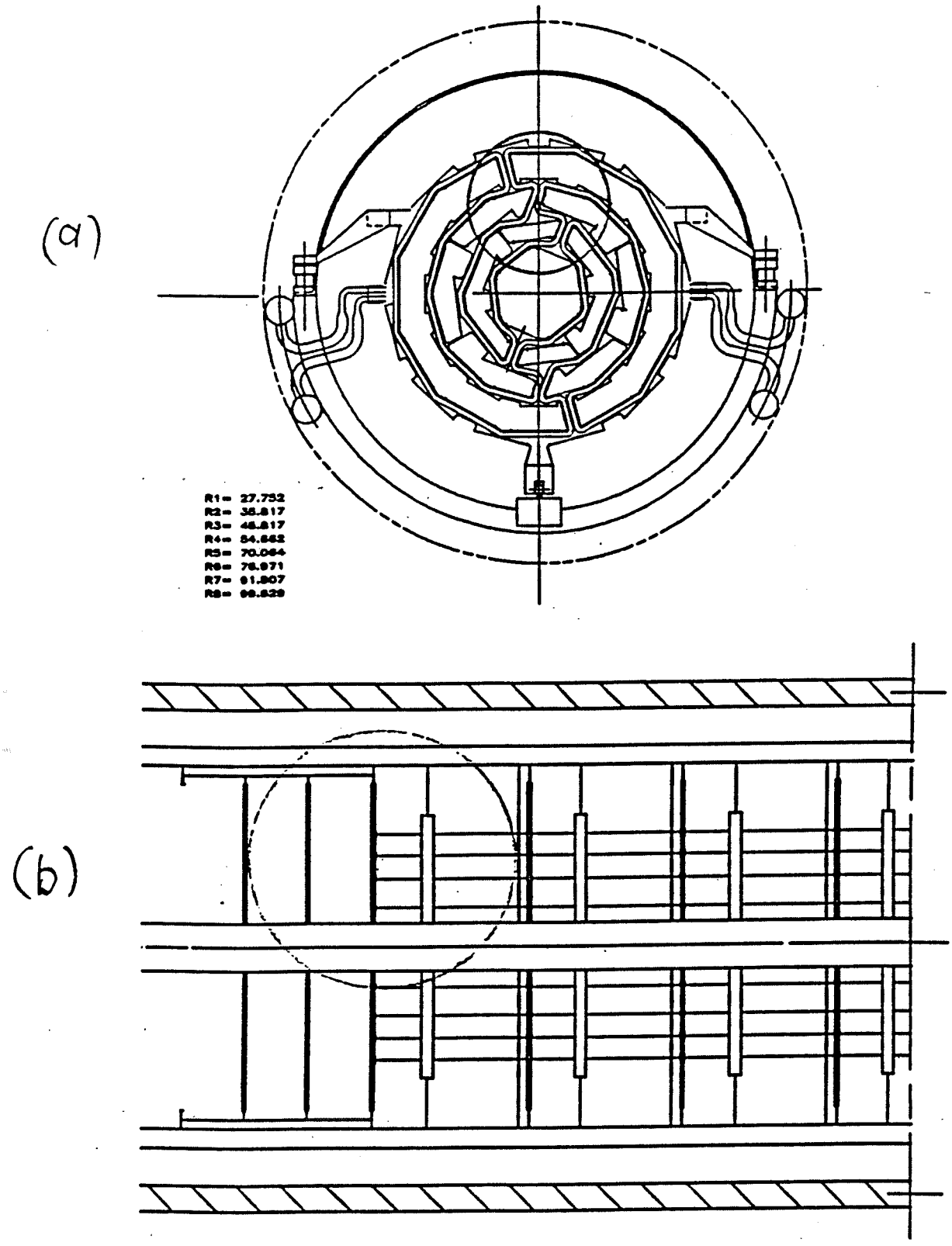

Figure 9.5: A partition of the silicon tracker detector proposed for the the beam test: (a) cross-section in ϕ, and (b) cross-section in θ.

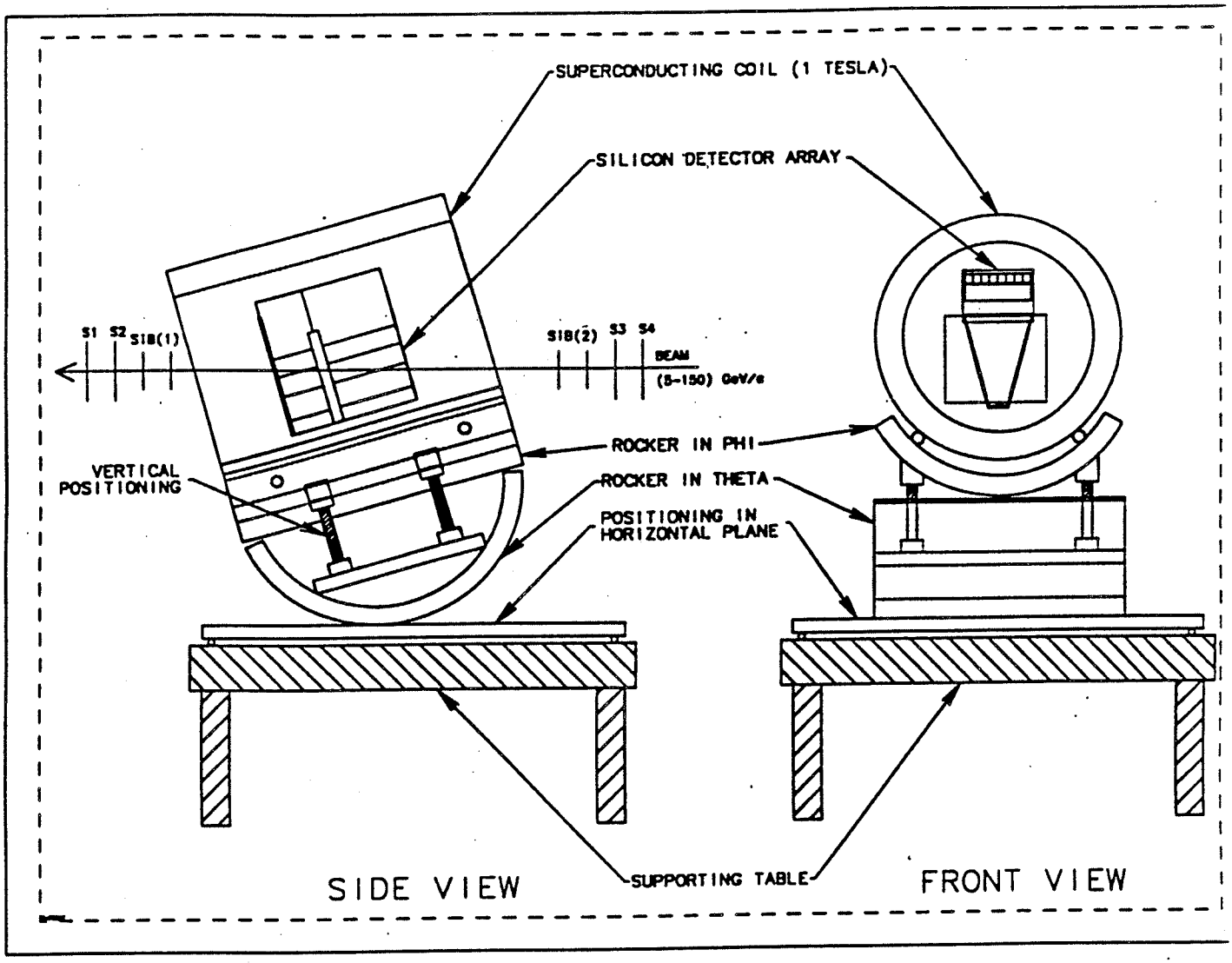

Figure 9.6: A conceptual view of the silicon tracker test-beam arrangement.

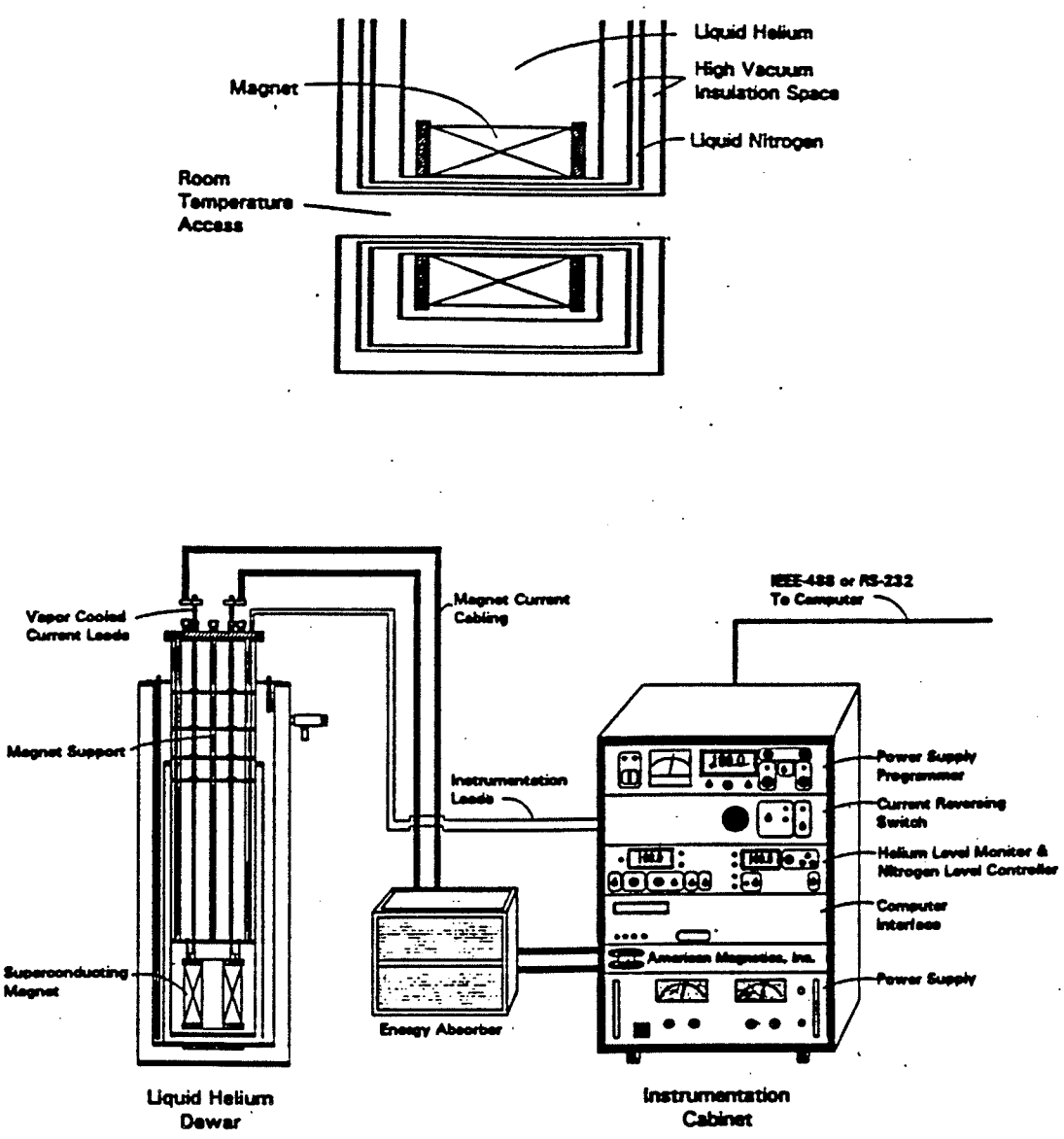

Figure 9.7: The 1 T superconducting coil for the silicon tracker beam test and the associated superconducting magnet system.

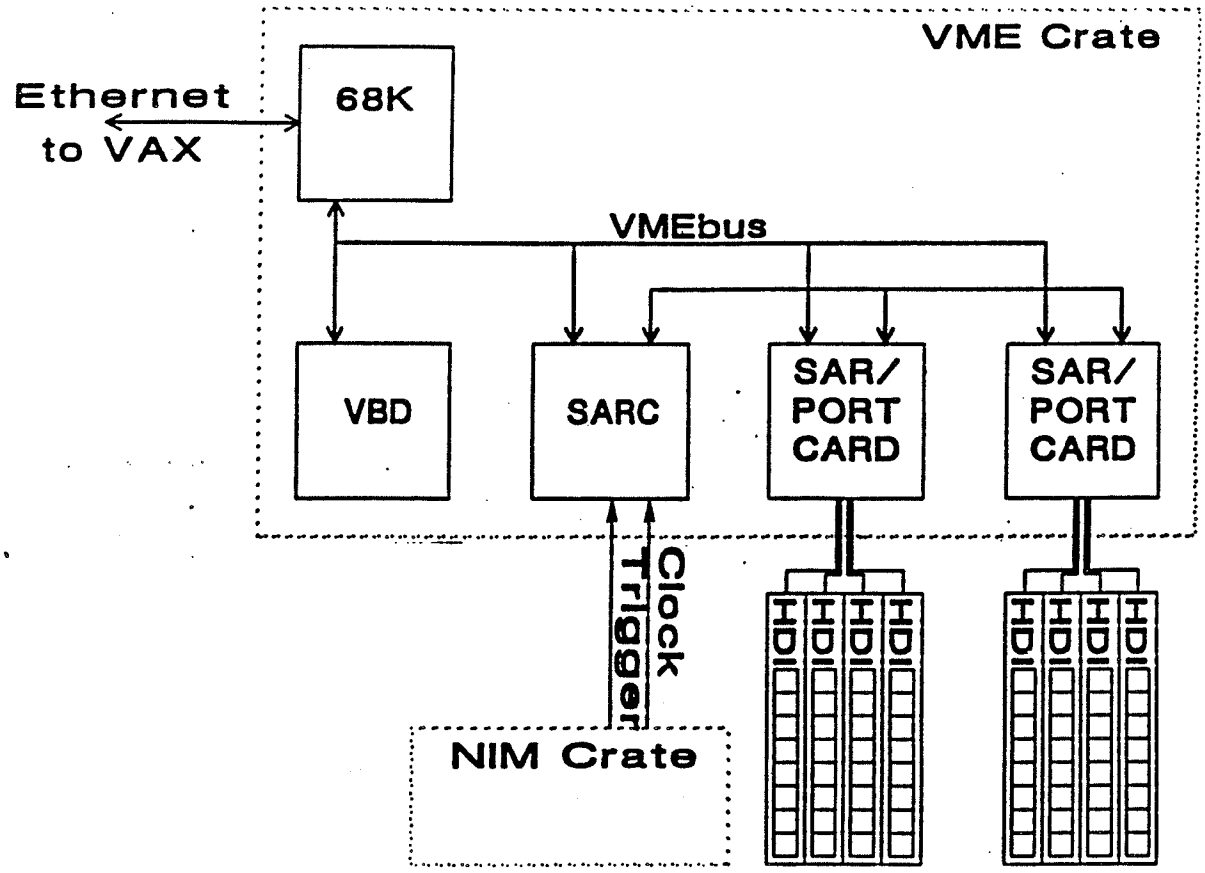

Figure 9.8: A layout of the proposed readout electronics and data acquisition system.

9.3.3 Readout Electronics

A block diagram of the readout electronics is shown in Fig. 9.8. We assume that standard DØ readout electronics will be used in the test-beam. It will consist of one VME crate housing two SAR/PORT cards, a SARC controller card, and a VBD card. Each of the SAR/PORT cards will read data from four HDI's with each HDI supporting eight SVX-II chips. This arrangement will provide 8192 readout channels.

The CLOCK and the TRIGGER signal for the beam will be derived from NIM logic and will directly access the SARC controller. The data will be transfered via Ethernet to a VAX with a 68K processor.

9.3.4 Controls

The Silicon Tracker test-beam setup will be equipped with standard controls of:

- Detector electronics cooling system,

TEST SILICON ARRAY SELECTION	MAGNET SPECIFICATIONS			PRICE (k$)
	LENGTH (cm)	WARM BORE DIA. (cm)	FIELD (T)	
1 Wedge + 4 Layers from attached Ladder	30	15	1	40
Silicon Array as above and 1 Layer of Fibers	30	24	1	50

Table 9.1: Magnet specifications and price.

- Detector HV system,
- Readout electronics LV, calibration, monitoring, and debugging utilities.

9.4 Test-Beam Location and Schedule

The NWA enclosure in the NW beamline at Fermilab is proposed as the primary location for the Silicon Tracker beam test. This beamline features identified electron and pion beams with momenta in the range $5 - 150\,\mathrm{GeV}/c$.

The South end of the NWA enclosure was traditionally used for testing tracking chambers in preparation to Run Ia. The central part of NWA is occupied by the DØ Test Cryostat. We would like to use the space in the South end of NWA (in front of the DØ Test Cryostat) for installation of the D0 Silicon Tracker test-beam setup.

The next Fixed Target Run at Fermilab is scheduled to start in Fall 1995. We anticipate that by Summer 1995 the Silicon detectors will be available in the quantities necessary to instrument the proposed Test Arrays. The Silicon readout electronics is expected to be tested in Fall/Winter 1994. Consequently, a full data acquisition system (hardware + software) will be available for the test-beam in 1995. The test-beams available at other laboratories are listed in Appendix 1.

9.5 Preliminary Cost Estimate

We assume that the silicon detectors and readout electronics should not be included in the test-beam cost estimate as they will be reused in the DØ Silicon Tracker. Consequently, the projected material cost is limited to the magnet and the turn-table.

9.5.1 Magnet

The information in Table 9.1 is based on preliminary discussions with American Magnetics, Inc.. The quoted price includes: magnet, cryostat, power supply and cryogenic controls.

COMPONENT	PRICE (k$)
Motors/Controllers/Gear boxes ×4	12
Controls	8
Vertical Position Drive	4
Rocker in Phi	1
Rocker in Theta	1
Horizontal positioning table	1
Miscellaneous	3
Total	30

Table 9.2: Prices of major turn-table components, and total.

9.5.2 Test-Beam Turn-Table

We assume an overall 1 ton weight for the magnet and Silicon Tracker Test Array. The positioning precision will be in the range of ± 0.25 mm. The major components of the turn-table are listed in Table 9.2.

The design, fabrication, and assembly of the turn-table, as well as programming of the controls, will be provided by the DØ Mechanical Department.

9.5.3 Total Cost

Assuming the larger version of the magnet (Table 9.1), the projected material cost (excluding Detectors and Electronics) of the DØ Silicon Tracking Detector beam test is expected to be about $80k.

Appendix 1: Test-Beams at Other Sites

Test-beams available outside Fermilab are listed below together with the respective contact people.

1. **BNL** (Alan Carroll)

   Test-beam is booked solid with 20 Institutions, but they promise to "squeeze" DØ into the test-beam area.

2. **SLAC** (David Fryberger)

   SLAC plans beam modifications for 1994 and part of 1995, so no beam running at least through first half FY 1995. SLAC developed recently the capability for a test-beam in the ESA line and plans to develop a test-beam area for the C (FFTB) line. SLAC is interested in helping DØ.

3. **CEBAF** (Roy Whitney)

   Extremely interested, but beams not ready until late 1994 or beginning 1995. Would allow us to make our test in the first available beam.

4. **LAMPF** (Earl Hoffman)

   Very interested to help. The beam energy up to 0.5 GeV. The program for beam runs is not known at this time and so no procedures for beam requests.

5. **TRIUMF** (Jean-Michel Poutissou)

   Very interested to help us, offered technical support. Maximum beam energy 0.3 GeV. Need to apply for beam time. Committee meets twice a year.

6. **KEK** (Takayoshi Ohshima)

   Current KEK policy allows outside users to run experiments at KEK but collaboration with a Japanese Institution (and/or individuals) is strongly recommended. KEK runs all year round. The beam time allocation is considered every 3 month for no more than 3 weeks of running time.

Bibliography

[1] E.Belau *et al.*, Nucl. Instr. & Meth. 214 (1983), 253.

[2] Y. Unno *et al.*, KEK Preprint 93-127.

[3] R.Brenner *et al.*, Nucl. Instr. & Meth. A326 (1993), 189.

Chapter 10

Schedule and Costs

10.1 Schedule

The DØ silicon tracker has an order of magnitude more channels than any previous silicon detector. It is also an order of magnitude smaller than proposed LHC detectors. The construction of these detectors will be a major challenge. This section describes our understanding of the R&D and construction schedules and resources needed for the DØ silicon tracker. The current Fermilab schedule shows Run II beginning in 1998. We hope to have the detector installed and tested at least three months before the beginning of the run.

We have used Macproject to model the R&D and manufacturing process. Where possible previous CDF experience is used to predict the time necessary for each step. Estimates of the manpower necessary are also based on CDF experience. We have tried to be conservative in these estimates. Our schedule assumes availability of the Fermilab silicon facility equipment on a two shift basis. It also assumes a substantial contribution to the module testing by university groups.

10.1.1 R&D Schedule

Figure 10.2 shows our best estimate of the tasks needed to complete the R&D phase of the project. By its nature R&D is difficult to schedule and these estimates should be viewed with caution. However in many cases the detailed designs are now complete and only preproduction models are necessary to complete R&D. There are areas, such as the external cabling design, which are less well developed and have larger uncertainties.

The R&D project is broken into several subprojects:

- Mechanical Design (Fermilab)
  - Utilities
  - External Support
  - Disks
  - Ladders
  - Bulkheads and cable routing

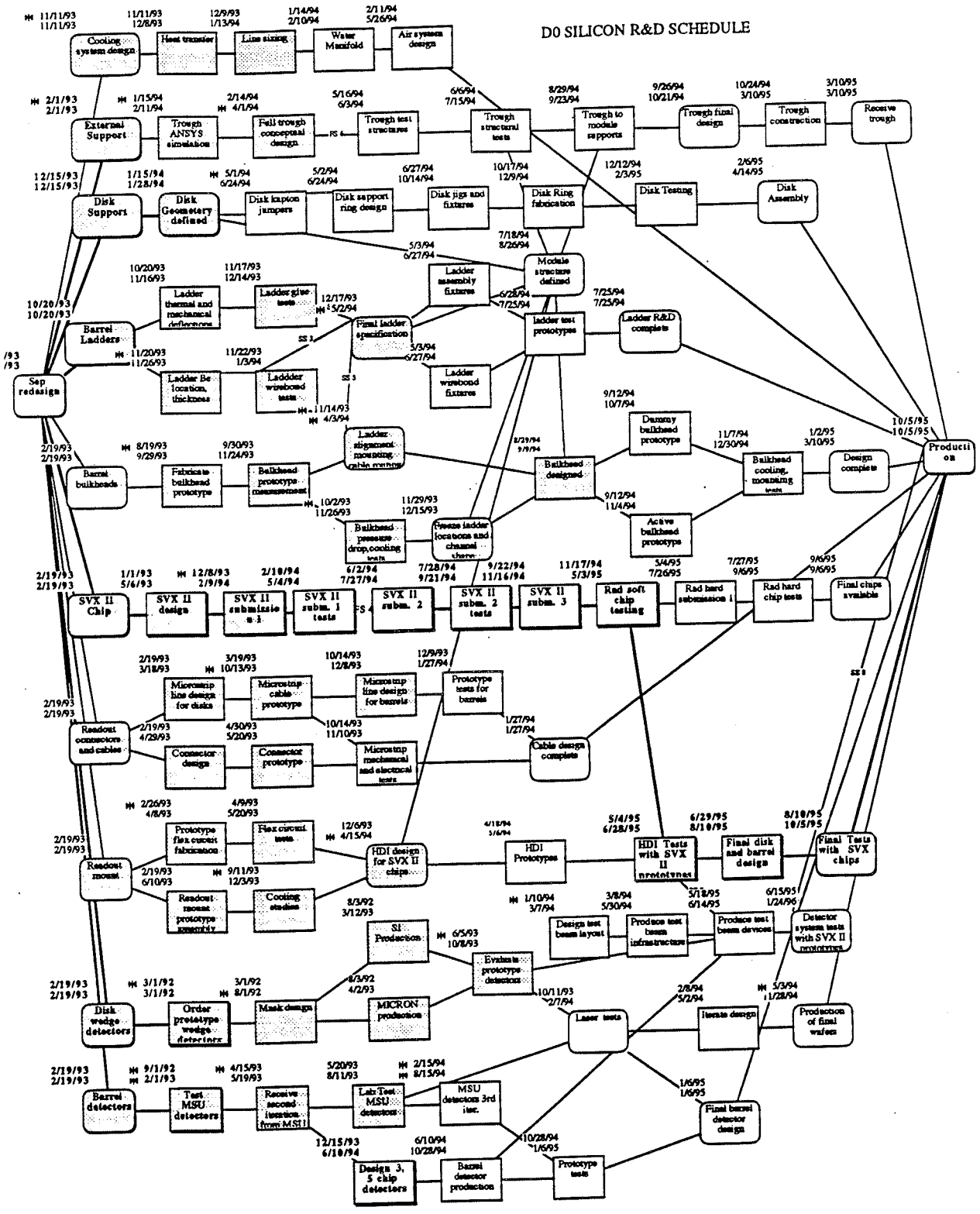

Figure 10.1: Tasks needed for completion of R&D phase

- SVX-II (Fermilab/LBL)
- Readout HDI and cables (LBL)
- Readout (Fermilab)
- Detectors and testing (UC Riverside)

Each of these areas is covered in detail in previous chapters of this design report. The various subprojects are, of course, interdependent. For example, the HDI layout and ladder layouts depend on the final dimensions, power consumption, and signal connections of the SVX-II. Essentially all of the subprojects are in the final prototype phase. There will need to be another iteration of the HDI prototype as the SVX pinout changes between iterations.

There are some important near-term milestones. We expect to perform a large scale (> 5000 channel) test of detectors and readout electronics in the fall of this year. This test is dependent on the production of a successful radiation-soft SVX-II chip this summer. The next large-scale system test would come in the DØ test-beam run during the next Fermilab fixed target running period.

An analysis of the R&D schedule shown in Fig. 10.1 shows that the SVX-II is squarely on the critical path. Our current estimate is that two radiation-soft submissions will be necessary before we are ready to produce radiation-hard chips. Each submission involves two months for production and three months for evaluation and for new layouts to be produced. Our current estimate is that the first radiation-hard chips will be available in the summer of 1995.

10.1.2 Detector Production

The production phase is outlined in Table 10.1. Wedge and ladder testing, and HDI construction and testing are all assumed to be done in parallel. Detector testing can begin as soon as wafers arrive from the manufacturer. Since this phase is expected to be very time consuming we hope to begin detector testing this fall, well before we are ready for ladder assembly.

Our time estimates for the production phase are based on wire-bonding and assembly experience from CDF. We assume that the HDI fabrication and testing is done commercially. Ladder and disk assembly will be done at Fermilab. We have used the following estimates for wire-bonding, testing and assembly times:

Wire-bonding hours/IC	0.4
Probe hours/IC	0.5
Assembly hours/ladder	4
Assembly hours/wedge	4

We assume that there are two shifts on the Fermilab wire-bonding machines and that there are two automatic bonders shared by DØ and CDF. The probe testing is expected to be shared by Fermilab, UC Riverside and the University of Oklahoma.

Our current estimates show that we should be able to complete construction by spring of 1998 if the SVX-II is not further delayed. The next generation SVX-III would delay the starting date by at least a year.

Construction Tasks and Schedule

Level	Task	Duration	Start	Finish
	Start Construction	0	6/1/94	6/1/94
1.	Barrel assembly			
1.1.	Receive Barrel wafers	60	9/1/94	10/25/95
1.2.	Probe test ladder detectors	130	9/29/94	10/22/97
1.3.	Manufacture ladder supports	22	6/1/94	11/1/94
1.4.	Mount MCM and wirebond ladde	81	12/14/95	7/4/97
1.5.	Test and Burn in Ladders	65	1/11/96	4/9/97
1.6.	Mount ladders on bulkhead	65	10/17/96	1/14/98
1.7.	Barrel Final tests	65	11/14/96	2/11/98
2.	Front end electronics			
2.1.	Probe test SVX II on wafer	30	6/1/95	12/27/95
2.2.	Receive Interconnect substrate	0	12/1/94	12/1/94
2.3.	Electrical tests of substrates	40	12/1/94	9/6/95
2.4.	Manufacture Multichip modules	12	11/2/95	1/24/96
2.5.	Test and burn-in MCMs	20	11/16/95	4/3/96
3.	Disk assembly			
3.1.	Receive Disk Wafers	52	1/1/95	12/29/95
3.2.	Probe test wedges	84	1/16/95	8/23/96
3.3.	Mount MCM on wedge	16	1/11/96	5/1/96
3.4.	Wirebond wedges	96	1/25/96	11/26/97
3.5.	Wedge Electrical and laser test	32	2/8/96	9/18/96
3.6.	Mount wedge on ring	32	3/21/96	10/30/96
3.7.	Disk final tests	32	5/29/97	1/7/98
4.	Assembly into Spaceframe	44	5/8/97	3/11/98
5.	Plumbing and cooling system	24	9/1/94	2/15/95
6.	Monitoring systems	18	9/1/94	1/5/95
7.	Alignment System	60	9/1/94	10/25/95
8.	External support			
9.	Manufacture support	24	1/1/95	6/16/95
10.	Measure support	8	6/19/95	8/11/95
11.	Assembly into D0	8	3/12/98	5/6/98

Table 10.1: Detector production phase tasks

10.2 Costs

10.2.1 R&D Costs

The tasks and associated operating costs for research and development are shown in Table 10.2. Much of this has already been spent. These include prototypes for the mechanical supports, readout electronics, and two SVX-II submissions.

10.2.2 Production Costs

Table 10.3 summarizes the M&S costs for the DØ silicon tracker. These estimates do not include costs for test-beam work or for a possible silicon Level 1.5 trigger. Where possible the M&S costs are based on budgetary estimates from manufacturers or on CDF experience. Sources for our estimates for the major items are summarized below:

Detectors:	Quotes from MICRON semiconductor and CSEM.
Bulkheads:	CDF experience and discussions with manufacturers.
SVX-II:	Current cost for rad-hard foundry service with 75% yield.
Readout:	Current hardware costs and expected costs for fiber links.
HDI and Cables:	Quotes from IBM and Cal-Flex based on LBL prototype designs.

10.2.3 Manpower

Figure 10.2 shows the Macproject calculation of the manpower profile for technicians for the R&D and construction phases of the project. It is clear that the staffing of the silicon group will have to grow quickly as the construction phase ramps up. Some of the personnel will be provided by the silicon facility (5 technicians, 3 engineers, 3 physicists half CDF and half DØ) but the primary manpower for detector assembly will be provided by DØ, which currently has one technician on the project.

10.2.4 Facilities

Much of the component testing can be done in university facilities. LBL, UC Riverside, and LBL all have substantial test facilities for silicon and electronics. We imagine that the final ladder and disk assembly, which will utilize coordinate measuring machines extensively, will be done at Fermilab.

Fermilab Silicon Facility

The Fermilab silicon facility was organized to provide infrastructure for the construction of the DØ and CDF upgrade silicon systems. The facility provides the specialized equipment and physicists, engineers, and technicians with the knowledge necessary for these ambitious projects. The facility is located in a semi-clean room in Lab D and currently provides:

- 3 Coordinate Measuring Machines

Level		Duration	Start	Finish	
1.	External Support	0	2/1/93	2/1/93	0
1.1.	Trough ANSYS simulation	4	1/15/94	2/11/94	0
1.2.	Full trough conceptual design	1	2/14/94	4/1/94	0
1.3.	Trough test structures	3	5/16/94	6/3/94	5,000.00
1.4.	Trough structural tests	6	6/6/94	7/15/94	1,000.00
1.5.	Module structure defined	6	7/18/94	8/26/94	0
1.6.	Trough to module supports	4	8/29/94	9/23/94	2,000.00
1.7.	Trough final design	4	9/26/94	10/21/94	0
1.8.	Trough construction	20	10/24/94	3/10/95	25,000.00
1.9.	Receive trough	0	3/10/95	3/10/95	0
2.	Disk Support	0	12/15/93	12/15/93	0
2.1.	Disk Geometery defined	2	1/15/94	1/28/94	0
2.2.	Disk kapton jumpers	8	5/1/94	6/24/94	2,000.00
2.3.	Disk support ring design	8	5/2/94	6/24/94	0
2.4.	Disk jigs and fixtures	16	6/27/94	10/14/94	0
2.5.	Disk Ring fabrication	8	10/17/94	12/9/94	2,500.00
2.6.	Disk Testing	8	12/12/94	2/3/95	0
2.7.	Disk Assembly	10	2/6/95	4/14/95	0
3.	Barrel Ladders	0	10/20/93	10/20/93	0
3.1.	Ladder Be location, thickness	1	11/20/93	11/26/93	0
3.2.	Ladder glue tests	4	11/17/93	12/14/93	1,000.00
3.3.	Laddder wirebond tests	5	11/22/93	1/3/94	0
3.4.	Ladder thermal and mechanica	4	10/20/93	11/16/93	0
3.5.	Final ladder specification	0	12/17/93	5/2/94	0
3.6.	Ladder wirebond fixtures	8	5/3/94	6/27/94	10,000.00
3.7.	Ladder assembly fixtures	8	5/3/94	6/27/94	15,000.00
3.8.	ladder test prototypes	4	6/28/94	7/25/94	7,500.00
3.9.	Ladder R&D complete	0	7/25/94	7/25/94	0
4.	Barrel bulkheads	0	2/19/93	2/19/93	0
4.1.	Fabricate bulkhead prototype	6	8/19/93	9/29/93	100
4.2.	Bulkhead prototype measurem	8	9/30/93	11/24/93	0
4.3.	Freeze ladder locations and cha	8	11/29/93	12/15/93	0
4.4.	Ladder alignment mounting cal	6	11/14/93	4/3/94	1,000.00
4.5.	Bulkhead pressure drop,cooling	8	10/2/93	11/26/93	500
4.6.	Bulkhead designed	2	8/29/94	9/9/94	0
4.6.1.	Active bulkhead prototype	8	9/12/94	11/4/94	12,500.00
4.6.2.	Dummy bulkhead prototype	4	9/12/94	10/7/94	2,000.00
4.7.	Bulkhead cooling, mountimg te	8	11/7/94	12/30/94	1,000.00
4.8.	Design complete	10	1/2/95	3/10/95	0
4.	SVX II Chip	0	2/19/93	2/19/93	0
4.1.	SVX II design	18	1/1/93	5/6/93	0
4.2.	SVX II submission 1	8	12/8/93	2/9/94	0
4.3.	SVX II subm. 1 tests	12	2/10/94	5/4/94	0
4.4.	SVX II submission 2	32	2/23/95	10/4/95	20,000.00
4.5.	Rad soft chip testing	24	7/28/94	1/11/95	0
4.6.	Rad hard submission 1	12	1/12/95	4/5/95	250,000.00
4.7.	Rad hard chip tests	6	4/6/95	5/17/95	0
4.8.	Final chips available	0	5/17/95	5/17/95	0
5.	Readout connectors and cables	0	2/19/93	2/19/93	0
5.1.	Microstrip line design for disks	4	2/19/93	3/18/93	0
5.2.	Microstrip cable prototype	8	3/19/93	10/13/93	5,000.00
5.3.	Microstrip mechanical and elec	4	10/14/93	11/10/93	1,000.00
5.4.	Microstrip line design for barrels	8	10/14/93	12/8/93	0
5.5.	Prototype tests for barrels	6	12/9/93	1/27/94	0
5.6.	Connector design	10	2/19/93	4/29/93	0
5.7.	Connector prototype	3	4/30/93	5/20/93	2,500.00
5.8.	Cable design complete	0	1/27/94	1/27/94	0
5.9.	Production	0	6/15/95	6/15/95	25,000.00
6.	Readout mount	0	2/19/93	2/19/93	0
6.1.	Prototype flex circuit fabricatio	6	2/26/93	4/8/93	6,000.00
6.2.	Flex circuit tests	6	4/9/93	5/20/93	0
6.3.	Readout mount prototype asse	16	2/19/93	6/10/93	2,000.00
6.4.	Cooling studies	12	9/11/93	12/3/93	0
6.5.	HDI design for SVX II chips	10	12/6/93	4/15/94	0
6.6.	HDI Prototypes	3	4/18/94	5/6/94	15,000.00
6.7.	HDI Tests with SVX II prototype	8	1/12/95	3/8/95	2,500.00
6.8.	Final Tests with SVX chips	8	4/20/95	6/15/95	0
6.9.	Final disk and barrel design	6.06	3/9/95	4/20/95	0
7.	Disk wedge detectors	0	2/19/93	2/19/93	0
7.1.	Order prototype wedge detect	0	3/1/92	3/1/92	0
7.2.	Mask design	0	3/1/92	8/1/92	0
7.3.	SI Production	32	8/3/92	3/12/93	80,000.00
7.4.	MICRON production	35	8/3/92	4/2/93	50,000.00
7.5.	Evaluate prototype detectors	18	6/5/93	10/8/93	10,000.00
7.6.	Laser tests	16	10/11/93	2/7/94	0
7.7.	Iterate design	12	2/8/94	5/2/94	0
7.8.	Production of final wafers	30	5/3/94	11/28/94	151,000.00
8.	Barrel detectors	0	2/19/93	2/19/93	0
8.1.	Test MSU detectors	8	9/1/92	2/1/93	0
8.2.	Receive second iteration from M	5	4/15/93	5/19/93	0
8.3.	Lab Test MSU detectors	12	5/20/93	8/11/93	0
8.4.	MSU detectors 3rd iter.	0	2/15/94	8/15/94	18,000.00
8.5.	Design 3, 5 chip detectors	24.24	12/15/93	6/10/94	0
8.6.	Barrel detector production	20	6/10/94	10/28/94	240,000.00
8.7.	Prototype tests	10	10/28/94	1/6/95	0
8.8.	Final barrel detector design	0	1/6/95	1/6/95	0
9.	Cooling system design	0	11/11/93	11/11/93	0
9.1.	Heat transfer	4	11/11/93	12/8/93	0
9.2.	Line sizing	4	12/9/93	1/13/94	0
9.3.	Water Manifold	4	1/14/94	2/10/94	1,000.00
9.4.	Air system design	15	2/11/94	5/26/94	2,500.00

Table 10.2: R&D Tasks and Costs

1.1.2	SILICON TRACKING	Unit	#	Unit Cost	M&S TOTAL
1.1.2	SILICON TRACKING				
1.1.2.1	***Engineering & Design***				
1.1.2.1.1	Wafer/Strip	CAD	0	25,000	0
1.1.2.1.2	Readout IC	SUBMISSI	0	20,000	0
1.1.2.1	Total Eng&Design				0
1.1.2.2	***Silicon Disks***				
1.1.2.2.1	F disk	det	144	2,100	302,400
1.1.2.2.1.1	F wedge fab	det	144	400	57,600
1.1.2.2.2	H disk	det	192	600	115,200
1.1.2.2.2.1	H wedge fab	wedge	96	250	24,000
1.1.2.2.3	Spares (20%)				95,040
1.1.2.2.4	Disk support	disk	16	12,500	200,000
1.1.2.2	Total Silicon Disk				794,240
1.1.2.3	***Silicon Barrels***				
1.1.2.3.1	I barrel	det	168	800	134,400
1.1.2.3.2	J barrel	det	168	1,300	218,400
1.1.2.3.3	K barrel	det	336	800	268,800
1.1.2.3.4	L barrel	det	336	1,300	436,800
1.1.2.3.4	Spares (20%)				211,680
1.1.2.3.5	Ladder Fabrication	ldr	504	400	201,600
1.1.2.3.5	Barrel support	brl	7	22,000	154,000
1.1.2.3	Total Silicon Barrel				1,625,680
1.1.2.4	***Readout IC's***				
1.1.2.4.1	Disk F	IC	2304	125	288,000
1.1.2.4.2	Disk H	IC	960	125	120,000
1.1.2.4.3	Barrel I	IC	252	125	31,500
1.1.2.4.4	Barrel J	IC	840	125	105,000
1.1.2.4.5	Barrel K	IC	504	125	63,000
1.1.2.4.6	Barrel L	IC	1680	125	210,000
1.1.2.4.7	Spares	IC	654	125	81,750
1.1.2.4	Total Readout IC's				899,250
1.1.2.5	***Readout System***	assuming 30 crates			
1.1.2.5.1	Detector->PC				
1.1.2.5.1.1	Disk HDI	pc	240	350	84,000
1.1.2.5.1.2	Barrel HDI	pc	504	350	176,400
1.1.2.5.1.3	IBM Cables	pc	186	300	55,800
1.1.2.5.1.4	Matrix card	pc	186	200	37,200
1.1.2.5.1.5	Port Cd Cable	pc	186	280	52,080
1.1.2.5.1.6	Transition card	pc	186	200	37,200
1.1.2.5.1.7	Bias Voltage	pc	186	100	18,600
1.1.2.5.2	Port Card System				
1.1.2.5.2.1	Port Cards	pc	93	4,400	409,200
1.1.2.5.2.2	Backplanes	pc	24	600	14,400
1.1.2.5.2.3	Download Systen	pc	8	2,000	16,000
1.1.2.5.2.4	Controller Card	pc	8	2,000	16,000
1.1.2.5.2.5	Rack (prep)	pc	4	1,000	4,000
1.1.2.5.2.6	Power Supplies	watt	10000	3	30,000
1.1.2.5.3	SAR System				
1.1.2.5.3.1	SAR Cards	pc	93	1,000	93,000
1.1.2.5.3.2	Crates	pc	14	0	0
1.1.2.5.3.3	power supplies	watt	0	3	0
1.1.2.5.3.4	SAR controller	pc	14	1,500	21,000
1.1.2.5.3.5	J3 Back Planes	pc	14	600	8,400
1.1.2.5.3.6	Diagnostic car	pc	14	1,000	14,000
1.1.2.5.3.7	Diag. Computer	pc	14	7,000	98,000
1.1.2.5.3.8	Racks (PREP)	pc	7	1,000	7,000
1.1.2.5.3.9	VSB Connector	pc	14	100	1,400
1.1.2.5.4	Spares	pc			119,368
1.1.2.5	Total Readout system				1,313,048
1.1.2.6	***Exterior Mechanical Support***				0
1.1.2.6.1	Ext Support	unit	1	25,000	25,000
1.1.2.6.2	Utilities	unit	1	50,000	50,000
1.1.2.6	Total Mechanical Support				75,000
	SUBTOTAL DETECTOR				4,707,218
1.1.2.7	***Physicist Manpower***				
1.1.2.7.1	Fermilab physicists				0
1.1.2.7.2	Collaboration physicists				0
1.1.2.7	Total Physicist				0
1.1.2	**TOTAL SILICON TRACKING**				**4,707,218**

Table 10.3: Silicon Tracker Cost Summary

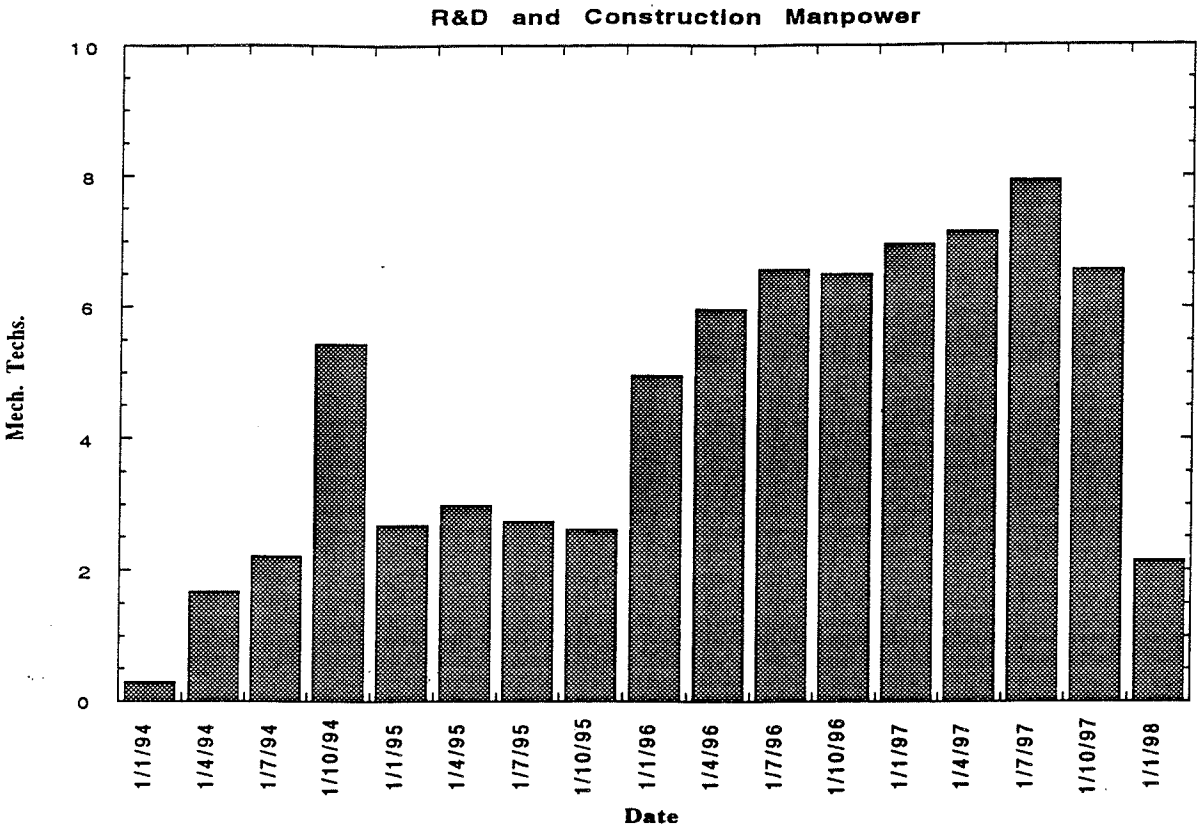

Figure 10.2: Mechanical technician requirements for R&D and construction

- 2 Probe stations
- 2 SVX I readout systems
- 1 Laser test stand
- 1 Automatic wire-bonding machine
- 1 Manual wire-bonding machine
- GPIB test equipment (picoammeters ...)

The manpower associated with the facility includes:

- 4 Physicists (half time)
- 3 Engineers
- 5 Technicians

There is a project underway to expand the clean room space in Lab D. This is expected to take 9 months. The resulting building, including the 3700 ft^2 clean room, is shown in Fig. 10.3.

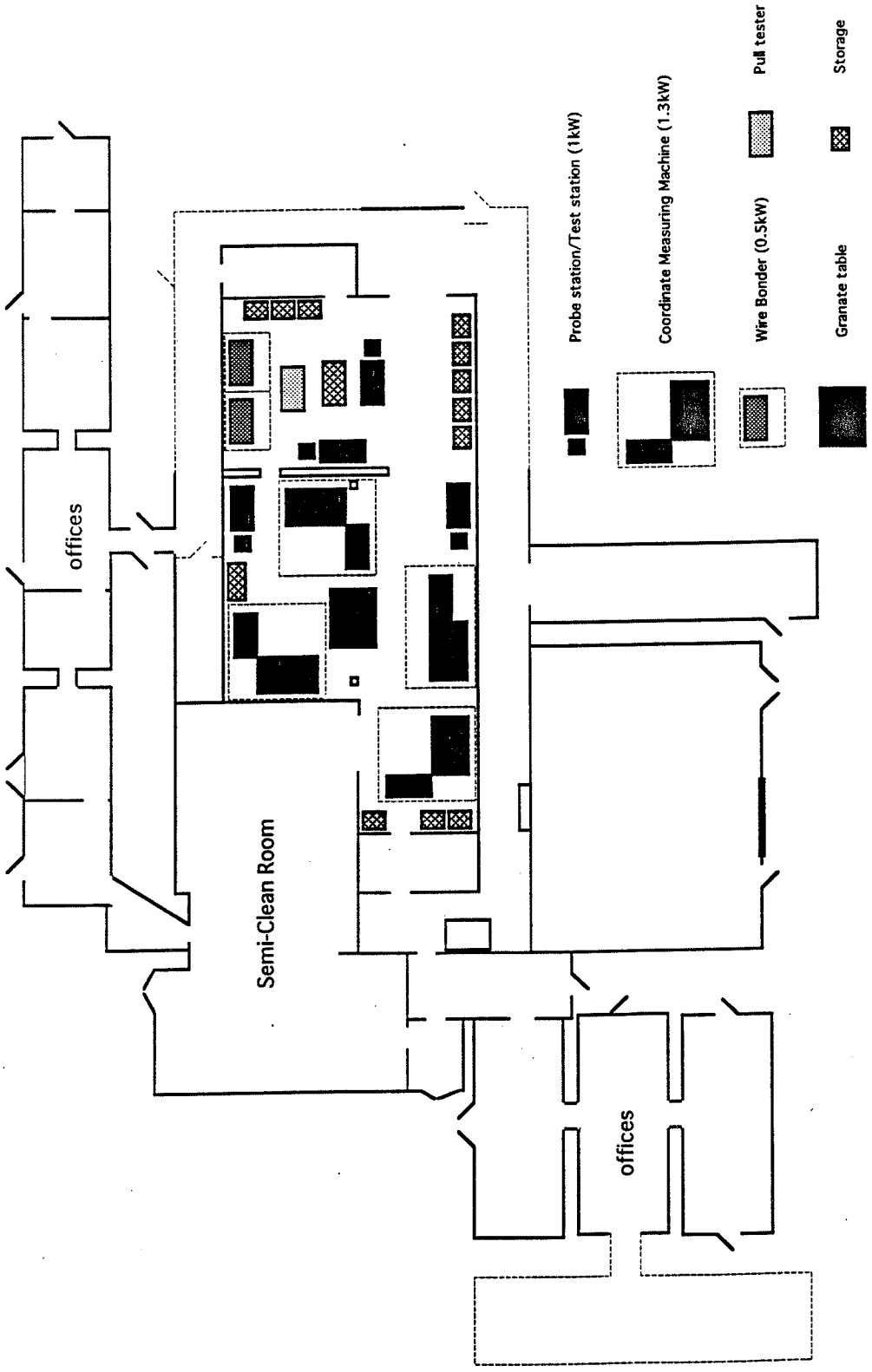

Figure 10.3: Expansion of Lab D clean room space

University Facilities

Both UC Riverside and the University of Oklahoma have existing probe station and clean room facilities. Riverside is coordinating the detector testing and it is expected that Fermilab and the University of Oklahoma will join Riverside in the testing effort. UC Riverside is currently constructing a model test stand which will be duplicated at Oklahoma and Fermilab.