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Test for the mitigation of the Single Event Upset for ASIC in 130 nm technology

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The Micro Vertex Detector (MVD) is the innermost sensitive layer of the $\bar{\text{P}}$ANDA experiment at the new Facility for Antiproton and Ion Research (Fair). The MVD will be composed of two kind of sensors: hybrid pixels and double sided strips. The front end electronics of the MVD will be placed at a few centimetres from the interaction point, where high radiation levels are expected. Therefore the ASIC have to be designed with radiation tolerant techniques, both in terms of Total Ionizing Dose (TID) and Single Event Upset (SEU). The TID issue has been addressed using a sub micron technology as the CMOS 130 nm, which has proven an intrinsic good tolerance to radiation damage. On the other hand these technologies are very sensitive to SEU, due to the reduced size of the active devices. Therefore SEU mitigation techniques have to be applied at circuit level, in order to prevent data corruption and failure of the control logic. Various architectures and techniques are proposed in literature, which essentially show a trade off between protection level and area penalty. Some of these techniques have been implemented in the prototypes for the readout of MVD pixel sensors, based on space constraints. The prototypes have been then tested at the Legnaro INFN facility with ions of various species, in order to asses the effective capability of SEU mitigation. The obtained results have shown some limitation in the implementation of these techniques, which will serve as a guideline for the design of the final ASIC.

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1. Introduction on the detector electronics

The antiProton Annihilation at DArmstadt ($\overline{\text{P}}$ANDA) is a new experiment under development[1], with fixed target layout . It exploits the antiproton beam that will be available at the Facility for Antiproton and Ion Research (Fair).

The Micro Vertex Detector (MVD) is at few centimetres from the interaction point, and it is composed of 4 coaxial barrels, and 6 forward disks. Pixels were chosen for the internal layers to cope with the high event rate, while strips for the external ones to cover large areas [1]. A 100 kGy TID and a 1 MeV equivalent neutron fluence of $1 \cdot 10^{14}$ neutron/cm^2 is expected, in 10 year lifetime with a 50 % duty cycle. The front end electronics allows to acquire information as the position, time and energy of the incoming particle.

The readout electronics for the pixel sensor is a custom project, called Topix, in a 130 nm CMOS technology. The size of the pixel is 100×100 μm^2 and contains the analogue section with the amplifier, and the digital part with registers [2]. The analogue chain foresees a Charge Sensitive Amplifier (CSA), with an input dynamic in the range from 1 fC to 50 fC, and a comparator to discriminate the output with a threshold that can be trimmed individually for each channel.

The GBT chip set is a large project, developed at CERN, for the data transmission. It is envisaged for the next generation experiments, working with a high luminosity beam [3]. The aim is to provide a bidirectional serial link for data acquisition and slow control, which is able to work in a radiation environment. The activity foresees also the development of the electronics on the other end of the optical fibre, typically implemented on an FPGA. The INFN Torino department was involved in the design of the GigaBit Laser Driver (GBLD), to control the laser diodes. This chip set represents the current solution, for the MVD, to send the data towards the counting room.

1.1 The devices under test

Regarding the radiation damage due to neutrons or hadrons, the sensitive section for each Topix cell is the digital one where the memory elements are placed. There is a couple of 12 bit registers to store the leading and trailing edges, which define the TOT. Then there is an 8 bit configuration register for the pixel setting, as the local threshold, the masking and others controls. The device under test was a reduced scale prototype with 640 cell instead of $12.8 \cdot 10^3$ cell, as in the final ASIC [4]. Due to the limited area, the registers are implemented with latches. They are protected against the Single Event Upset (SEU), by the Triple Modular Redundancy (TMR).

In Topix the pixels are organized in columns, with some electronics to store the events before the serialization. The present design foresees 110 column, each one arranging 116 cell. To save room on the layout, the same bus serves two adjacent columns transferring data towards the output FIFO. These end of column structures are made of 32 word, each one 40 bit long. The stored information are the time stamps for the leading and the trailing edges, and the hit pixel address. In this region the SEU protection is implemented by the Hamming code, that allows the detection and correction of one bit error. Since in the present design the selected encoding assures a minimal Hamming distance of 3 between two valid words, a protection failure may only happen when two bit flip together inside the same word.

[1] The first antiproton beam is delivered to the apparatus for testing in the hall from the beginning of 2019.

The GBLD circuit is made in a 130 nm CMOS technology, as well Topix. It is designed for a 4.8 Gbit/s data rate and the capability to drive both VCSEL and EEL diodes, but it is still working well up to 10 Gbit/s. To manage a high capacitive load, a pre emphasis circuit is available. The bias and modulation setting, can be done via an I^2C interface. The configuration is stored in 7 register 8 bit wide implemented with D type flip flops, and the SEU protection is performed by the TMR. Due to power consumption optimization a second versions, Low Power GBLD (LPGBLD), has been specifically designed and tested to drive VCSEL. They differ also for the metal stack: the GBLD used the option with thick metal layers, while the LPGBLD employed the standard layers.

2. The facility and test results

The SEU measurements were performed at the Sirad facility, in the INFN Legnaro Laboratory. Several ions at different energies are available, to test the devices placed in a vacuum chamber. The facility provides also a system for the evaluation of the dosimetry, performed acquiring the flux and the fluence with monitoring diodes.

The measurements were accomplished with ions in a large range, from O at 101 MeV up to Cl at 197 MeV. The device was set in a working state and checked every 2 s, when an error occurs it is counted and the circuit is configured again.

2.1 The results for Topix

From the ratio, between the errors and the incident ions, the frequency of the upset can be evaluated. Normalizing these ones, to the number of bits for the configuration registers in the Topix prototype (5120 bit), the cross section can be estimated. The points are fitted with a Weibull function, that is currently used to model this quantity. For the Topix configuration register, a saturated cross section of about $2 \cdot 10^{-8}$ cm^2/bit is obtained (figure 1). This structure, protected with TMR, becomes sensitive to the upset above a LET of 2 MeV cm^2/mg.

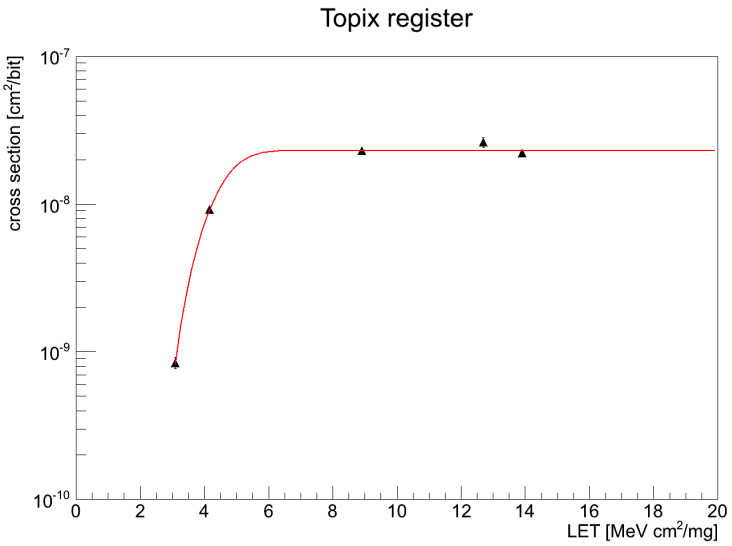

Figure 1: The plot of the SEU cross section as a function of the LET, for the Topix configuration register.

Since the prototype under test contains only 4 columns with output FIFO, the related number of bits to use in the normalization is again 5120 bit. In that case the saturated cross section for the output FIFO buffer, protected with Hamming code, is roughly $7 \cdot 10^{-8}$ cm^2/bit. The threshold, where the upset effect becomes evident, is around a LET of 1 MeV cm^2/mg. The comparison, from Topix configuration register, shows that the TMR protection looks more effective than the Hamming code.

2.2 The results for the GBLD

For the standard GBLD circuit, that is the first version which is able to drive VCSEL and EEL, the total number of bits dedicated to the storing of the configuration is 56. The layout featuring thick metal layers is the same of the final ASIC, and foresees D type flip flop. The measurement for the structure, protected with TMR, shows a saturated cross section of around $4 \cdot 10^{-9}$ cm^2/bit (figure 2). Regarding the threshold, the upset effect starts to arise for a LET of about 2 MeV cm^2/mg.

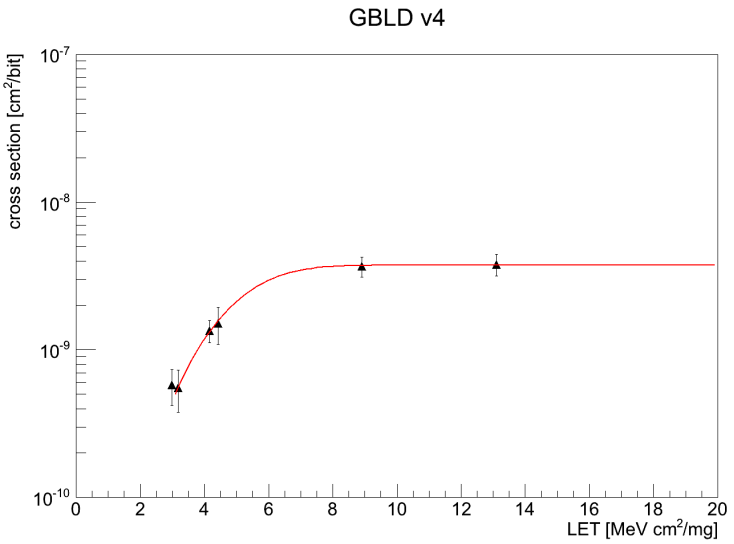

Figure 2: The plot of the SEU cross section as a function of the LET, for the I^{2}C interface of the GBLD.

The LPGBLD, that is the second version, features a low current consumption driving VCSEL only. The circuit has a similar interface composed of 56 bit, but with standard metal layers. The register structure, protected with TMR also in this case, has a saturated cross section of $3 \cdot 10^{-9}$ cm^2/bit. The upset threshold is at a LET of around 2 MeV cm^2/mg, as for the generic GBLD. Even though the circuits comes from different design, the protection systems are very similar and the saturated cross sections are quite comparable.

2.3 Conclusions on the results

The Topix circuit shows a saturated cross section an order of magnitude larger than the GBLD circuit, and that is considered due to the configuration register made of latches instead of standard flip flops. For that reason the new Topix version is going to make use of D type flip flops, to take advantage of the GBLD experience.

For what is concerning the GBLD circuit, the designers evaluated positively the present tests on SEU. Since all others requirements for that project have been successfully assessed, the CERN collaboration has established to proceed toward the full production run.

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References

[1] MVD group. Technical Design Report for the $\overline{\text{P}}$ANDA Micro Vertex Detector. Preprint, Fair, panda-wiki.gsi.de/pub/Mvd/TalkOrPaperDrafts/panda_tdr_mvd.pdf, 2011.

[2] S. Bonacini, D. Calvo, P. De Remigis, T. Kugathasan, G. Mazza, M. Mignone, A. Rivetti, L. Toscano, and R. Wheadon. A CMOS 0.13 μm silicon pixel detector readout ASIC for the $\overline{\text{P}}$ANDA experiment. *Journal of Instrumentation*, 7(c02015), 02 2012.

[3] S. Baron, S. Bonacini, Ö. Çobanoglu, F. Faccio, S. Feger, R. Francisco, P. Gui, J. Li, A. Marchioro, P. Moreira, C. Paillard, and .. . The GBT SerDes ASIC prototype. *Journal of Instrumentation*, 5(c11022), 11 2010.

[4] I. Balossino, D. Calvo, A. Candelori, F. De Mori, P. De Remigis, A. Filippi, S. Marcello, S. Mattiazzo, G. Mazza, M. Mignone, L. Silvestrin, and .. . Single Event Upset tests on the readout electronics for the pixel detectors of the $\overline{\text{P}}$ANDA experiment. *Journal of Instrumentation*, 9(c01042), 2014.