Fermi National Accelerator Laboratory

FERMILAB-Pub-87/187-E
[E-741/CDF]

A Two Level FASTBUS Based Trigger System for CDF*

D. Amidei, M. Campbell, H. Frisch, C. Grosso-Pilcher
J. Hauser, T. Liss, G. Redlinger, A. Roodman
H. Sanders, M. Shochet, J. Ting, Y. D. Tsai
Enrico Fermi Institute
The University of Chicago
5640 S. Ellis Avenue
Chicago, Illinois 60637

M. Dell'Orso, P. Giannetti, L. Ristori
INFN, Pisa
S. Piero a Grado
Pisa, Italy 56010

July-August 1987

*Submitted to Nucl. Instrum. Methods A

A Two Level Fastbus Based Trigger System for CDF

D. Amidei, M. Campbell, H. Frisch, C. Grosso-Pilcher
J. Hauser, T. Liss, G. Redlinger, A. Roodman
H. Sanders, M. Shochet, J. Ting, Y.D. Tsai
Enrico Fermi Institute
The University of Chicago
5640 S. Ellis Avenue
Chicago, IL 60637

M. Dell'Orso, P. Giannetti, L. Ristori
INFN, Pisa
S. Piero a Grado
Pisa, Italy 56010

Abstract

We describe a two level Fastbus based trigger processor designed and built for the CDF detector at the Fermilab $\bar{p}p$ collider. The Level 1 decision is based on the global energy deposition in the calorimeters as well as the presence of muon candidates and stiff tracks in the central drift chamber. The Level 1 decision is made in the 3.5μs between beam crossings, incurring no deadtime while reducing a raw event rate of 50-75 kHz to a few kHz. The remaining events are passed on to Level 2. The Level 2 decision is driven by the topology of the event, operating on calorimeter clusters, central stiff tracks and muon candidates. Level 2 is designed to reduce the rate to 1-100 Hz, incurring less than 10% deadtime, before initiating readout of all the detector elements. A large fraction of the trigger hardware is used for both the Level 1 and Level 2 decisions.

I. Introduction

The CDF detector at Fermilab[1] has been built to study the physics resulting from $\bar{p}p$ interactions at a center of mass energy of 2 TeV. The interaction rate at the collider, at the design luminosity of 10^{30} cm^{-2} s^{-1}, is expected to be 50-75 kHz, with

a typical minimum bias multiplicity of 50 or more particles. We have built a sophisticated trigger processor the function of which is to sift through the complex event structure, picking out only events of particular interest. The rate of data taking is limited primarily by two factors: the rate at which events can be written to tape, and the rate at which physicists can analyze the data. The first of these factors limits the data taking rate at CDF to about 1 Hz. This coincides nicely, given the projected computing power, with the rate at which data can be analyzed. Thus, it is the formidable task of the trigger system to choose 1 out of every 50 to 75 thousand events to be written to tape.

The CDF trigger consists of three levels. The first two, with which we will be concerned in this paper, consist of specially designed hardware which make the decision to initiate the full detector readout. Level 3 consists of a software processor farm, and is discussed elsewhere[2].

The goal in designing the trigger for CDF is threefold. First, we must be capable of triggering on the signatures of known physics. This includes such things as $Z^0 \rightarrow \mu^+\mu^-$ or e^+e^-, $W \rightarrow e\nu$ or $\mu\nu$, jets, etc. Secondly, the trigger should be flexible enough to encompass signatures of as yet unknown physics - things which may become interesting, for a variety of reasons, during the lifetime of the experiment. Finally, the various strengths of the detector itself should be exploited to the fullest extent possible in the trigger electronics. For CDF these strengths are a finely segmented, projective electromagnetic and hadronic calorimeter, excellent tracking, and a strong magnetic field. The segmentation of the calorimeters is preserved at the trigger level, and information regarding high P_t particles (stiff tracks) and muon candidates is incorporated at both Level 1 and Level 2. These features allow a trigger decision to be based on the topology of transverse energy flow and on the identification of electrons, muons and jets in the event.

II. Overview

The idea behind the multi-level trigger structure is to introduce as little bias as possible at the lower levels, with the goal of reducing the rate to a point where the next level can do a more sophisticated analysis without incurring significant deadtime. The most time consuming process in data taking at CDF is the readout of the detector components by the data acquisition system, which is projected to take of

order 1ms. Readout of the detector begins after a Level 2 trigger has been satisfied, which must happen at a rate of 100 Hz or less if the deadtime due to readout is to be kept below 10%.

The trigger is built on a large number of different Fastbus cards, each of which will be described below. The digital logic used on these cards is almost entirely ECL, both for reasons of speed and for compatibility with the ECL Fastbus backplane. Fastbus data transfers are used in the setup and intitialization of the trigger system (i.e. for downloading trigger constants and setting control bits), for testing, and during readout. The operation of the trigger under run conditions, however, is almost completely independent of Fastbus. We will not go into details concerning Fastbus interfaces in this paper, since they are peripheral to the trigger decision making and have been discussed elsewhere[3]. All trigger components, unless otherwise noted, are Fastbus slaves.

The Level 1 decision is made in the 3.5μs between beam crossings (assuming six bunch accelerator operation) and it therefore incurs no deadtime. At the time the Level 1 decision must be made, the trigger system has accumulated information regarding only the global features of calorimeter energy deposition: no information regarding energy flow in the detector is known at this time. Specifically, the Level 1 decision is based on the following information (note that other information may be easily added to this list - see section Vb):

1. Electromagnetic, hadronic and total transverse energy (E_t), summed over those calorimeter elements which are above programmable thresholds.

2. The transverse energy imbalance in the electromagnetic and hadronic calorimeters, given by $E_t\cos\phi$ and $E_t\sin\phi$ summed over those calorimeter elements which are above programmable thresholds, where $E_t\cos\phi$ and $E_t\sin\phi$ are essentially the x and y components of transverse momentum as measured by the calorimeters.

3. The existence of stiff tracks in the central tracking chamber (but not their directions) and the existence of muon candidates in the central and forward muon chambers (but not their positions).

4. Presence of a beam-beam interaction and/or the presence of a beam-gas interaction.

5. Hits in the small angle silicon counters in combination with hits in the beam-beam counters (diffractive and elastic events).

Level 1 delivers a rate of a few kHz to the next level. At Level 2 a deadtime of about 5%-10% is allowed. This gives Level 2 approximately 10μs to make a decision (for a small fraction of particularly interesting events, a longer decision time may be allowed). In this time it is possible to determine topological features of the transverse energy deposition, such as clustering of energy in the calorimeters, and to perform simple calculations, such as finding the invariant mass of a group of clusters. It is also possible to associate stiff tracks with calorimeter clusters and therefore to do a first order electron-π^0-jet discrimination. Level 2 is driven by the clustering of energy in the detector: a list of the cluster properties, including position, width, and transverse energy is compiled. This list is passed to a set of programmable processors that make a decision based on the information in the list. These processors are easily expandable in the sense that new types of calculations may be added to the processors as the need and desire arise.

The parameters upon which the Level 2 decision is based are the following:

1. Number of energy clusters in the detector and their properties, corresponding to both electromagnetic and total energy deposition: E_t, $E_t\sin\phi$, $E_t\cos\phi$, mean pseudo-rapidity ($<\eta>$), rms width in pseudo-rapidity (σ_η), mean azimuth ($<\phi>$), and rms width in azimuth (σ_ϕ), as well as the presence of high P_t tracks pointing at these clusters.

2. The presence and position of track segments in the muon chambers that are associated with high P_t tracks in the central tracking chamber.

3. Transverse energy summed over the detector as a whole and transverse energy imbalance in the detector.

4. Presence of a beam-beam interaction and/or the presence of a beam-gas interaction.

We now proceed with the details of the CDF trigger. In section III we describe the circuitry involved in the Level 1 decision. This will of necessity include many items that are also relevant to the Level 2 decision; their placement in section III is not meant to imply specificity to Level 1. In section IV we cover the Level 2 decision, with emphasis on those parts of the electronics that are used solely during Level 2. Finally, in section V we describe the final decision logic, including a description of the relationship between the trigger system and the data acquisition system. Partitioning, i.e. the ability to split the detector into several, independent, co-running sub-systems, will be briefly described here.

III. Level 1

Signal processing in the CDF trigger system is built around a scheme that, in the interest of speed, uses analog signals to form sums and moments before digitizing. This analog processing is done in ten Fastbus crates. These analog crates map onto the calorimeter in a one to one fashion, as shown in Figure 1. Each crate can be identified by the type of calorimeter signals it receives and the geographical location on the detector from which they come. Separate crates, hereafter referred to as electromagnetic and hadronic crates, receive signals from the electromagnetic and hadronic calorimeters respectively.

The final Level 1 trigger decision is made using a look-up table stored in a 4K RAM. This is described in section V. In this section, we describe the processing that is done to produce the inputs to this look-up table.

Our description of the trigger system focuses on the functions of the individual boards, beginning with the board responsible for overall synchronization and control of the system.

a) Trigger system synchronization - the Timing Control Operation of the trigger system depends critically on the timing of both the collider and the rest of the CDF detector. The overall synchronization of the trigger system with the rest of the detector, as well as synchronization of the components of the trigger system with each other, is established by the Timing Control. The Timing Control, in turn, gets its reference from the Master Clock[2]. As its name suggests, the Timing Control sends out programmable timing and control information to all other parts of the trigger system during the generation of a trigger.

The Timing Control consists of two types of boards, a master and any number of slaves. The Timing Control Master is a 50 Mhz programmable sequencer, and the Timing Control Slaves generate the timing signals which control the rest of the trigger while receiving status information from a variety of other trigger modules.

The Timing Control Master generates the address of the current instruction which is then bussed to the Timing Control Slaves. The address is used in the Master to select a location from a 16K by 64 bit memory. Twelve bits of this memory are used to specify the dwell time of the current instruction. Remaining bits specify the next address for jump instructions, the sequencer's instruction, and select a status bit from one of the slaves for use in branch conditions.

The Slaves each have 16K by 32 bit memories which contain the strobe information. The address for the memory comes from the Timing Control Master. Each slave can receive up to eight status bits back from the modules they control, which can then be multiplexed to the Master and used for conditional jumps.

In addition to the timing and control signals, the Timing Control is responsible for a variety of other trigger functions. These include storing threshold values which must be loaded serially, one threshold every 80-100 ns, into the analog front end of the trigger (see below), and during Level 2, the assembly of a 64 bit word of cluster information which is used by the Level 2 Processors (see section IVc).

b) The calorimeter trigger.

1) Trigger cables and the Tubesum Front end electronics (RABBIT electronics[4]), consisting of charge integrating amplifiers, are located on the the detector in the collision hall. Differential analog signals are sent upstairs to the trigger counting room via 200 ft. lengths of specially designed cable. The signals from the RABBIT electronics are series terminated at the detector end in 49.9Ω resistors for both wires of a pair. This configuration is chosen to produce the best possible settling time of signals at the trigger end of the cable in accordance with the design of the cable. Approximately 60 dB of common mode noise rejection for signals of frequencies up to 20 kHz is achieved with this design.

Two different varieties of the cable exist, one for the scintillator based calorimeters, which are viewed by photomultiplier tubes, and one for the gas proportional chamber calorimeters. The cables from the scintillator calorimeters, covering the central region from η=-1.0 to η=+1.0, consist of four shielded twisted pairs with a drain wire having electrical contact with the shield. The four shields are mylar-aluminum laminated and are insulated from each other. The insulation on

individual wires is foamed polypropylene. The four shielded twisted pairs are themselves shielded with aluminized mylar with a drain wire. The outer shield is wired to the ground at both the detector and trigger ends, while the individual twisted pair shields are connected to ground only at the detector end. These inner layers act as a Faraday shield, while the outer shield relates the grounds of the signals at each end. The cable has an impedence of 100Ω and a capacitance of 12.5 pf/ft. The propagation velocity is 0.78c.

The central calorimeter consists of projective towers of 15° width in ϕ and a width of .1 in pseudo-rapidity, η. Each of these towers is viewed by two photomultipliers. This projective geometry is preserved in the trigger, but to reduce the number of signals, four photomultiplier signals are summed together to produce logical trigger towers with a width of 0.2 in η and 15° in ϕ. This summation is done on a Fastbus card called the Tubesum where sets of four analog inputs are summed in high input impedence operational amplifiers. The output impedence of the op-amps is matched to the output cable using 0.1% resistors. The speed and settling time of the summing circuit are much faster than that of the input signal. The Tubesum cards as presently implemented have no intelligence, taking just 15V power from the Fastbus crate. We have left room to make, if necessary in the future, an intelligent Tubesum card where such things as a comparison of the pulse heights between two tubes can be made in order to compensate for non-uniformities in the response of the calorimeters.

The signals reaching the trigger system at the end of the 200 ft. cables have a risetime of approximately 500ns (10%-90%). About 2μs after a beam-beam interaction signals at the trigger end of the cables have settled to within 1% of their final values. These signals have a long decay time which allows them to be considered as essentially DC. The gain of the front end electronics has been adjusted so that, for central calorimeters, a 100 GeV energy deposition in the center of a tower gives -1V out of the Tubesum.

The gas calorimeters, which have finer azimuthal segmentation, are also summed into logical trigger towers of $\Delta\phi$=15° and $\Delta\eta$=0.2. In this case, however, the summation is done at the detector on the front end amplifier cards. After summation into trigger towers, the signals are sent to the trigger counting room via cables similar to those used for the central calorimeters, but with just one twisted pair per cable. Gas gains are adjusted such that a 50 GeV <u>transverse</u> energy deposition produces -1V at the trigger. The discrepancy between central and gas calorimeter gains is compensated for in the trigger system. This compensation is performed in the Receive

and Weight (RAW) cards which form one of the major components of the analog front end of the trigger system.

2) Receive and Weight The RAW board is the entry point into the processing electronics of the CDF trigger. Signals from the central calorimeters are relayed from the Tubesum to RAW over cables of the same construction as before. Signals from the gas calorimeters go directly from the detector into RAW.

The RAW cards are distributed among the ten analog Fastbus crates of the trigger system which they share with the Compare and Sum (CAS) and Crate Sum cards (see sections IIIb.3 and IIIb.4). Each RAW card contains 24 channels, from a single $\Delta\eta$=0.2 slice of either electromagnetic or hadronic calorimeter. The 24 channels correspond to the 24 different ϕ values for a given η slice. The calorimeter signals are received in RAW by a high input impedence, balanced, differential amplifier with a gain of minus three. The output of this amplifier is input to a dual multiplying DAC with output

$$V_{out} = 0.5[(V_{in} \times W)/256 + (0.5 \times B)/256],$$

where W is a weighting factor between 0 and 255, and B is a bias between 0 and 255. The weighting factor accomodates gain variations and generates the $\sin\theta$ factor needed for converting E to E_t for the central calorimeters. The adjustable bias is used to compensate for calorimeter amplifier pedestals. It is at this stage that the compensation for the gas gain is made by reducing the weight W by a factor of two. The output of the dual multiplying DAC is fed into a non-inverting amplifier with a gain of four. and then to an emitter-follower. The output of the final RAW amplifier stage is then relayed across a short jumper to the RAW companion card, CAS. The DAC bias constant, 0.5V, can be changed so that with W=0 the bias can be used as a source of simulated inputs for trigger testing.

The RAW board has an 8 bit high speed DAC that can be controlled either by Fastbus or by the Crate Sum. The output of the fast DAC is a differential current which is sent to CAS where it is converted to a voltage and used as the reference in the comparators (see section IIIb.3). RAW also contains correction circuits to maintain linearity and full scale range for the fast DAC.

The digital section of the RAW card includes the Fastbus protocol for both RAW and CAS, shadow memory that holds the digital input values for the multiplying DACs (W & B). and registers for CAS control.

3) Compare and Sum Each CAS card has 24 channels in a one to one correspondence to the 24 channels on the companion RAW card. During the Level 1 cycle, the function of the CAS card is to sum all towers from a single RAW card that are above a programmable threshold. CAS does not have Fastbus protocol, only connections to the Fastbus address and data lines (AD lines). All controlling strobes are generated on RAW. If the cable connecting a RAW/CAS pair is removed, CAS goes to a quiescent state with all signals removed from the AD lines.

Each analog signal from RAW is delivered to a set of analog switches, and to the positive input of a comparator. The other input to the comparator is the reference voltage produced by the fast DAC on RAW. When a particular analog signal is over threshold, the corresponding comparator output is loaded into a "sum register". The state of this register controls the analog switch matrix, directing the tower signals into summing amplifiers. Three different sums are performed for those towers above threshold, a linear sum, a sum weighted by $\sin\phi$, and a sum weighted by $\cos\phi$. It takes approximately 500ns for the analog sum signals to settle to 0.1% accuracy. At Level 1 time, these sums are performed to an accuracy of about 1% (determined by the settling time of the signals from the front end electronics). There are four sets of sum circuits on each channel of CAS, so that four different tower thresholds may be loaded in parallel (at Level 2 time, this parallelism facilitates high speed operation).

Each of the twelve sum circuits is monitored by a zero detection circuit. The outputs of the twelve zero detection circuits are available as a Fastbus register. There are also twelve eight bit DACs, one per sum circuit. The output of the DAC is used as a bias for the corresponding sum circuit. These devices allow for correction of input offset bias by ramping the offset DAC and monitoring the state of the zero crossing comparator.

A block diagram outlining the various functions of the RAW and CAS cards is shown in Figure 2.

A register known as the "inclusion register" is used as a mask to either inhibit, allow, or force participation of specific towers in the summation. This register has one bit for each of the 24 analog channels. If the inclusion register is enabled, then only those channels whose inclusion register bit is set to one will be permitted to activate a comparator. If inclusion register negation is in effect, the converse is true. This function allows masking of bad channels in the calorimeters or in the trigger. The inclusion register can also be loaded into a sum register thereby forcing a channel to be summed.

The output of any CAS register can be gated onto the Fastbus AD lines under the control of the Fastbus protocol circuits located on RAW. In addition, the four sum registers, the inclusion register and the Cluster Finder bus can all be loaded via Fastbus. We will reserve discussion of the Cluster Finder bus until the description of Level 2 below (see section IVa.1).

4) Crate Sum The transition between the analog portion of the trigger and the digital portion takes place in the Crate Sum. In each analog crate there is one set of Crate Sum boards which receive the analog sums E_t, $E_t\sin\phi$ and $E_t\cos\phi$ from each CAS board, and perform a further stage of analog summing to produce complete sums at the crate level. In addition to these sums, the Crate Sum uses hardwired weighting factors corresponding to the mean pseudo-rapidity, η, of each CAS card to produce the sums $E_t\eta$ and $E_t\eta^2$. The pseudo-rapidity weighted sums are used only during Level 2. Each analog sum is digitized in an 8-bit flash ADC (FADC) and sent, for Level 1, to the Level 1 Sum board. There are four sets of identical analog summing circuits in the Crate Sum, corresponding to the four sets of summing circuits on each CAS card.

The analog section of the Crate Sum is contained on two boards. The first board uses high speed summing operational amplifier circuitry to produce the four $E_t\sin\phi$ and $E_t\cos\phi$ sums from the analog signals coming from the ten CAS boards in the crate. Each of these sums is then digitized in a FADC upon command from the Timing Control board. The second analog Crate Sum board uses the E_t signals from the CAS boards to produce the E_t, $E_t(\eta-\eta_0)$, and $E_t(\eta-\eta_0)^2$ sums, where η_0 is the mean rapidity in that crate. The sums about the mean are taken in order to optimize the resolution of the FADCs. The 120 analog input signals which come from the CAS cards to the Crate Sum are contained in a specially designed fourteen layer auxiliary backplane. The digital output from the four sets of sum circuits passes through a multiplexer, with the selected set passing to the digital Crate Sum board.

The digital board receives one set of E_t, $E_t\sin\phi$, $E_t\cos\phi$, $E_t(\eta-\eta_0)$ and $E_t(\eta-\eta_0)^2$ sums. It performs the digital arithmetic necessary to produce twos-complement values of E_t, $E_t\sin\phi$, $E_t\cos\phi$, $E_t\eta$, and $E_t\eta^2$. This board also produces N, the number of calorimeter towers which are part of a Level 2 cluster. The Fastbus protocol and all of the registers for the Crate Sum reside on this board. Finally, all RAW, CAS, and Crate Sum control signals which come from the Timing Control, pass through the digital Crate Sum board. Control signals for the RAW/CAS pairs are shipped out on the special backplane.

5) Interceptor board The Interceptor board is an intelligent patch panel that intercepts the Crate Sum output on its way to the Level 1 Sum (during Level 1) and

the Listmaker (during Level 2). Each Interceptor board receives sets of signals from two Crate Sums, one hadronic and one electromagnetic. The data are recorded in a RAM and then re-arranged into the groups of signals required by the Level 1 Sum and the Listmaker boards.

The main function of this board, aside from acting as a patch panel, is to aid in the testing and debugging of the trigger system. By recording the Crate Sum output in a RAM, it holds information that would otherwise be lost before readout. In addition, by storing the Crate Sum outputs for an entire event, an event can be "played back" at full speed to test all downstream components of the trigger.

6) Level 1 Sum After the digitization by the Crate Sum, the sums from the five electromagnetic crates and five hadronic crates are brought together at the Level 1 Sum board. There is one Level 1 Sum board for each of the quantities summed during Level 1: E_t, $E_t \sin\phi$ and $E_t \cos\phi$. These quantities are received as 10 bit digital values from the Crate Sum. This is done to facilitate a potential future change to 10 bit FADCs on the Crate Sum.

At the front end of the Level 1 Sum board, a strobe from the Timing Control clocks the Crate Sum values into a set of multiplexer/latches. A second set of inputs to the mux/latches allows simulated Crate Sum values to be downloaded through Fastbus for testing. The outputs of the mux/latches feed a set of digital adders. Each board creates grand total sums of electromagnetic, hadronic and total (the sum of electromagnetic and hadronic) transverse energy. These grand total sums are compared to programmable thresholds, and a bit is set if the corresponding sum is above threshold. Since there are four sum registers on CAS, each corresponding to a different tower threshold, the Level 1 summation is also done four times, once for each tower threshold. The results of each comparison, and the total energy sums are stored in a RAM where they will stay until the next event flushes them out, or they are overwritten by Fastbus.

The output of the Level 1 Sum board consists of four bits. Each bit is the logical OR of the electromagnetic, hadronic and total energy comparison to threshold corresponding to one of four sum registers on CAS. These four bits are sent to the final decision logic, Fred (see section V), where they are used, in conjunction with other Level 1 information, in the Level 1 decision.

7) A recap of the Level 1 calorimeter trigger In real time, the operation of the Level 1 calorimeter trigger is as follows. At a fixed time after the beam crossing, and after the front end electronics have generated analog levels on the trigger cables, the fast DAC on RAW is loaded with the first tower threshold by the Crate Sum. The

comparators on CAS generate a signal for any tower that is above this threshold. This output signal is then loaded into the first sum register. This causes the first summer to add the energies of all towers over the fast DAC threshold. These sums are passed to the Crate Sum over the analog backplane, and the Crate Sum produces analog sums over the crate corresponding to E_t, $E_t\sin\phi$, and $E_t\cos\phi$ and then digitizes these values in an 8 bit FADC. These digital values are then strobed into and latched by the Level 1 Sum, where global sums over 5 electromagnetic and 5 hadronic crates are made and compared to thresholds.

Once the first sum register is loaded, the Crate Sum is free to load the next threshold into the fast DAC on RAW and the results of the next comparison are loaded into the second sum register. This process is repeated a total of four times, once for each sum register. Note that this process goes on in parallel for the electromagnetic and hadronic calorimeters and further that the operation of RAW and CAS is controlled by the Crate Sum under the supervision of the Timing Control. When the Timing Control is operating the system, no Fastbus transactions involving data registers located on RAW or CAS are allowed.

c) Other Level 1 triggers

Several Level 1 triggers are available that are not associated with the calorimeters. These include the Beam-Beam Counters (BBC), the fast track finders, the muon systems, and the silicon hodoscopes.

1) Beam-Beam Counters The Beam-Beam Counters consist of two planes each with 16 time-of-flight scintillation counters, one to the east and one to the west of the interaction region. The counters are one inch thick and are arranged in four quadrants of four counters each. The dimensions of the four counters in each quadrant are such that each counter covers an approximately equal range in pseudo-rapidity of $\Delta\eta = 0.7$. The BBC system as a whole covers the region $3.2 < |\eta| < 5.9$. Hamamatsu H1949 photomultiplier assemblies, consisting of 2 inch tubes plus bases, are attached at each end of the three larger counters while Hamamatsu R2076 assemblies, consisting of 3/4 inch tubes plus bases are attached at each end of the smallest counters. The smallest, innermost counter sits directly on the Tevatron beam pipe, and the next three counters are placed touching their nearest neighbors. The two planes of scintillator are equidistant from the detector's center with a total distance between the two planes of 1182 cm.

An anode signal and an inverted dynode signal are taken from each BBC phototube. The gains of each of the phototubes are balanced by adjusting the high voltage. Each signal travels upstairs to the counting room along a 200 ft. length of low dispersion RG-213 co-axial cable. The inverted dynodes go directly to a 96 channel LeCroy 1885N Fastbus ADC. The pulse heights recorded in the ADC are used primarily to correct timing information. Each of the anode signals is fed directly into a LeCroy 621 discriminator with the threshold set at a pulse height corresponding to 1/10 of the minimum ionizing peak. The outputs from the two discriminators for each counter are fed both to the stop inputs of a LeCroy 2228A CAMAC TDC, and to the two inputs of a single channel of a LeCroy 624 meantimer. The TDCs are read out by the Fastbus data acquisition system through a Struck STR320 Fastbus CAMAC branch driver, and used in the offline analysis. The signals emerging from the meantimers perform the trigger function of the BBCs. These signals are converted to ECL logic levels and input to a Struck 136 input/output register. The Struck 136 has been custom modified for us to provide two separate gate inputs so that each of the 32 input signals can be latched at two separate times. The first latch gate is timed for incoming beam halo particles, while the second latch gate coincides with the time at which outgoing particles from a beam-beam interaction will penetrate the counters. This allows the tagging of incoming beam halo and outgoing beam-beam particles. The 64 latch bits are read out by the data acquisition system with each trigger. Fast out signals from the latch are combined in a fast logic board to make the logic signals that are used in the trigger: E·W and E·W·(no halo), where E·W means hits in both the east and the west counter walls in time with outgoing beam particles, with no requirement on beam halo particles, and E·W·(no halo) includes the additional requirement that no beam halo time hits be recorded in any of the counters. These trigger signals are then sent to Fred where they are combined with other Level 1 trigger signals to generate a final Level 1 decision (see section Vb.1).

The BBC provide CDF with a nearly minimum bias trigger, and also tag incoming beam halo particles. If such beam halo deposits energy in a calorimeter cell without being tagged, it may appear to be a very high P_t particle when it is assumed that the particle originated at the interaction point. The BBC are also useful in finding the interaction point, which is necessary because the bunch size at the Tevatron is expected to have $\sigma \sim 30$ cm. With a timing resolution of 200 ps, the BBC can be used to localize the interaction point to within 10cm at the trigger level, and also to provide the tracking chambers with an accurate measure of the interaction time.

2) Diffractive and elastic triggers The silicon small angle hodoscopes[1] will be used to generate trigger inputs for elastic and diffractive scattering events. The silicon hodoscopes have four stations in the $\bar{p}$ direction and three in the p direction. Each of the seven stations generates one signal from the electrode covering the back of the entire silicon strip detector. These seven signals are combined with the two Beam-Beam Counter hodoscopes in a Fastbus based RAM look-up module. Here several Level 1 signals are generated for elastic and diffractive events. These signals are then sent to Fred where they are combined with the other Level 1 inputs to generate a Level 1 decision (see section Vb.1).

3) Track finders Two fast track finders are currently under construction for the 1986-87 data taking run. During this run, both of these systems will be used in the trigger and evaluated. We give here just a brief description of the track finders. Details concerning the hardware may be found elsewhere in this volume[5].

The first track finder, known as the Prompt Hit Track finder, provides a trigger signal in time for the Level 1 decision that indicates the presence of a CTC track above a programmable P_t threshold. The CTC is designed[6] in such a way that any reasonably stiff central track is guaranteed to pass within 3.5mm of at least one sense wire in each superlayer. This generates a pattern of 'prompt' drift chamber hits which are identified by a 70-80 ns coincidence gate. The wire patterns of these hits are used by a look-up table to identify stiff tracks in the CTC.

The second fast track finder is known as the Segment Finder and is also capable of producing a Level 1 trigger signal indicating the presence of a high P_t track. The operating procedure for this track finder is to first find track segments or vectors for each axial supercell in the CTC and then to link them together.

Each of the track finders sends its Level 1 trigger signal to Fred for inclusion in the final Level 1 decision (see section Vb.1).

4) Muon triggers The forward/backward muon system also provides a Level 1 trigger. The trigger signal is made using three planes of drift chambers in the forward/backward muon toroids. A hit in the plane closest to the interaction point is used to produce a road in the two outer drift planes to search for hits corresponding to high P_t muons. Triggers are generated with three different P_t thresholds and sent to Fred where they are combined with other Level 1 inputs (see section Vb.1). Details of this trigger input are described in reference 7.

A Level 1 trigger input from the central muon system is made by forming track segments from hits in the muon drift chambers. An angular cut in the R - ϕ plane, corresponding to a P_t threshold and the requirement that the track point back to the

nominal interaction point, is then made. A signal indicating the presence of a central muon candidate is sent to Fred to be included in the final Level 1 decision (see section Vb.1). Details of this trigger input are described in reference 8.

IV. Level 2

a) The calorimeter trigger.

1)CAS and the Cluster Finder The Level 2 decision begins with the interaction between CAS and the Cluster Finder board. During Level 1, the outputs of the comparators on CAS are loaded directly into the sum registers. During Level 2 these outputs are first loaded into the Cluster Finder. The Cluster Finder processes the data and returns a set of towers corresponding to one cluster to CAS where it will then be loaded into a sum register. This procedure causes CAS to create sums for individual clusters of energy in the calorimeters.

The procedure for finding calorimeter clusters is as follows. The threshold value loaded into the fast DAC on RAW is a decreasing ramp. The comparator threshold starts at a high value (eg. 100 GeV) and begins to decrease until one or more calorimeter towers are above threshold, at which point the ramp stops and the output of the comparators are gated onto a 1008 bit bus (24x42, the logical OR of the comparator outputs from the electromagnetic and hadronic crates), the Cluster Bus, and loaded into the Cluster Finder as seed values. A second, low threshold (eg. 1 GeV) is then loaded into the fast DAC, and the towers above this threshold are loaded into the Cluster Finder as low level towers. At this point CAS ceases driving the Cluster Bus. The Cluster Finder asserts the η addresses of all seeds and the cluster control card selects the smallest η value and enables the Cluster Finder to assert the ϕ addresses of all seeds of the selected η. The cluster control card then selects the smallest ϕ value and enables the tower with the selected η and ϕ values to turn on. The selected tower sends a signal to its four nearest neighbors (the 'diagonal' neighbors with different η and different ϕ values are not included) instructing them to turn on if they are above the low level threshold. The newly selected towers send signals to their nearest neighbors and so on until no more contiguous towers are found. A bit map of all towers in the cluster is then sent back over the Cluster Bus to CAS where it is loaded into a sum register. The process is repeated at a cycle time of about 150ns until no new seed towers exist. At this time the high threshold

may be lowered and the process repeated. Once a tower is included in a cluster, it is prohibited from being included in any of the subsequent clusters.

During the processing of clusters, the track finders are monitoring the Cluster Bus. When a cluster bit corresponding to the coordinates of a stiff track is turned on, 5 bits are sent to the Timing Control. 1 bit indicates the existence of a stiff track, and 4 bits provide its momentum. These bits are included in a 64 bit word which is sent to the Level 2 Processors (see section IVc).

After all other Cluster Bus activity has finished, the Cluster Finder will treat the entire detector as a single cluster and a global sum of energies for towers over threshold will be made, just as it is during Level 1. This is useful primarily as a more accurate measurement of missing transverse energy than can be accomplished at Level 1 time when the signals have not settled completely.

2)Crate Sum The operation of the Crate Sum during Level 2 is very similar to that described in section IIIa.4 for Level 1. During Level 2, however, the three analog quantities received from CAS, E_t, $E_t\sin\phi$ and $E_t\cos\phi$, correspond to a single calorimeter cluster. In addition, during Level 2 the Crate Sum uses E_t to produce the pseudo-rapidity weighted sums $E_t\eta$ and $E_t\eta^2$. These five quantities are digitized in an 8 bit FADC, a rounding bit is added, and they are sent as 12 bit quantities to the Listmaker (in anticipation of upgrading to a 10 bit FADC). The Crate Sum also sends to the Listmaker a 7 bit value for N, the number of calorimeter towers in a cluster. If N is zero, that is if no towers are summed, the output of the Crate Sum is forced to zero.

3)Listmaker The Listmaker consists of three different types of boards. Together they perform a variety of arithmetic functions on digital values received from the Crate Sums to produce a list of properties of the clusters found by the Cluster Finder. The list consists of two 64 bit words per cluster (a third word has its origin in the Timing Control, see section IVc), one for electromagnetic energy quantities and one for total energy quantities. The contents of the two words includes 10 bits each of E_t, $E_t\sin\phi$, and $E_t\cos\phi$, 8 bits each of $<\eta>$ and σ_η, 7 bits of $<\phi>$, and 8 bits of σ_ϕ. In the event that a calorimeter cluster spans the boundary between crates, the first three quantities listed will be different from that produced by any single Crate Sum module.

The first of the three Listmaker boards, the Sum board, receives the 12 bit quantities output by the Crate Sum. There is one Sum board for each of the six quantities, and each board receives the outputs of five electromagnetic and five hadronic Crate Sums. These boards sum over the ten crates to produce a 12 bit electromagnetic energy sum and a 12 bit total energy sum. A pipeline latch at the

output stage of the Sum board is strobed by the Timing Control. The 12 bit sum for N is sent to the Timing Control for inclusion in the third word of the list. The remaining five 12 bit sums are sent to the second of the Listmaker boards, the Multiplier board, consisting of an array of 4K RAMs and an array of high speed multipliers. There are two Multiplier boards, one operating on electromagnetic energy sums, and one operating on total energy sums. The 12 bit sum E_t forms the address to the RAMs whose output is a 12 bit representation of $1/E_t$. Four sets of multipliers are used to form the products of $1/E_t$ with each of the four quantities $E_t\sin\phi$, $E_t\cos\phi$, $E_t\eta$ and $E_t\eta^2$. The outputs of the multipliers, $\langle\sin\phi\rangle$, $\langle\cos\phi\rangle$, $\langle\eta\rangle$ and $\langle\eta^2\rangle$ are sent to the last of the three boards, the RAM board. Once again there is one RAM board operating on the electromagnetic energy quantities and one on the total energy quantities. Here a number of functions are performed, primarily through the use of look-up tables stored in RAMs, and the last three quantities needed, $\langle\phi\rangle$, σ_ϕ and σ_η are calculated from:

$$\langle\phi\rangle = \sin^{-1}(\langle\sin\phi\rangle) \text{ if } |\langle\cos\phi\rangle| > |\langle\sin\phi\rangle| \text{ or } \cos^{-1}(\langle\cos\phi\rangle) \text{ otherwise}$$

$$\sigma_\phi = \sqrt{1 - \langle\sin\phi\rangle^2 - \langle\cos\phi\rangle^2}$$

$$\sigma_\eta = \sqrt{\langle\eta^2\rangle - \langle\eta\rangle^2}$$

The five Listmaker quantities (excluding N) are then latched by a strobe from the Timing Control at the output stage of the RAM board for use by the Level 2 Processors.

b) Other Level 2 triggers When the interaction between the Cluster Finder and CAS finishes, the muon systems take over the Cluster Bus, turning on bits corresponding to the η and ϕ locations of muon candidates. For central muons, these candidates are "golden muons", i.e. those muon candidates with CTC stiff tracks directed at them. The map of all muons found is loaded into the Cluster Finder from the Cluster Bus. The Cluster Finder will then select one muon at a time and assert the corresponding bit on the Cluster Bus. During this time the Muon Match Box[8] monitors the Cluster Bus and sends to the Timing Control the momentum of each muon as it is selected. The Cluster Finder will send the η and ϕ values for the selected muon to the Timing Control where it will be included in the third of the three 64 bit words to be sent to the Level 2 Processors. As each bit on the Cluster Bus is turned on, the CAS -

Crate Sum - Listmaker processing proceeds as usual so that the first two words of the list received by the Level 2 Processors contain information regarding energy deposition in the calorimeter by the muon candidates.

c) Level 2 Processors The Level 2 Processors consist of three types of modules: the Cluster Memory, the Mercury modules and the Jupiter module. The modules reside in a single Fastbus crate with a special auxiliary backplane known as the Processor Bus.

The list of calorimeter clusters, isolated muons and total event energy comes to the Level 2 Processors as three 64 bit words every 150-200 ns. The first two words come from the Listmaker, representing electromagnetic and total energy sums as described above. The third word comes from the Timing Control and incorporates information from the Cluster Finder, the muon systems, the track finder and the Timing Control itself. The contents of this word are a 4 bit code describing the origin of the cluster (the Cluster Finder and the muon systems both drive the Cluster Bus), 8 bits for the number of trigger towers in the cluster (N), 11 bits to describe the position of the Cluster Finder seed tower in its 24 x 42 array, a bit to indicate that a stiff track was associated with a calorimeter cluster, and 4 bits of momentum information from the track finder.

As each group of three words arrives they are written in parallel into three Cluster Memory modules, one word per module, and then read out serially onto the Processor Bus. From the Processor Bus, the cluster information is latched by any number of Mercury modules, each designed to calculate a specific physical quantity of interest. For example, one Mercury module, Mercury ET, sums the clustered energy deposition and counts the number of clusters whose energies are above a predefined threshold. Another Mercury module, Mercury EL, selects "electrons" based on cluster width, the ratio of electromagnetic to hadronic energy deposition and the presence of a high P_t track pointing at the cluster. A third Mercury module, Mercury Mu, selects "muons" based on the presence of a track in the muon chambers and, optionally, a cut on the amount of energy deposited in the associated calorimeter cell. The magnitude of missing E_t is also calculated by Mercury Mu. The Level 2 Processor system is easily expandable in that additional Mercury modules, designed to perform specific tasks such as kinematic correlations between clusters, may be added at any time. The results of the operations performed by the Mercury modules are stored in registers accessible to the Processor Bus. Each Mercury module contains a summary data register which is used to return results in a particularly compact form.

When the Mercury modules have completed their functions, the Jupiter module accesses the results through the Processor Bus and makes a Level 2 decision. The

Jupiter module is programmable and thus allows a flexible Level 2 trigger configuration. Jupiter is built on two boards, one of which, the sequencer board, contains microcode memory and a fast ECL sequencer to control program execution. The sequencer board is identical in construction to the Timing Control Master described above (see section IIIa). The other board of the pair, the processor board, manipulates the data from the Mercury modules with a barrel shifter and an ALU. The processor can present either a single condition bit or a group of up to four bits to the sequencer board for use in a branch decision. The global Level 2 trigger consists of the logical OR of a list of possible Level 2 triggers, each of which must satisfy a set of conditions. Typically, each condition is represented by bits in a Mercury data summary register. These bits are used in the Jupiter module as input to multiway branches within its microprogram. We anticipate that this design will allow the Jupiter module to make even a fairly sophisticated trigger decision in just a few microseconds.

The Jupiter module further serves as an interface between the Level 2 Processor system and Fred (see section V), and between the processor system and the Timing Control. Specifically, Jupiter receives a Level 2 enable from Fred which enables the processor system, and sends to Fred Level 2 accepts and Level 2 rejects. From the Timing Control, Jupiter receives and distributes a reset strobe and a strobe for loading data into the Cluster Memory.

Finally, the design of the Jupiter module is such that by adding a single board to handle the Fastbus master protocol, the Level 2 Processors would be able to access data from other Fastbus modules in the CDF data acquisition system.

For the upcoming run, one Level 2 Processor will exist. In the future, however, there will be four such processors in order to handle the partitioning of the detector (see section V).

V. Final Decision Logic: Fred

The Fred board serves several functions in the CDF trigger. It contains the logic for making the final trigger accept/reject decision for both Level 1 and Level 2 based on trigger bits collected from various components of the trigger system. Fred also serves as the interface between the trigger system and the data acquisition system.

a)Partitioning The CDF trigger has been designed to allow different parts of the detector ("partitions") to be run simultaneously with different triggers. Twelve

"autonomous" partitions are intended for calibration and debugging purposes, and are independent of each other. Four possible "CDF" partitions are reserved for physics runs and can share information from all detector elements. Each partition is assigned through a Cross-Point to a Trigger Supervisor[2] which controls the readout for that partition. The interface between the Level 1 and Level 2 triggers and the Trigger Supervisors is handled by two different types of Fred boards called "autonomous Fred" and "CDF Fred", according to the type of partition they handle. Autonomous partitions must provide their own trigger signals, while CDF partitions use the two level trigger described here. Fred is also responsible for keeping track of the deadtime generated by each partition, and for producing the gates needed for measuring the integrated luminosity for a run.

b) The final trigger decision

1)Level 1 Fred receives up to twelve Level 1 input signals and generates a Level 1 accept/reject using a look-up table stored in a 4K RAM. These twelve inputs include the four bits from the Level 1 Sum (section IIIb.6), and bits from the muon logic, the track processor, the beam-beam counters and the silicon counters. With this design, there are 4096 different combinations which can make a Level 1 trigger. The twelve inputs can easily be extended to include other trigger bits by adding a "pre-trigger RAM" as an additional look-up stage whose output is used as an input to Fred.

Each partition has four look-up RAMs which can be independently prescaled to rates between 0.15 Hz and 9.1 kHz. The final Level 1 decision is the logical OR of the outputs from the four RAMs, allowing the acceptance of rare processes at full efficiency along with prescaled rates for more abundant triggers.

2)Level 2 The Level 2 process is initiated by Fred sending a signal to the Timing Control indicating a Level 1 accept.

Each of four Level 2 Processors is assigned to a single partition in "standard" or "veto" mode. Fred generates a Level 2 accept as the logical OR of each of the standard processors' Level 2 accepts logically ANDed with each of the veto processors' Level 2 accepts. A Level 2 reject is generated as the logical AND of each of the standard processors' Level 2 rejects logically ORed with each of the veto processors' Level 2 rejects.

c) Triggering and the data acquisition system A trigger sequence is initiated by the Trigger Supervisor[2] sending a "clear and strobe" signal to the front end electronics and a "Level 1 query" signal to Fred. When an event has been accepted at Level 1, Fred sends a Level 1 accept signal to the Trigger Supervisor, thereby preventing a

reset of the front end electronics. If a trigger is accepted at Level 2, the Trigger Supervisor generates a start scan broadcast to the front end electronics, beginning readout of the event, and a scan in progress signal is sent to Fred. The readout of the trigger information is also started at this time, with the corresponding scanners[2] sending a done signal to Fred when the readout is complete.

To prevent a reset of the electronics by a partition which does not accept the event, a trigger busy signal is generated as soon as a partition accepts an event at Level 1 and sent to all Trigger Supervisors. The trigger busy signals are reset by a Level 2 reject or a signal from the Trigger Supervisor indicating that readout of the detector is complete.

VI. Conclusion

A two level hardware trigger processor for CDF has been described. This trigger system will be used beginning with the 1986-87 data taking run at the Fermilab $\bar{p}p$ collider. The trigger is designed to reduce a RAW event rate of 50-75 kHz to 1-100 Hz before initiating readout of the detector.

While the trigger system is complete, it is also easily expandable. At Level 1 this expansion can be achieved by adding one or more pre-trigger RAMs whose outputs are used as inputs to the 4K Level 1 RAM on Fred. At Level 2, expansion takes place by adding additional Mercury modules to the Level 2 Processors. Since each Mercury module is designed to calculate a particular physical quantity, the addition of a new Level 2 trigger means the addition of a new Mercury module and a re-programming of the Jupiter module. In this way, we have designed a trigger system which is both sophisticated enough to identify the signatures of known physics, such as W or Z bosons, and flexible enough to encompass new and exciting physics which we may find at a center of mass energy of 2 TeV.

Acknowledgment

This work was supported by the National Science Foundation.

References

1. F. Abe et al. "The Collider Detector at Fermilab", submitted to Nucl. Instr. and Meth.

2. E. Barsotti et al., "Fastbus Data Acquisition for CDF", submitted to Nucl. Instr. and Meth.

3. D. Amidei et al., IEEE Trans. Nucl. Sci. 33, No. 1, 817 (1986).

4. G. Drake et al., "The CDF Front End Electronics: The RABBIT System", submitted to Nucl. Instr. and Meth.

5. G. W. Foster et al., "A Fast Hardware Trackfinder fo the CDF Central Track Chamber"", submitted to Nucl. Instr. and Meth.

6. F. Bedeschi et al., "Design and Construction of the CDF Central Tracking Chamber"", submitted to Nucl. Instr. and Meth.

7. D. Carlsmith et al., "Forward Muon Electronics", submitted to Nucl. Instr. and Meth.

8 G. Ascoli et al. "CDF Central Muon Trigger Level 1 Electronics", submitted to Nucl. Instr. and Meth.

Figure Captions

Figure 1. A block diagram of the CDF Level 1 and Level 2 trigger system.

Figure 2. A simplified schematic showing the operation of the Receive and Weight and Compare and Sum boards.

CDF Trigger System

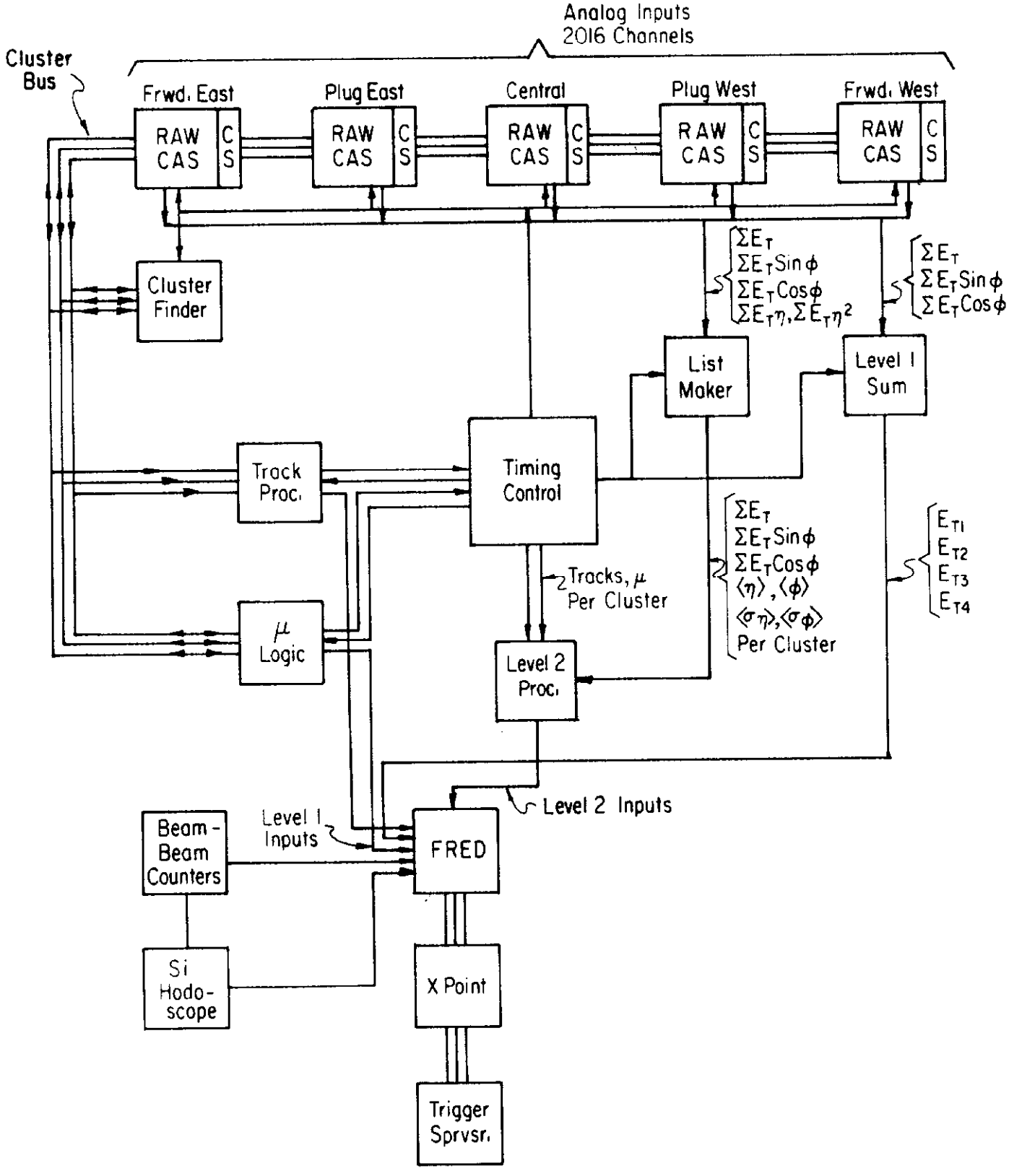

Fig. 1

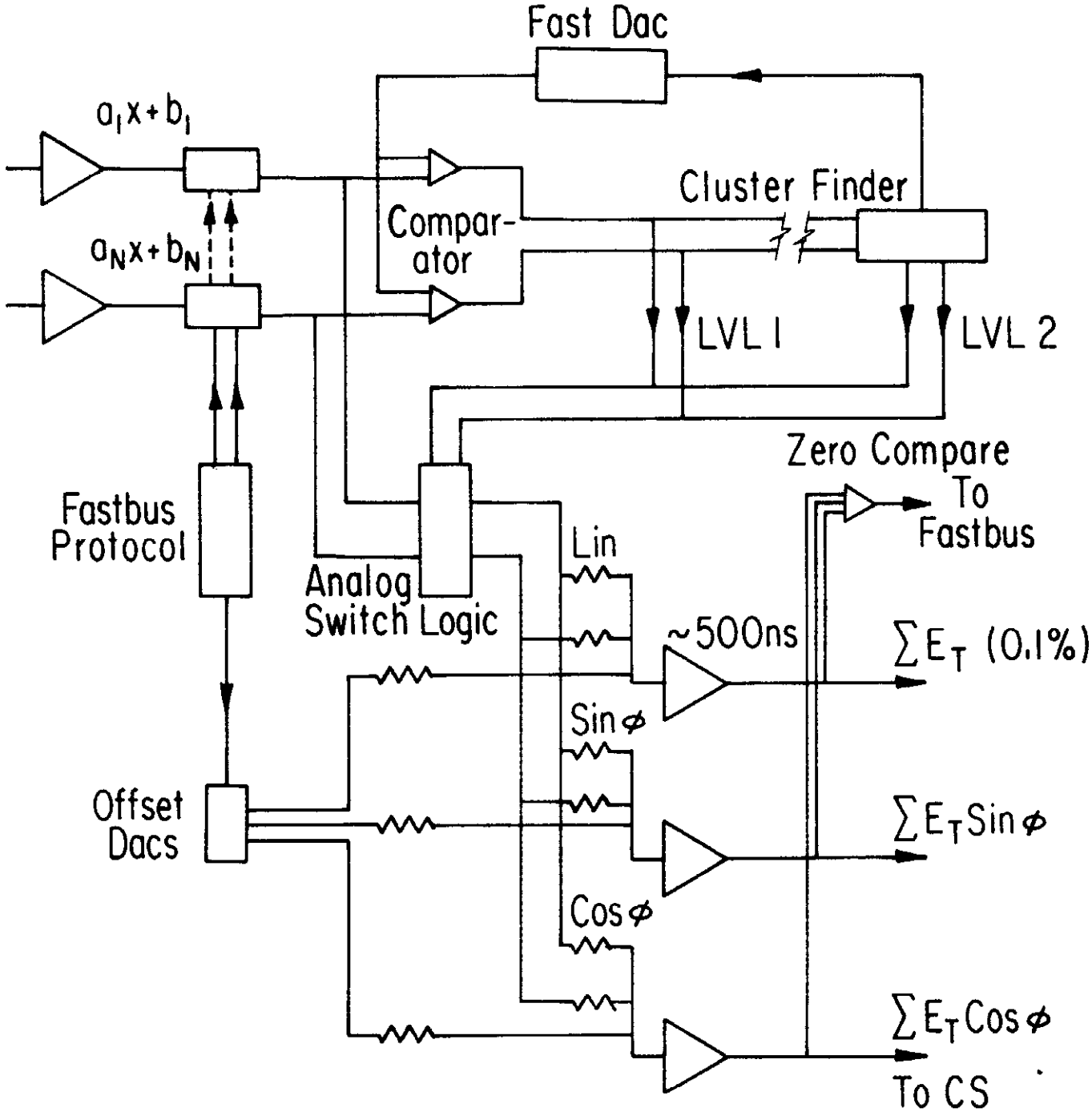
Fast Dac
a_1x+b_1
a_Nx+b_N
Compar-
ator
Cluster Finder
LVL 1
LVL 2
Zero Compare
To
Fastbus
Fastbus
Protocol
Analog
Switch Logic
Lin
~500ns
$\sum E_T$ (0.1%)
Sin ϕ
Offset
Dacs
$\sum E_T \sin\phi$
Cos ϕ
$\sum E_T \cos\phi$
To CS

Fig. 2