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LHCb Status Report

Prepared for October 2000 Resource Review Board meeting

LHCb Collaboration

1) LHCb Detector

1-1) Magnet

A dipole magnet with an iron yoke of about 1500 t and a normal conductive coil made from aluminium providing an integral field of 4 Tm will be used as the spectrometer magnet for the LHCb experiment.

After the approval of the Technical Design Report (TDR) by the research board in April 2000, further optimisation work continued till June. Particular care was taken to reduce the fringe field of the magnet. On 30th of June, the call for tender was sent out for three items, the iron yoke, aluminium conductor and coil construction, to those firms who had replied to the market survey made in late 1999. The tendering procedure has finished and offers are being evaluated now. It is hoped that the orders will be placed toward the end of 2000 to the beginning of 2001.

1-2) Vertex Locator

The design parameters of the detector were re-optimised for physics. Due to the new design of the wake-field suppresser, the silicon sensor can approach closer to the beam than anticipated in the Technical Proposal, reducing the effect of multiple scattering. The outer radius of the detectors was reduced and the number of stations was increased in order to stay with the same acceptance. As a result, the average number of hits per track increased giving more redundant track reconstruction. The number of readout-strips was reduced by 10% without deteriorating the resolution. The next prototype detectors, very close to the final design, will be thin n-on-n detectors. Resolution and efficiency of the detectors after heavy irradiation corresponding to several years of LHCb running were studied using the SPS beam. The outcome of this study will be the basis for deciding which technology to choose; i.e. p-strip or n-strip detectors.

A first version of a complete front-end chip in 0.25-micron technology was submitted in June. Another design of such a chip based on the radiation-hard DMILL technology will be submitted in November. A predecessor of this chip (SCTA) is now regularly used in our test beam. The design of a hybrid carrying 16 of these chips and reading out one silicon sensor is almost completed and first prototypes are expected at the end of year. Design of the off-detector electronics board is in progress. A prototype board including the FADC's is being tested. A first implementation of zero suppression algorithms has been synthesised in the FPGA and tested.

The design of the vacuum tank and the mechanics is now almost completed. In the latest modification, all the feed-throughs and cooling pipes are placed to one side of the tank. This gives more space for installation and the possibility to include Ti-evaporators for improved vacuum stability of the RF-shield. The new design also allows intermediate steps when moving in and out the detectors. This design was first presented to LEMIC, and then discussed in subsequent meetings with the LHC vacuum and RF groups. Various studies are underway to fulfil the machine requirements.

The Technical Design Report of the VELO is scheduled for May 2001.

1-3) Outer Tracker

Outer Tracker of the LHCb experiment is based on the straw technology. The straw tubes have a cell size of 5 mm and lengths up to 3.6 m with wire supports inside the tubes at every 50 cm. The longest prototype modules so far tested in the beam are 2 m long and gave encouraging results. It must be noted that further simulation studies of the performance of the detector could still lead to the conclusion that the cell size in regions of high occupancy should be reduced.

Test beam results show that a gas mixture of Ar(70 %)/CF_4(25 %)/CO_2(5 %) fulfils the LHCb requirements: the maximum drift time is well below 50 ns even for those chambers placed in the dipole magnet. Almost 100 % efficiency per drift cell is achieved and a spatial resolution of 0.2 mm per cell is obtained. Cross-talk between neighbouring cells is typically of the order of 1 % in amplitude.

Ageing effect of chambers is intensively studied. In addition to local irradiation with pencil beams, X-rays and radioactive sources, 2 m prototypes have been installed in the HERA-B detector in May 2000 providing a realistic global irradiation. During the run, which has finished early September 2000, no apparent signs of ageing were observed. The behaviour of the irradiated prototypes are being compared in detail with that of non-irradiated ones in a PS test beam now.

Designs of the tracker stations are in progress. Particular care is being taken to reduce the amount of material as much as possible. It might be possible to reduce the material of the station to be as little as 2 % of a radiation length.

The baseline solution for the readout electronics is being designed using a TDC chip developed for other LHC experiments. Pre-production chips will be available in fall 2000. Although acceptable, this TDC is not ideally suited to our purposes. Therefore, development of a dedicated TDC chip has started and complete prototypes are expected in early 2002. The choice between the two solutions will be made in the middle of 2002.

The Technical Design Report of the Outer Tracker is scheduled for March 2001. Hardware development is essentially on course for meeting this date. Sharing of responsibilities in the production phase will be largely defined by January 2001, one year before the foreseen start of series production of detector modules.

1-4) Inner Tracker

The Inner Tracker of the LHCb experiment covers the region close to the beam pipe where the particle density is very high. Our exhaustive test beam studies show that a micro-pattern gaseous detector with triple GEM-foil can operate in a stable condition with the expected particle density. However, the triple GEM detector has significant drawbacks. First, the size of the charged clusters arriving at the readout plane is rather large. A FWHM diameter of 0.5 mm is observed. Secondly, tracks entering the chamber with a large angle produce signals on several adjacent channels. These effects increase the occupancy of the detector. Therefore, the triple GEM detector cannot be used in the region with the highest particle density. For this region, the silicon micro-strip detector is foreseen.

Engineering studies of the tracking stations with Si micro-strip detectors are in progress. Evaluation of the optimal parameters of the silicon technology was performed and detailed specification fixed. A few pieces of two different prototype sensors have been ordered from two different companies. We plan to have complete detectors by the beginning of 2001. They will be tested at PSI for the high rate and at CERN to measure position resolution with high momentum particles.

The triple GEM detector has an advantage over silicon micro-strip devices in that larger sensor planes can be built without increasing the number of readout channels. If the region to be covered by the inner tracker system increases much beyond 40×40 cm^2, the Si detector becomes too expensive. Therefore, further development of the triple GEM detector is pursued.

A final decision on the layout and technology depends very much on the simulation studies of the particle density, taking account the beam pipe, cables for the detectors and other details. This work is in progress and the decision is planned for early 2001.

1-5) RICH

Work on the RICH detectors over the last year has culminated in the submission of the Technical Design Report for the RICH system in September 2000. In addition to the development of a detailed engineering design for the two detectors, RICH-1 and RICH-2, successful tests have been made of the mirrors and their support structures. The major progress, however, has been on the photon detectors.

During 1999 three options were still being investigated for the photon detectors: two varieties of hybrid photodiode (HPD) and the commercial multianode photomultiplier (MAPMT). The HPDs were development projects at CERN and in conjunction with industry, and were differentiated through the size of their silicon sensor elements: they are known as the Pixel and Pad HPDs. At the end of the year, a review panel was set up to choose the baseline photon detector. It was found that all three would satisfy the performance requirements of the experiment, so the choice was made on the basis of weighing cost against risk. Finally, the Pixel HPD was selected as baseline, with the MAPMT being retained as a backup solution.

During 2000, progress has been made towards realising the final Pixel HPD. The anode will be a silicon sensor with 1024 channels, bump-bonded to a pixel electronics chip. The pixel chip, developed in conjunction with the ALICE experiment, has been submitted to the manufacturer, although delayed by a few months with respect to the original schedule. The rest of the tube, consisting of an 80 mm diameter quartz window with photocathode, and electrostatic focussing to demagnify the image onto the silicon sensor, has been successfully tested with prototype tubes. The current iteration of the pixel anode will be delivered and tested by the end of 2000. At that time, the progress towards production of the final detector will be reviewed. For the Pixel HPD, the pixel anode has to be ready on time before starting the encapsulation of the tube. Therefore, a decision will be taken in the review either to continue the development with a revised schedule, or to change over to the MAPMT backup. Meanwhile, prototypes of the read-out electronics are being produced to verify the complete binary readout chain.

Over the coming year, the engineering design of the RICH vessels, support structure and mirrors will be reviewed, and in the case of the optical components, undergo further testing before finalising detailed drawings by end 2001. There is an ongoing R&D programme for aerogel, aimed at producing samples of high clarity for use as a radiator in RICH-1. Also the study of alignment, monitoring and control will continue, before the final choice of systems is made by end 2001.

1-6) Calorimeter

The LHCb calorimeter system is mainly optimised for the first stage of the trigger by detecting a single high p_T hadron, electron and photon. It consists of a scintillator pad detector combined with a preshower counter followed by a "shashlik" type electromagnetic calorimeter and a hadron calorimeter based on the iron/scintillator tile technology developed for the ATLAS experiment. A similar shashlik type electromagnetic calorimeter has been successfully commissioned at HERA-B.

All the detector parameters were fixed and basic mechanical designs completed for the Technical Design Report submitted in September 2000. For the choice of the parameters, the following points were considered:

- Level-0 trigger efficiency
- Hadron, electron and photon identification
- High and medium energy π^0 reconstruction
- Optimisation of cost and construction effort

A complete calorimeter system was prototyped and tested in the test beam giving the expected performance.

Production of the detectors, in particular for 3312 modules (5952 cells) of the electromagnetic calorimeter and 828 modules (1468 cells) of the hadron calorimeter, is time consuming and labour intensive. For the coming months, we will produce "Module-0" prototypes with exactly the same

parameters as the final detectors in order to prepare necessary tools and to optimise the production process and some design details.

A common front-end electronics will be used for the electromagnetic and hadron calorimeters. A preamplifier chip capable of working with 40MHz bunch-crossing rate without introducing any spillover effect from the previous bunch crossing have been developed. It has been successfully tested in the test beam using the prototype calorimeters. A front-end card including the ADC and Level-0 pipeline buffers has been designed, prototyped and tested successfully. The preamplifier chips for the scintillator pad detector and preshower counter have to cope with the fluctuating pulse shape produced by minimum ionising particles. The two designs can be made very similar. Prototype chips for the preshower counter were successfully tested with the test beam. The common front-end card for the scintillator pad detector and preshower counter is similar to the one for the electromagnetic and hadron calorimeters and their schematic designs have been completed.

1-7) Muon Detector

The optimisation of the muon system layout has finished, resulting in a reduction of 44% of logical channels (now 26k) and 35% of physical channels (now ~150k) compared to the Technical Proposal. The optimised layout has been used to establish a baseline front-end architecture with a realistic data-flow from the chambers to the Trigger and DAQ system.

From the various chamber technologies investigated in many beam tests, Multi-Wire Proportional Chambers (MWPC) with anode and/or cathode readout have been chosen for more than half the area of the muon system. In addition, Resistive-Plate Chambers (RPC) will be used in areas where the required rate capability is less than 1 kHz/cm^2 and where the requirement on cluster-size is rather moderate.

Special emphasis in this year's beam tests has been put on the investigation of front-end chips. It has been shown that for the readout of MWPC the ASDQ chip with an adaptation allows efficiencies above 95 % to be obtained within a 20 ns time window over a plateau of 400 V. The input capacitance was up to 200 pF and an Ar(40%)/CO_2(50%)/CF_4(10%) gas mixture was used. In parallel, CARIOCA, a fast binary 0.25 μm CMOS FE-amplifier has been developed, using a novel current-mode technique. A feasibility study of a first prototype showed very encouraging results. Since CARIOCA is an application specific circuit, it allows to integrate parts of the required OR logic of the muon system on the chambers. The GaAs and Bari chips, developed for ATLAS and CMS, are under study for the RPC detector.

1-8) Trigger

Level-0: Muon trigger

The performance and robustness of the trigger has been tested for the different layouts, worst-case noise levels and for luminosities more than twice larger than our nominal running scenario and found to be satisfactory. Several boards have been prototyped to test the following:

- High-speed optical links with high integration density (1.6 Gbit/s, and up to 20 links/9 U board).
- Synchronisation protocol.
- Utilisation of high density FPGA's.
- Point to point backplane connections at 480Mbits/s.
- Multi-point connections between up to 16 boards at 40MHz.

Several of the above aims have been already achieved in preliminary tests. The final design is foreseen for the end of this year.

Level-0: Calorimeter trigger

The part of the calorimeter trigger situated on the Front-end Cards has been defined in detail, and has been fully simulated. The board is being prototyped to confirm the simulation. A technical description of the Selection crate has been made. The Validation Cards sit in between the Selection Crate and the front-end cards, and will be designed by beginning 2001. The description of the Validation Card has to

be improved to obtain a complete and detailed specification at the end of this year. In particular, the inclusion of the π^0 trigger, and the consequence of these changes to the Selection Crate will be clarified in the next few months.

Level-0: Pile-up veto

The effectiveness of the pile-up veto has been re-evaluated, especially in view of the new PYTHIA settings that have been adopted by LHCb. The new generator gives a multiplicity distribution that is much wider than that given by the old generator and the algorithm had to be refined. The new algorithm is much more robust. The electronics design is foreseen for the end of this year.

Level-0: decision unit

The Level-0 Decision Unit was modelled in VHDL. Some ideas on the basic trigger algorithms to be implemented have been exchanged, which should lead to a final definition of the requirements by the end of this year when the usefulness of triggering on π^0 will reach its final decision.

Level-1

The network between the Front-end Boards and the CPU farm was simulated in Ptolemy, leading to the adoption of a 2D-mesh topology using SCI as a test bench. A prototype network has been set-up to test the results of the simulation, and reach a transaction rate of 1 MHz. This should be achieved by the beginning of next year, but first results (0.5 MHz rate) have already been obtained. The algorithm has been coded in C inside the LHCb GAUDI framework. The algorithm is now being completed, and bench-marked to be able to calculate the size of the farm needed, and the necessary L1 latency. This should be achieved by the end of 2000. Work is going on improving the algorithm. Also combining Level-0 and Level-1 data is under study. First results are expected at the beginning of next year.

1-9) Computing

The computing project in LHCb covers both off- and online aspects of the experiment, including the Experimental Control System.

Data Acquisition System

The architecture of the Timing and Fast Control (TFC) System has been revised to allow for more flexible partitioning of the DAQ system. The TFC switches have been specified and designed, and a design review is planned for October 2000. The Readout Supervisor module has been specified, and the design is in progress. The design review for this board is foreseen for February 2001.

Prototype boards of the Readout Unit have been produced and commissioning of the functional blocks is now in progress. The protocol between the Readout Unit and Event Builder has been specified.

Studies have started on use of Gigabit Ethernet as the switching fabric of the event builder. Simulation of the full LHCb readout architecture and protocols is now starting. The event building software is to be implemented to run on intelligent Network Interface Cards (NICs). Performance tests on the NICs have already been completed. The event building code is now being implemented.

No specific LHCb studies have been made so far for the Event-Filter Farm (EFF) but we participate in the common EFF project meetings. Our specific concern is to integrate the control of the EFF with the LHCb Experimental Control System (ECS).

Experiment Control System

LHCb participates actively in the Joint Controls Project (JCOP) with the other LHC experiments and CERN/IT division. The tendering procedure for the commercial controls software package (SCADA) was recently completed. The approval by CERN Finance Committee for the selected product was given in September 2000. The JCOP Architecture Working Group has defined a controls hierarchy, including partitioning rules and the basic alarm handling mechanism.

A single controls framework is being built which has responsibility for configuring the operational environments of the detector (voltages, temperatures, gas pressures etc.) and of the data-taking system (hardware configuration, run control). A first prototype has been built based on the SCADA software, which includes a Finite State Machine package and a communication mechanism for accessing non-SCADA platforms. Investigations have started into the use of commercial credit-card PCs for interfacing the control system with electronics boards in a radiation free environment. A prototype is being designed now. We plan to replace the existing test beam DAQ system (CASCADE) by the new SCADA-based framework prototype.

Data processing Software

All LHCb data processing applications are being constructed using a basic software framework, called GAUDI. Five releases of this framework have now been made since the project started in September 1998, each increasing the functionality. The latest releases allow simulated events stored in ZEBRA format to be read and new data to be written using an OO persistency tool taken from the ROOT package. Other new components include a structured description of the detector and its geometry based on the use of the XML language and support for statistical data e.g. histograms. Work is now in progress to extend the framework in many specialised areas, such as integration with the GEANT4 simulation package, the addition of components for managing calibration and alignment data, the development of a visualisation framework and analysis tools.

A new LHCb reconstruction program, called BRUNEL, has been developed that is based on the OO framework (GAUDI) but which uses most of the existing physics algorithms written in FORTRAN. At the same time much effort has gone into developing new algorithms, redesigned using OO methods and written in C++. Examples include the RICH pattern recognition algorithms, the track reconstruction algorithms etc. This new OO code is gradually being incorporated into BRUNEL with the aim of eventually producing a reconstruction program that conforms entirely to an OO design.

Studies have also started to check the ability of GEANT4 to reproduce the results obtained with detector prototypes in the test-beam. This is the first step towards the development of a new OO simulation program, based on GEANT4 and GAUDI.

Computing Infrastructure

LHCb has participated in the MONARC project, and in the definition of the Datagrid and national GRID projects. As part of the participation to the LHC computing review, an LHCb computing model has been defined to respond to the special needs of the experiment. In accordance with the "1/3 CERN, 2/3 outside" rule the majority of the Monte Carlo production load has been notionally placed outside CERN in Tier-1 and Tier-2 centres in France, Italy, UK, The Netherlands and, hopefully, other countries (Switzerland, Russia). Estimates have been made of the requirements for these centres and CERN.

In the coming years LHCb will fully participate in the GRID projects, and develop the MC production facilities appropriately. Work has already commenced involving CERN, RAL and Liverpool, and will be extended to other countries and institutes.

2) Experimental Area

2-1) Infrastructure in UX cavern

The counting houses from the DELPHI experiment will be used in LHCb and their arrangement within LHCb behind the radiation-shielding wall has been determined. The final design will be available end of this year. The counting house will have room for all racks presently foreseen including a high safety factor. Platforms for the gas racks will be placed, above the two SAS's. They will provide space for 24 gas racks in total.

At present the detector assembly close to the interaction point is being studied. As the available space for the RICH-1 and the Vertex detector is very tight, a careful study of the different manoeuvre has to be performed.

2-2) Equipment from LEP experiments

LHCb has studied the LEP-LHC equipment transfer list and decided which of the available parts of the LEP experiments are useful to acquire. Most of the equipment will come from the DELPHI experiment and a few facilities from ALEPH are planned for the support structure of the LHCb detector.

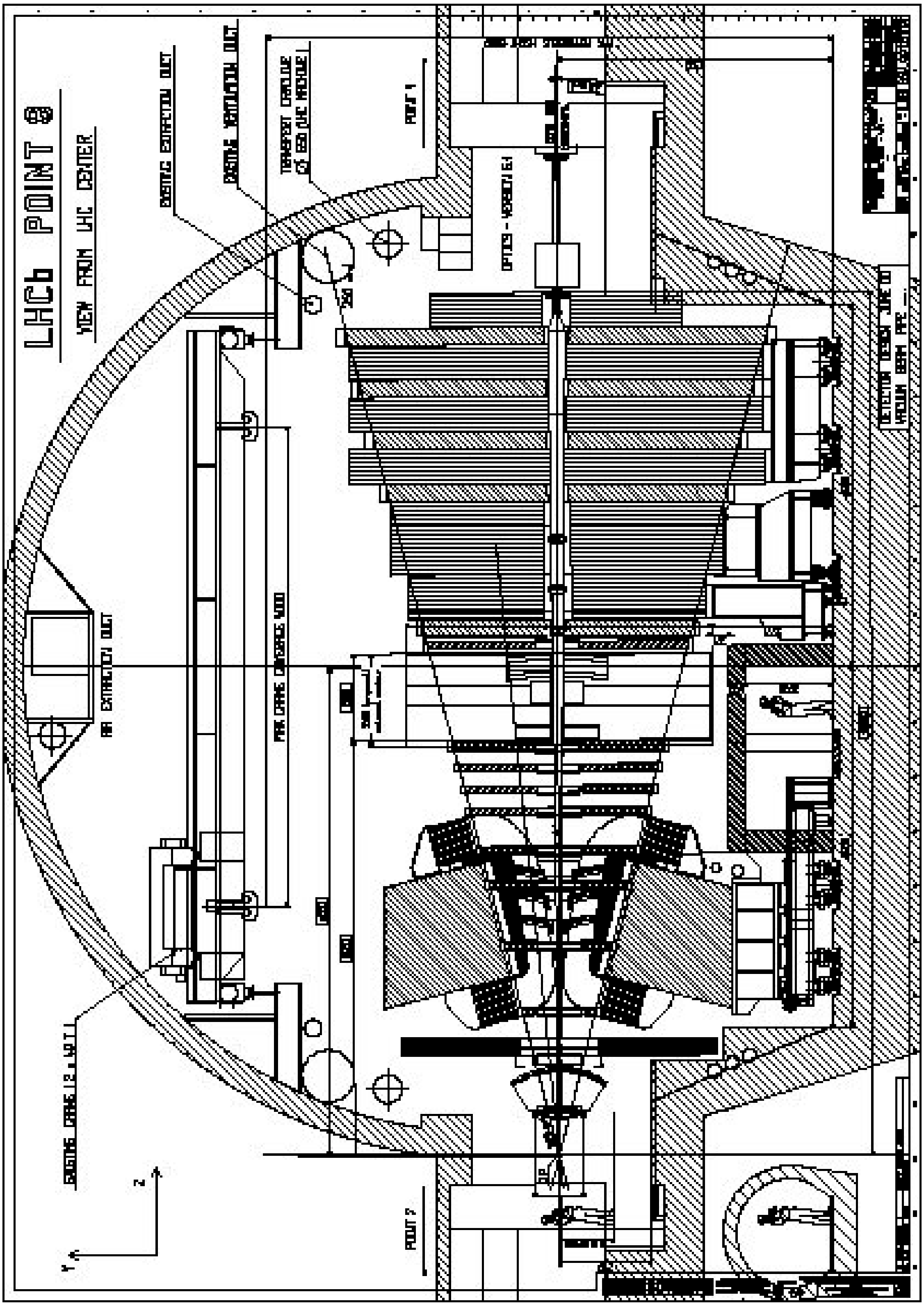
3) TDR submission dates

Magnet	Completed (12/1999) and Approved (4/2000)
Vertex Locator	5/2001
Inner Tracker	9/2001
Outer Tracker	3/2001
RICH	Completed (9/2000)
Calorimeter	Completed (9/2000)
Muon	5/2001
Trigger	1/2002
DAQ	1/2002
Offline	12/2002

4) Status of the Collaboration

In addition to CERN, we expect funding from the following 13 countries: Brazil, France, Germany, Italy, China, Poland, Romania, Russia, Spain, Switzerland, the Netherlands, Ukraine, and United Kingdom. About 500 physicists are participating from 50 institutes.

Additionally, two institutes are participating in the experiment as "Technical Associate Members". They participate in the experiment for education of their students (Esppo-Vantaa Institute of Technology, Finland) or some specific technical aspect of the detector (Geneva Engineering School, Switzerland). Their participation is hosted by one of the member institutes (CERN for Esppo-Vantaa Institute of Technology and University of Lausanne for Geneva Engineering School) who guarantees the responsibility of the Technical Associate Institute toward the LHCb collaboration.


LHCb POINT 8
VIEW FROM LHC CENTER
AIR EXTRACTION DUCT