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CDF Run IIb Silicon Vertex Detector DAQ Upgrade

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Abstract— **The CDF particle detector operates in the beamline of the Tevatron proton-antiproton collider at Fermilab, Batavia, IL. The Tevatron is expected to undergo luminosity upgrades (Run IIb) in the future, resulting in a higher number of interactions per beam crossing. To operate in this dense radiation environment, an upgrade of CDF's silicon vertex detector (SVX) subsystem and a corresponding upgrade of its VME-based DAQ system has been explored. Prototypes of all the Run IIb SVX DAQ components have been constructed, assembled into a test stand and operated successfully using an adapted version of CDF's network-capable DAQ software. In addition, a PCI-based DAQ system has been developed as a fast and inexpensive tool for silicon detector and DAQ component testing in the production phase. In this paper we present an overview of the Run IIb silicon DAQ upgrade, emphasizing the new features and improvements incorporated into the constituent VME boards, and discuss a PCI-based DAQ system developed to facilitate production tests.**

Index Terms— **CDF Run IIb, Silicon strip detector, Data acquisition, VME, PCI.**

I. Introduction

In the ongoing Run IIa phase, the Tevatron collides proton and antiproton beams at a bunch crossing interval of 396 *ns*, producing a center-of-mass energy of 1.96 TeV. In the future the instantaneous luminosity is expected to go up by a factor of 3-4. From the viewpoint of SVX DAQ, this change demands a radiation-hard electronic system, able to support a sufficiently high rate of data transfer. At a typical first level trigger rate of 40 KHz, the data necessary for making trigger decision must be digitized and read out within 10 μs. The Run IIb silicon upgrade [1] is thus driven by two important aspects of the Run IIb operating conditions. Since the SVX detector is located in a dense radiation environment, all the active electronic components need to be radiation-hard. Secondly, owing to a higher number of interactions per beam crossing, a high data transfer rate and a fast trigger decision logic must be employed for deadtimeless DAQ operation. The first issue is addressed by minimizing electronic components in the high radiation region and fabricating all the remaining active components based on a 0.25 μm CMOS technology, which is adequately radiation tolerant for Run IIb purposes. For deadtimeless operation of the DAQ an optimized readout configuration has been adopted.

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II. Changes in DAQ Scheme

In the present (Run IIa) configuration, silicon data is digitized and read out from double-sided sensors (r-ϕ and z) using SVX3 chips. Silicon sensors in the SVX detector are assembled into ladders, arranged in a 12-fold symmetry in ϕ, 5 layers radially and 3 barrels in z. A single readout chain comprises of a Port Card (PC) connected to 44 SVX3 chips, mounted on sensors from 5 layers in a ϕ wedge, by means of High Density Interconnects (HDIs). The PC decodes control signals from a Fiber Interface Board (FIB) directed to the chips, generates calibration voltages using a DAC and provides regulated analog power to the chips. It also converts the data coming from the chips into optical signals to be sent out to the FIB, through a FIB Transition Module (FTM). At the FTM these signals are converted back to electrical (ECL) signals. These inter-conversions are achieved by Dense Optical Interface Modules (DOIMs), which employ transmitters (PC-end) and receivers (FIB-end) to send the data from the PC to the FIB. A FIB module controls 2 PCs through a set of copper lines, based on commands sent from the Silicon Readout Controller board (SRC), which acts as a command/data flow supervisor for the whole SVX DAQ system. Command signals from SRC are sent to FIB boards in a crate via a FIB fanout board (FFO), over a 1.5 GHz optical link (G-Link). Data from each FIB are serialized into high speed G-Links and transferred to the VME Readout Buffers (VRBs). Each SRC controls 12 VRBs

in a crate through a VRB fanout (VFO) board. The SRC communicates with CDF Trigger System Interface (TSI) over an optical link.

In the Run IIb design, a *stave* is used as the fundamental element of the new SVX system. Figure 1 show the layout of the Run IIb silicon detector (SVXIIb). A stave consists of 3

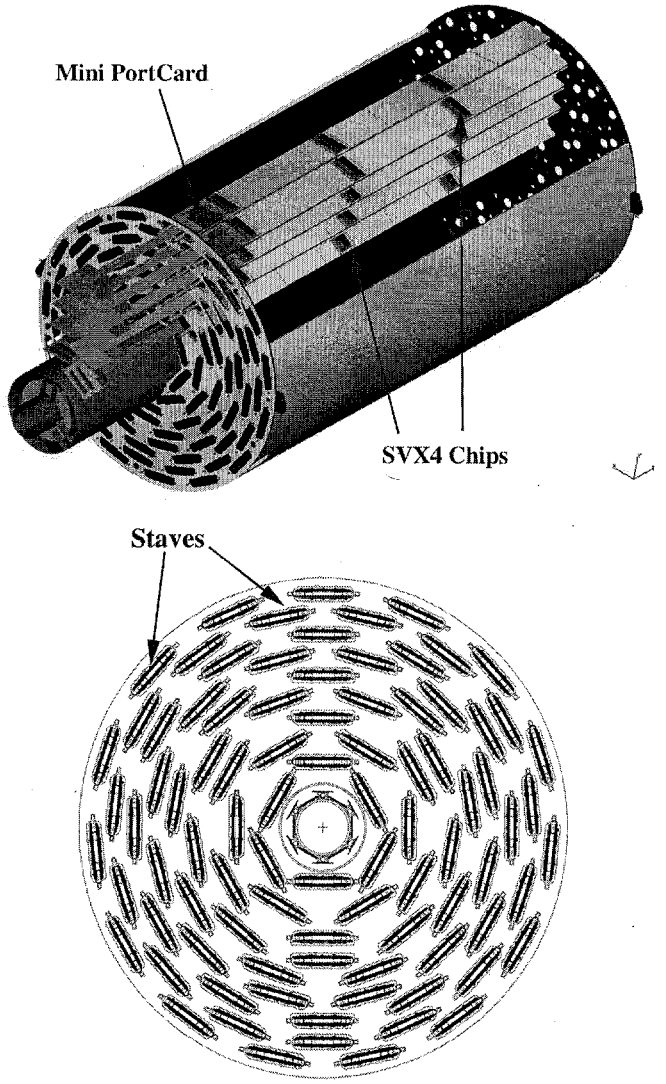

Fig. 1. Stave configuration and layout of the SVXIIb detector.

modules mounted on each side of a carbon fiber - foam core with embedded cooling and cables. Each module consists of 2 single-sided silicon sensors and one hybrid. Each hybrid has 4 SVX4 chips for charge integration, digitization and readout of silicon data. Each stave (6 modules) comprises a single readout unit. The stave design was optimized to give excellent tracking performance in a high radiation environment with minimal mass and ease of construction. Figure 2 shows a block diagram of the SVXIIb DAQ components. Command and data flow directions are indicated by arrowheads. As mentioned earlier, it is desirable to move active electronic components out of the high radiation environment. As a step in this direction, the decoder functionality of the DAC/Decoder/Regulator (DDR) chip of Run IIa Port Card has been moved to a new FTM [2], outside the high radiation region of Run IIb, leaving the transceiver chips on a new Mini Port Card (MPC) [3] which is mounted on one end of each stave. A new pair of Junction Port Cards (JPC) [4] are located just outside the detector volume, between MPC and FTM, for data/control transmission and power supply. The data JPC transmits data and control (LVDS) signals bi-directionally, as appropriate, and the power JPC provides digital and analog voltages for the SVX4 chips, HV for the sensors and power for the MPC. JPC is split into two boards due to space constraints. A study showed the DOIMs not sufficiently radiation-hard to survive Run IIb. So copper cables are chosen to carry data from the MPCs to the FTMs.

Before an SVXIIb data acquisition cycle begins, the SVX4 chips are initialized by FIB. In this step FIB commands are decoded by FTM which then sends them to the chips via the data JPC and the MPC. The configuration and channel mask bits are first downloaded to a 148-bit shift register on each SVX4 chip and then the configuration bits are clocked into a shadow register, completing the initialization. As in Run IIa scheme, SRC coordinates trigger, control and data flow in a DAQ cycle.

A. Trigger Configuration

To facilitate higher rejection power for uninteresting events, CDF employs a 3 tiered trigger system in Run IIa. The decision time for level-1 trigger being 4 μs, all front-end electronics are pipelined, with on-board buffering of 42 beam crossings. The level-1 trigger is distributed by the TSI to SRC, and subsequently transmitted to the SVX3 chips through FIBs, controlling them, for the readout of data from a particular pipe-cell. The data is sent to VRB buffers where they wait for a level-2 trigger. VRBs store data from events corresponding to up to 4 pending level-2 decisions in their internal buffers. A splitter is employed to send a replica of this data to help discriminating tracks with large impact parameters in level-2. A successful level-2 trigger initiates transfer of the data to DAQ buffers and subsequently to level-3 nodes via a network (ATM) switch, where events are fully reconstructed from various sub-detector informations. A successful level-3 trigger lets the data be stored in mass storage media.

Most of the Run IIa trigger scheme remains same in Run IIb with a few exceptions. The non-wedge geometry of SVXIIb requires a few modifications to the existing (Run IIa) wedge-symmetric level-2 Silicon Vertex Trigger (SVT) hardware, for complete compatibility. These modifications, however, have no impact on the Run IIb SVX DAQ design.

III. Design and Functionality of the Boards

MPC is a fine pitch thick film circuit laid out on 500 μm thick *BeO* substrate. It is composed of 6 circuit layers made of Gold and features high thermal dissipation and long radiation length. Each MPC has 5 transceiver chips for control signal and clock reception from the FIB and silicon data and control signal

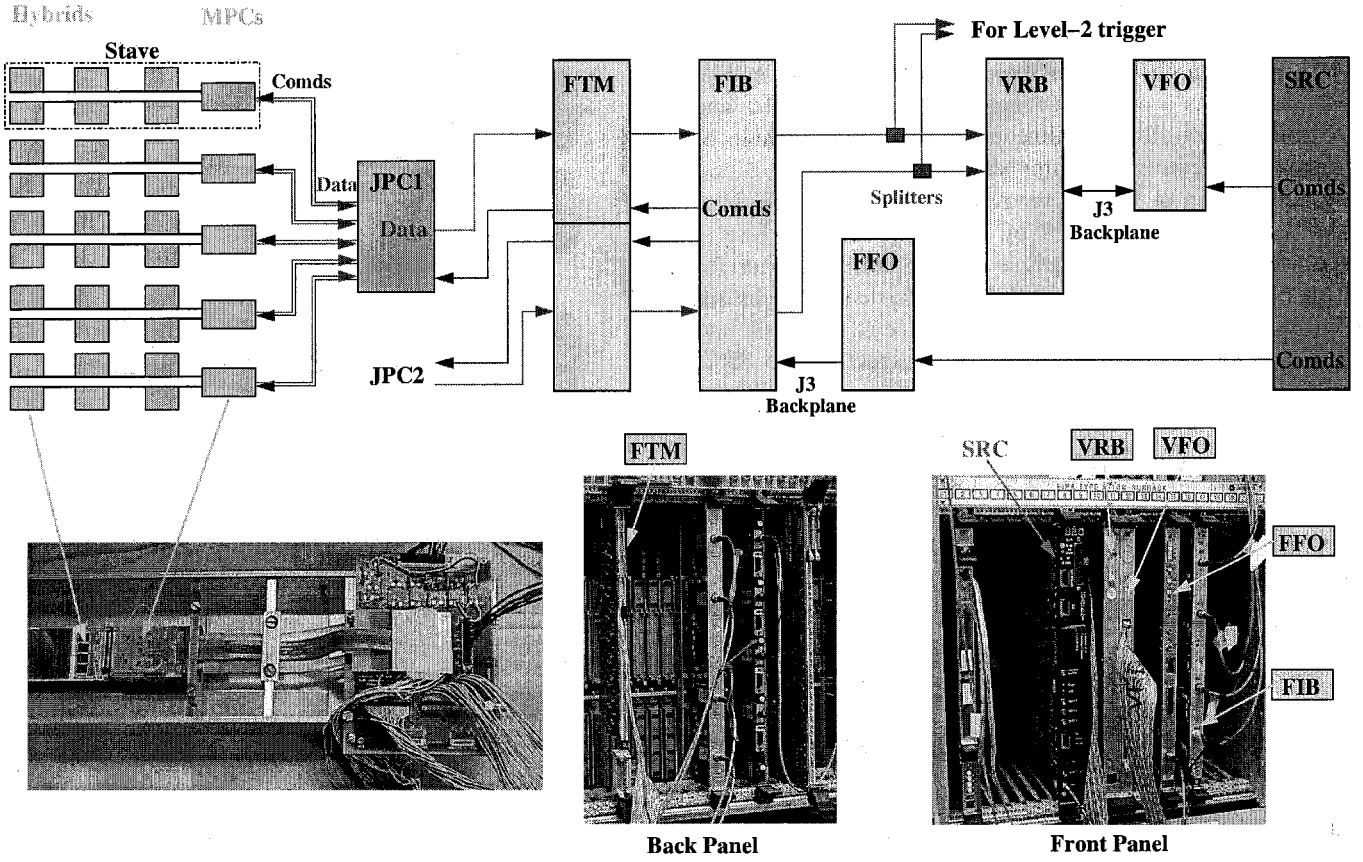

Fig. 2. Block diagram of the SVXIIb DAQ system. Also shown are pictures of real DAQ components from a test stand.

transmission back to it. In addition, it converts differential signals to single-ended, as necessary, and regenerates the clocks to drive the SVX4 chips. MPC is electrically connected to the ϕ–side bus cable by means of wire bonds and to the z–side bus cable by means of a flex circuit, called the *Wing*, soldered to it. Another pair of flex circuits (*pigtails*) provide low bias voltages for SVX4 operation, high voltage for sensors and carry data out of the chips. A total of 180 MPCs would be used to readout layers 1–5 of the SVXIIb detector. MPC functionalities are embedded into the hybrids for the innermost (L0) layer.

As mentioned in Section II, JPC functionalities are split into two boards due to space constraints. The power supply JPC is responsible for providing regulated power to all the stave components. The data JPC, on the other hand, acts as a bi-directional LVDS repeater between 5 MPCs and half of an FTM. Several control signals are fanned out from FTM to JPC, each of which are connected to two LVDS drivers in JPC. The SVX4 chip has 3 bi-directional LVDS bus lines which are driven in opposite directions during digitize and readout operations, using a control signal. JPC uses the same signal to control its bi-directional drivers, ensuring their compatibility with the MPC drivers. A total of 52 JPCs (18×2 for layers 1–5 + 8×2 for L0) would be used to readout the SVXIIb detector.

FFO and FIB boards are unchanged in Run IIb DAQ design. The FFO is a 9U$\times$400 VME board which resides in slot-14 of each FIB subrack. It receives commands and timing signals from SRC via G-Link and fans them out on the J3 backplane for use by the FIBs. Like the FFO, the FIB is a 9U$\times$400 VME board, a maximum of 12 of which populate a FIB subrack. On receiving SRC commands via FFO, it interprets them and sends clock sequences to the SVX4 chips for initialize, digitize and readout operations. It controls data readout from the SVX4 chips, transfers data to VRBs and the SVT system for level-2 trigger decision. The FIB firmware has been modified to accommodate new command clock sequences in Run IIb.

The new FTM is a 9U$\times$120 VME board which mates with a FIB board via J3 backplane in a FIB subrack. An FTM controls 240 SVX4 chips through 2 JPCs, each connected to 5 staves. It employs an FPGA to control and readout each JPC. The electrical protocol of the front and back panels of FTM are LVDS (JPC interface) and TTL (FIB interface), respectively. So a CPLD is used as a level translator to enable the FPGAs to drive the data bus directly to the backplane. A local 53 MHz clock is used to realign data in the FPGAs, before being sent out to the FIB, and also to readout data from SVX4 chips. FIB commands are decoded in each data channel of the FTM and then sent to 10 staves via 2 JPCs. Other attractive features of the FTM include remote programming through the VME bus, loopback mode, detector data emulation and logic analyser access for diagnostics.

The VRB, VFO and VTM 9U×400 VME boards are unchanged in Run IIb DAQ design. Functionalities of VFO and VTM are similar to those of the FFO and the FTM in FIB parlance. VRB is a multiport memory designed to buffer and filter data for transfer to online processors. It is capable of storing up to 12 events (programmable) which are either waiting for a L2 decision or waiting for readout to L3. In CDF SVX mode, the VRB is controlled by SRC. Following a level-1 trigger acceptance SRC assigns a readout buffer number for storage of incoming data. Several data consistency checks are performed while data is being received, *e.g.* pipe-cell and bunch crossing number mismatch with respect to the SRC, data truncation, *etc.* Following a level-2 trigger acceptance the SRC assigns a scan buffer number for the stored data to be transferred to a VME data output FIFO.

The SRC is a 9U×400 VME board which coordinates SVXIIb operation and data readout with the trigger supervisor (TS) and CDF master clock. It receives clock signals and bunch crossing information from the master clock and passes them on to FIB for use by the SVX4 chips and for timing all the G-Link connections. On receiving a level-1 trigger acceptance, SRC marks a particular pipeline capacitor of an SVX4 chip (containing an event of interest) and instructs FIB for its digitization and readout. On completion, marked by success status from the FIBs and VRBs, the SRC clears this cell at the next beam gap. The VRBs return status signals to the SRC indicating when they are busy reading data from the FIBs and when they are passing data to level-3 processors after a level-2 acceptance. After completion of all the tasks pertaining to a trigger decision, the SRC returns status signals to TS. An on-board trigger emulator on the SRC is convenient for DAQ debugging in test stand environment. Taking advantage of the on-board data buffering capability of the new FTM, studies are underway to allow the SRC to handle a level-1 trigger acceptance rate of 100 KHz, compared to the present rate of 40 KHz. This would be achieved by using a faster SRC/FTM clock for data digitization, reading out a fraction of data necessary for SVT processing, in addition to replacing present 8 FPGAs on the SRC with a faster and high logic capacity FPGA.

IV. VME DAQ Software and User Interface

In Run IIa a Java-based framework, called *cdfvme* [5], has been adopted for DAQ code development, operation and maintenance. It offers a convenient way to create board objects and link them together into a complex DAQ system. It employs a Fermilab version of CORBA (Common Object Request Broker Architecture), ROBIN, for the board objects (**clients**), *e.g.* FIB, SRC *etc.*, to talk to VME crates (**servers**) over ethernet. A Fermilab version of VISION (Versatile I/o Software Interface for Open-bus Networks) library, FISION, lets the actual boards in a crate talk to each other. On the VME crates MVME processors (68K or PowerPC architecture) run VxWorks operating system, capable of network-based DAQ operation. Figure 3 shows a block diagram of the SVX DAQ code and its components. For convenience, *cdfvme* framework

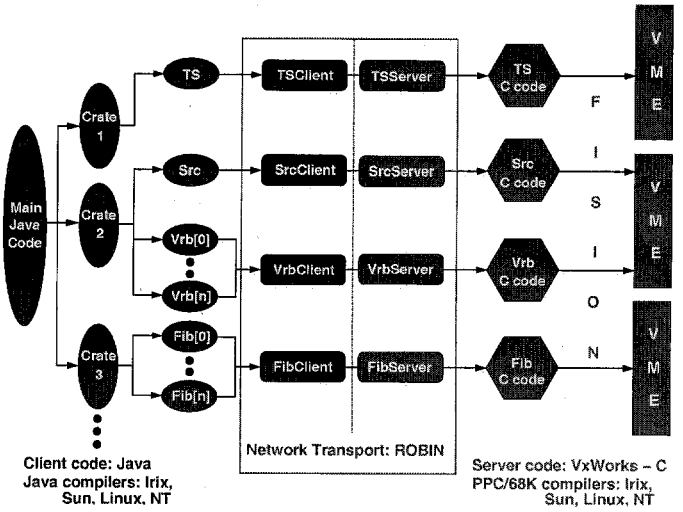

Fig. 3. A block diagram of various components of SVX DAQ code

is split into 3 packages, which are maintained and distributed centrally as Fermilab products:

- `cdfvme_common`: a package which carries all the code common to CDF DAQ systems, definition of boards, tools to combine basic boards into complex systems, base classes to write test programs and means to run them. It also provides a library of useful utility functions.
- `cdfvme_template`: a package containing templates for VME board control, monitoring and testing. These templates provide code structure for easy implementation of board-specific server-side (C) and client-side (Java) codes and link them together. For example, the core SVX DAQ package, `svxdaq`, is derived from this package, which implements the whole CDF silicon DAQ board assembly and the client code for driving *HistoScope*, the online histogramming package.
- `cdfvme_teststand`: a package containing template user interface code to implement, manipulate and run a board system derived from `cdfvme_template`. For example, the `svxii` package implements a test stand for the `svxdaq` system-of-boards, and is in use for all Run II silicon test purposes.

The user interface to `svxii` is highly configurable, making use of a set of ASCII config files. One of its most attractive features is that it lets direct access/manipulation of VME registers on the constituent boards for diagnostic purposes. A Fermilab-developed graphics package, *HistoScope*, is employed in `svxdaq` package for visualization and customization of online data. For Run IIb tests, an SVX4 chip class is created and integrated into the `svxii` package. The modified code lets use of SVX4 chip systems on demand and maintains backward compatibility with the Run IIa usage. Figure 4 shows a GUI panel for configuration of a series of SVX4 chips.

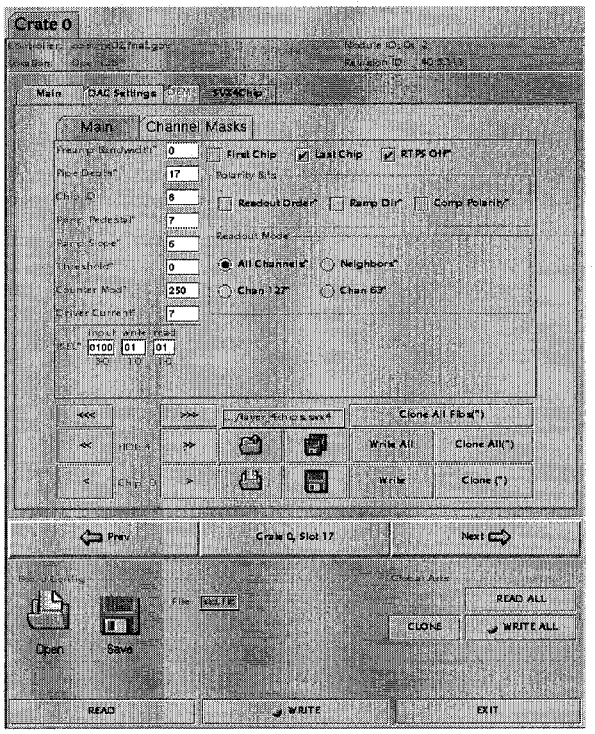

Fig. 4. A Java-based user interface to SVX DAQ system

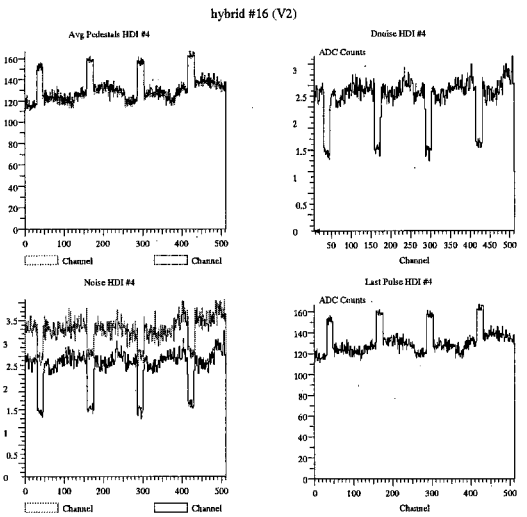

Fig. 5. A HistoScope (online) display of a pedestal run with internal charge injection

V. An SVXIIb VME Test Stand

All the prototype boards have been combined into a VME test stand and operated using the modified DAQ software. Utilizing the SRC on-board trigger emulator, this system works well in various modes of operation of the SVX4 chips, namely deadtimeless, read-all, sparsification and real-time pedestal subtraction. Figure 2 shows pictures of this setup in operation, which lets various detector and DAQ components, namely hybrids, silicon sensor modules and staves, to be tested under almost real conditions. A HistoScope online display is shown in Figure 5. The red (upper-left) histogram shows average pedestal distribution of 4×128 channels of an SVX4 hybrid. The bumps correspond to the injected charge. The blue (lower-left) histogram shows channel-by-channel measured noise.

VI. A PCI-based DAQ System

The PCI Test Stand (PTS) [6] is an inexpensive and flexible DAQ system, developed to test SVXIIb detector components during production. Its design is driven by the necessity to build several test stations to test the components quickly and efficiently, so as not to slow down the assembly and verification tasks. Flexibility is also important because new ways to study the electronics are constantly devised and must be implemented quickly for optimal progress.

The PTS consists of a Linux host computer and two specialized boards, a PCI Test Adapter (PTA) and a Programmable Mezzanine Card (PMC). Figure 6 shows a pair of PTA and PMC cards ready for installation into a host computer. The PTA contains 2 Mb of on-board memory, a PCI interface chip, an Altera APEX EP20K200E FPGA, and connectors needed to attach the mezzanine card. The PMC has a Xilinx Virtex II XC2V1000 FPGA which supports a large number of I/O standards, such as LVTTL, LVCMOS, LVDS, bi-directional LVDS, and DDR buffering on more than 200 pins connected to I/O headers on the PMC board. A 50 MHz crystal provides the timing reference. The Virtex II also has a small programmable RAM which is convenient for storing command sequences to be sent to the SVX4 chips. Signals may be programmed individually by direct register writes under computer control, or they may be clocked out of FPGA RAM at high speed. The former technique is used for initializing the chips, when the synchronization of the readback of the initialization bits is not guaranteed by the SVX4 chip. Acquisition, digitization, and readout are accomplished with high-speed sequencing of the control pattern, and the data are synchronized with the OBDV signal returning from the SVX4 chips.

The control patterns for the SVX4 chips are encoded in easily-editable ASCII files which are parsed on the computer, and then loaded into the Xilinx FPGA RAM. A signal is sent by the computer to execute the pattern once. Data received

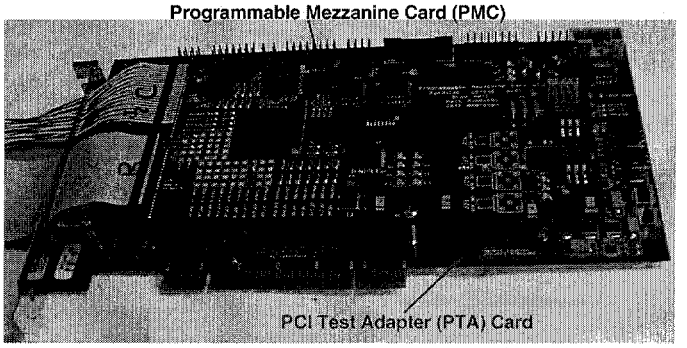

Fig. 6. A pair of PTA and PMC cards

from the SVX4 chips are latched in DDR buffers and sent to PTA RAM. The computer then reads the data back from PTA RAM at PCI bus speeds. An option allows an acquire pattern to loop indefinitely until an external trigger (which can also be simulated by a computer write to a register) arrives, upon which the digitize-and-readout pattern is sequenced, and control passes back then to the acquire pattern. The PTS is configurable to test single chips and hybrids by directly connecting them to the FPGA I/O pins, or to test staves via MPC and JPC interfaces.

Data acquisition with PTS is performed through a customized ROOT-based graphical user interface software package (ROOTXTL). Most of the dedicated tests available in the VME-based DAQ system are implemented in PTS and are functional, namely pedestal readback, noise measurement, scan of calibration signal strength to measure the gain, bandwidth scan and a deadtimeless scan. Results of deadtimeless scans from staves using PTS have been presented [7] in this conference. Figure 7(a) shows the main DAQ panel capable of executing

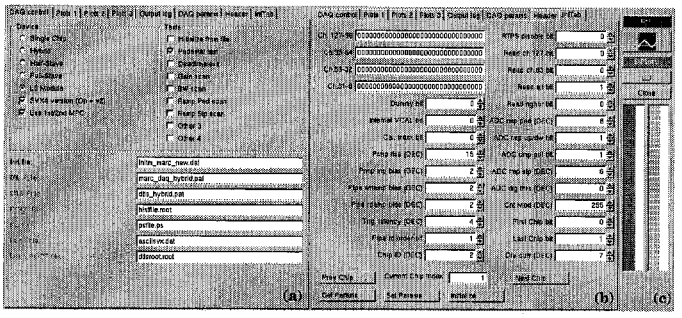

Fig. 7. ROOTXTL user interface showing (a) Main test panel, (b) Chip initialization panel and (c) global task button panel, aided with a pair of DAQ progress bars

multiple tests in a batch-like mode. Figures 7(b) and (c) show SVX4 chip initialization panel and a global task button panel, respectively. In Figure 8 results of a gain scan on an SVX4 chip is shown. In the upper graph average ADC counts are shown as a function of the input calibration voltage, set successively using a DAC, over the 128 channels of an SVX4 chip. The lower graph shows mean ADC counts averaged over all the channels. A fairly linear response is seen over most of the input voltage range.

Both VME DAQ and PTS save the acquired data into ASCII files in an identical gray-coded hexadecimal format. A set of ROOT-based GUI classes have been developed for a detailed analysis of the data, and more importantly, for cross-comparison of results from the two systems. Within statistical error, results from both the systems are found to be compatible.

VII. Conclusion

In this paper, we have compared design of the CDF Run IIa SVX detector with that of its proposed Run IIb successor and have outlined the upgrade path adopted for the VME DAQ

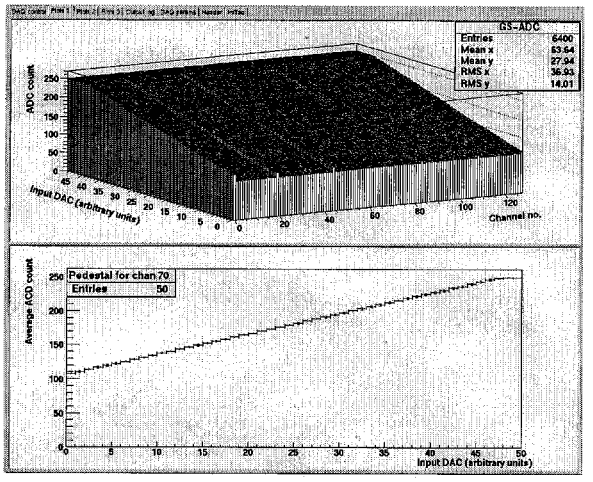

Fig. 8. Gain scan of an SVX4 chip. (a) average ADC counts as a function of input calibration voltage over 128 channels, (b) Y-projection showing ADC counts averaged over all the channels Vs. input voltage

system to meet requirements of the new environment. We have then explained implementation of these modifications involving changes at both the hardware and software levels of the DAQ system, emphasizing the components being upgraded. A test system is established incorporating all the upgraded components and found to work well with the SVXIIb detector components, thus meeting one of the foremost goals of the new system. A PCI-based DAQ system, developed to provide a simple testing ground for the silicon detector and DAQ components in the production phase, works well and features most of the functionalities of the VME-based full DAQ system.

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