SLAC-TN-70-22
September 1970
J.-L. Pellegrin

THRESHOLD AND DELAY CIRCUIT FOR PROPORTIONAL WIRE CHAMBER ELECTRONICS

ABSTRACT

This note describes the operation of a 4-channel module of electronics for proportional wire chambers. The circuit diagram is analyzed, and the measurements of all the parameters of interest are included.

Introduction

We present some test results obtained on a four channel module using emitter coupled logic (MECL II) elements. The instrumentation of each channel is made up of the usual amplifier-discriminator-delay-coincidence-latch combination; the data is available at standard TTL levels (0, +3V).

The principal characteristics of this circuit are the following:

- input sensitivity of 0.5 MV typical
- leading edge delay of 200 nsec, equalized on all channels within ±2.5 nsec; the delay temperature coefficient is 0.15% per ^{o}C
- output pulse width of 8 nsec typical
- time slewing of 12 nsec for signals of amplitude up to 40 dB above threshold
- adjacent channels crosstalk level larger than 100 MV.

In addition, the delay is completely independent of the input pulse width and is voltage adjustable. The four-channel module is particularly convenient for chambers with 2 mm wire spacing since its thickness does not exceed 8 mm. Data words of any multiple of 4 bits can be assembled with the proper external interconnections and OR-ing of the output lines (collector-wired OR).

Selection of the Amplifier Gain: Discriminator Sensitivity

A given minimum input signal and a given minimum discriminator sensitivity determine the required amplifier gain. We have tested (Fig. 1) a simple amplitude discriminator using a differential line receiver MC1020 and found a reliable 50% triggering threshold of 130 MV. This indicates that if the amplifier has a gain of about 200. The input sensitivity will be of the order of 0.65 MV. Such a gain can be implemented by cascading three MC1020 line receivers (gain of 6). Evidently, the advantage of using such a minimum gain is that a better rise time can be achieved as well as less noise and therefore less jitter of the output pulse.

The discriminator represented on Fig. 1 is of the "one shot" type rather than the Schmitt trigger type. Consequently, an output window wider than the input over-threshold width, and wider than the desired delay can be produced. Such a window prevents the delay multivibrator from being disturbed by the input pulse tail. Hence the discriminator leading edge only is of interest and the circuit is insensitive to the input pulse width.

Figure 2 shows the amplifier and discriminator circuit. Note that R1 establishes the amplifier operating point in the linear region. By varying R1, the threshold can be changed. Figure 3 represents a plot of the overall sensitivity obtained for different threshold values.

Operation of the Delay

In order to obtain a good stability of the monostable multivibrator which performs the delay function (Fig. 2), the timing capacitor is discharged toward as high a voltage as is practically possible, and the resistive path of the discharge is made independent of the transistor parameters.

The bias of the monostable is established by means of a diode which provides sufficient current for the circuit input; when a trigger is applied the diode becomes cut off, leaving the timing resistor as the only discharge path. By paralleling standard 5% resistor, the delay of all channels can be matched within ± 2.5 nsec. The temperature coefficient was measured for four channels and found to be about $0.15\%/^{\circ}C$ (Fig. 4).

Output Pulse, Time Slewing and Crosstalk

A narrow pulse can be obtained by differentiating the trailing edge of the monostable multivibrator output. A conventional MC1010 gate is used as an RC

feedback amplifier (Fig. 7) biased near the upper saturation level (-0.850 V); this arrangement provides a pulse 8 nsec wide and also rejects the leading edge differentiation.

This signal was found to be convenient to make a measurement of the circuit time slewing; the results are plotted on Fig. 5.

The crosstalk between adjacent channels was also evaluated using this pulse; the table of Fig. 6 indicates the maximum input pulse amplitude a channel can handle without triggering adjacent circuits.

Coincidence Gate and Latch

The remaining of each module instrumentation is straightforward; it is made up of a coincidence gate and a buffer implemented with MC1010 gates, a MECL to TTL level shifter and an open collector gate (Fig. 7). The reset and the read signals are at TTL levels.

The coincidence gate efficiency was tested using a gating signal of 15 nsec with a rise time and a fall time of 5 nsec. The curve obtained (Fig. 8) is consistent with the performance of Motorola emitter coupled integrated circuits.

Conclusion

The module we have described is built on a 4" × 4" board (Fig. 9); the total thickness does not exceed 8 mm, hence a chamber with 2 mm wire spacing can be instrumented with a stack of modules on one side of the chamber. A chamber with 1 mm wire spacing could use a stack at both ends.

All the circuit parameters we have measured are compatible with the present proportional wire chamber requirements. However the time slewing could be detrimental in some cases; since slewing is bandwidth dependent, it will be improved if the amplifier gain can be reduced, that is, if larger pulses can be obtained from the chambers.

Acknowledgement

The layout of these circuits is the result of a long term effort of Dick Carman; all tests have been conducted by Bob Partelow; their participation is gratefully acknowledged here.

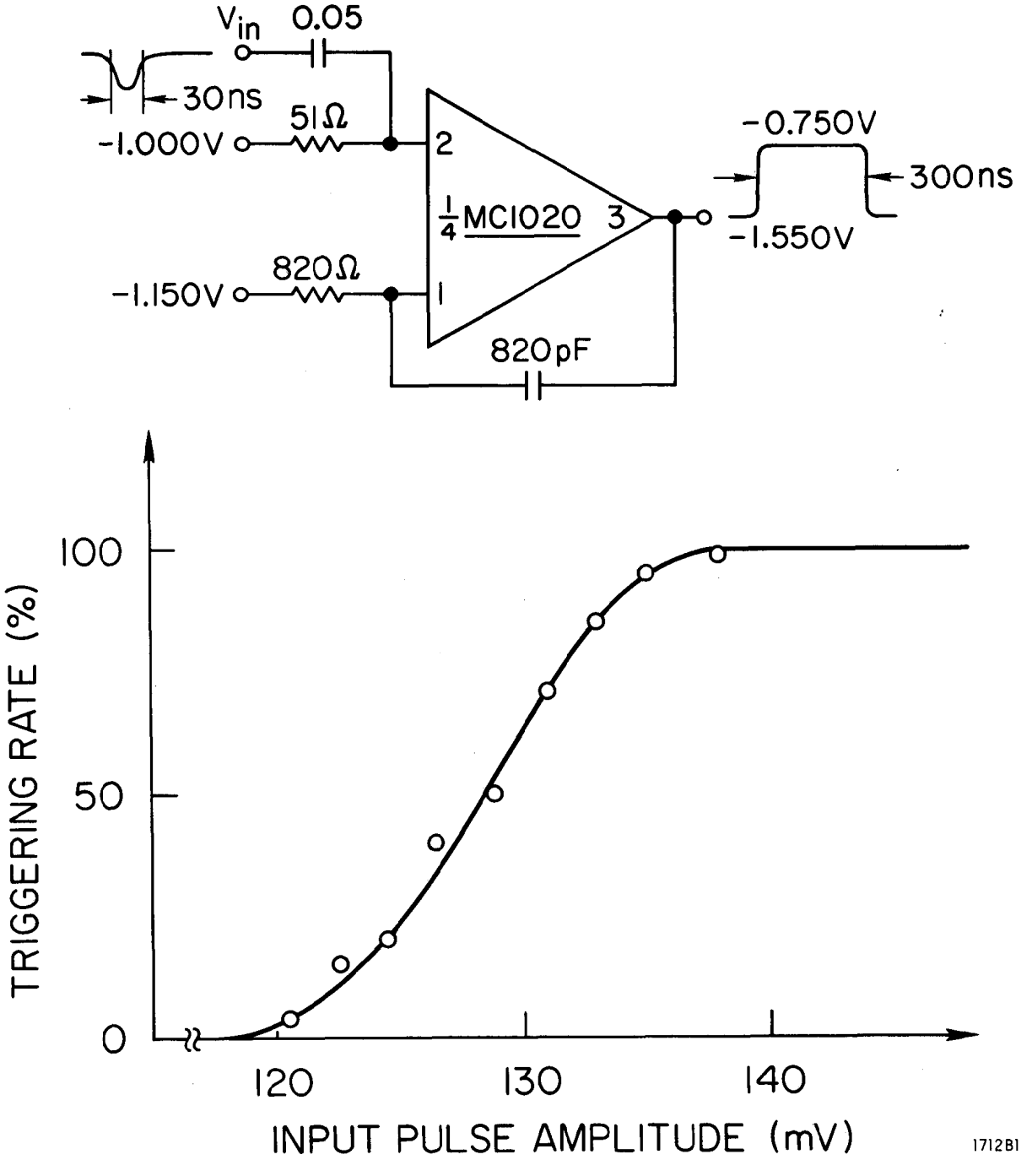


FIG. 1--Discriminator response; the output leading edge only is of interest.

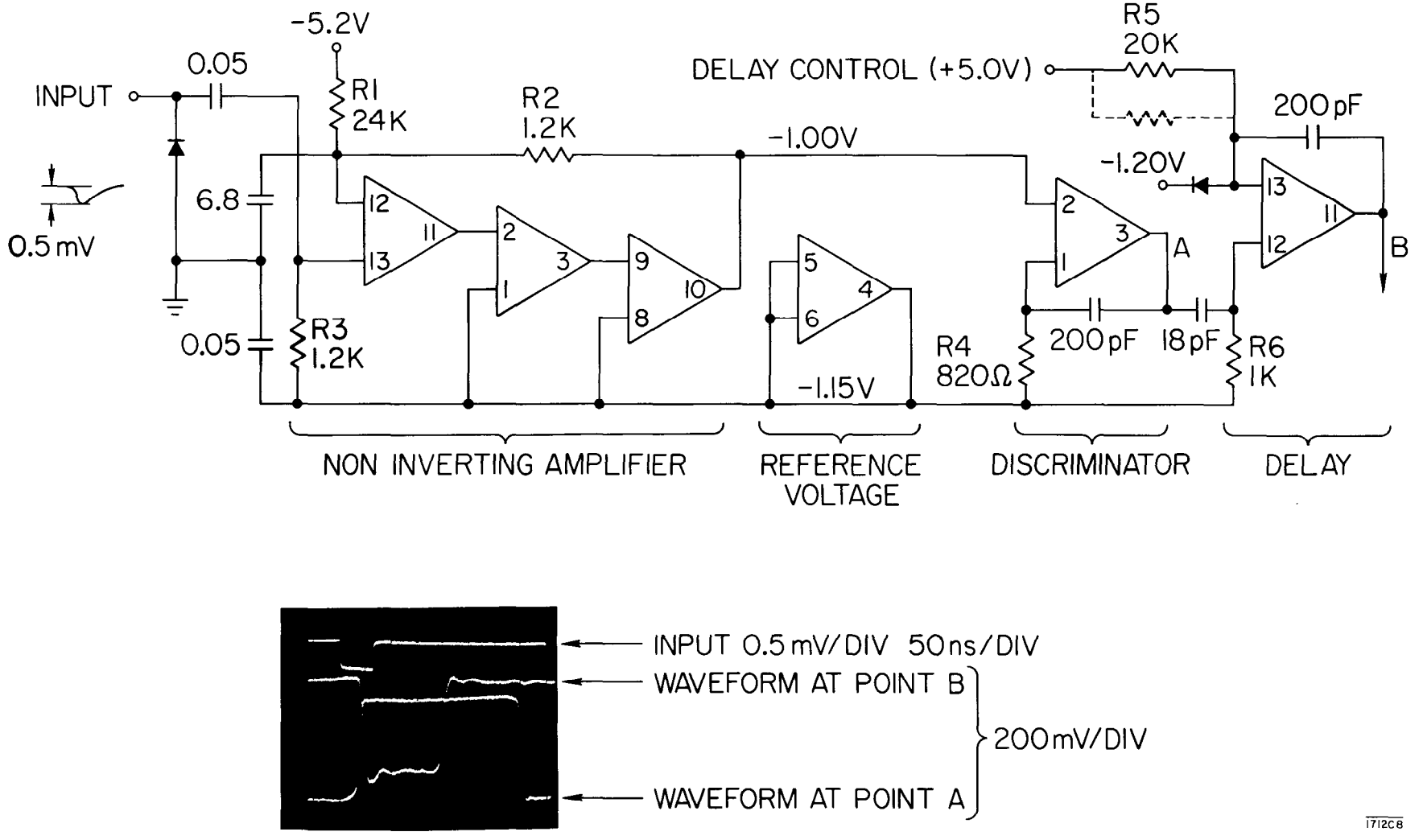


FIG. 2--Amplifier, discriminator, delay, circuit diagram.

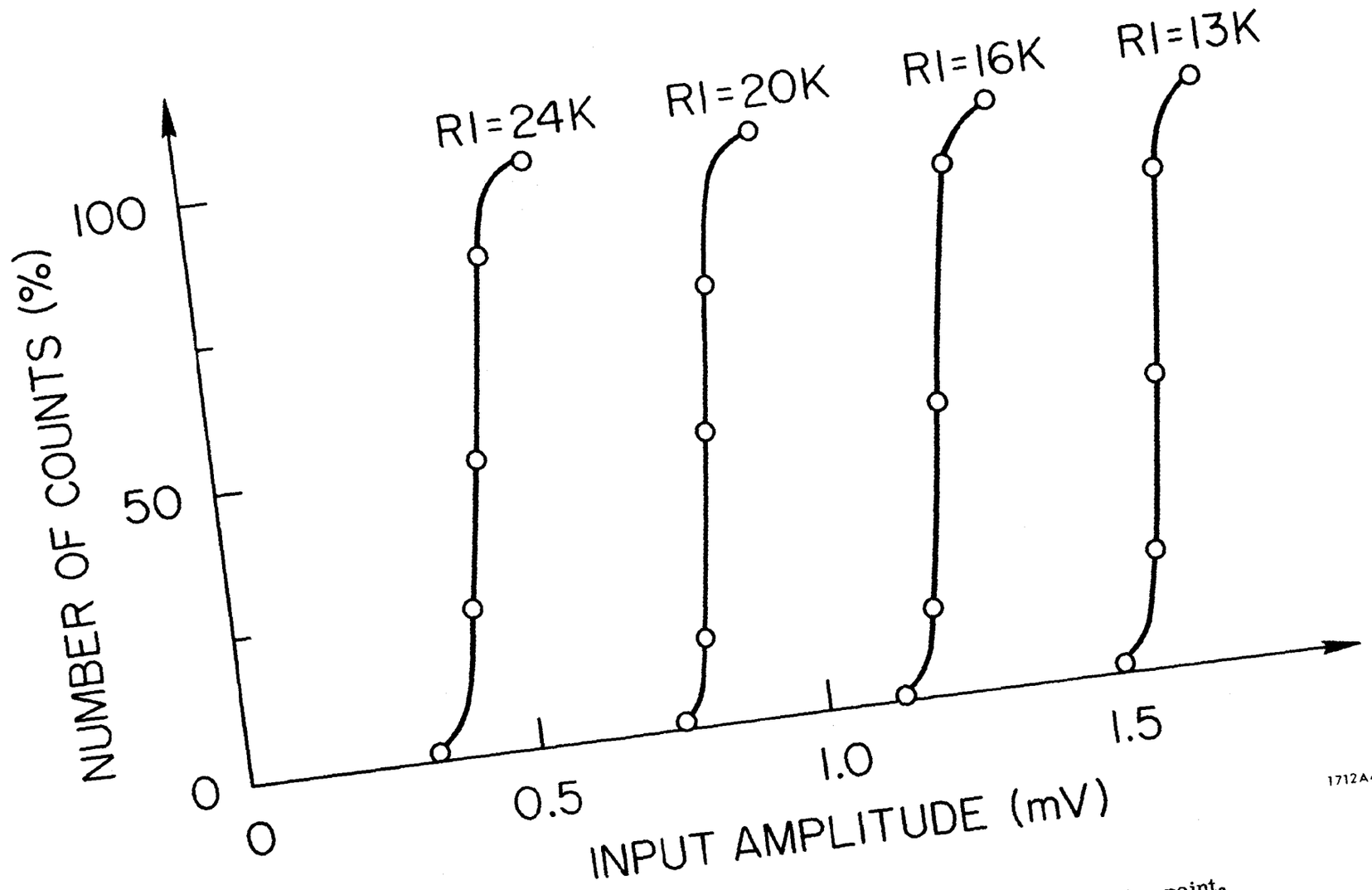


FIG. 3—Circuit threshold as a function of the amplifier operating point.

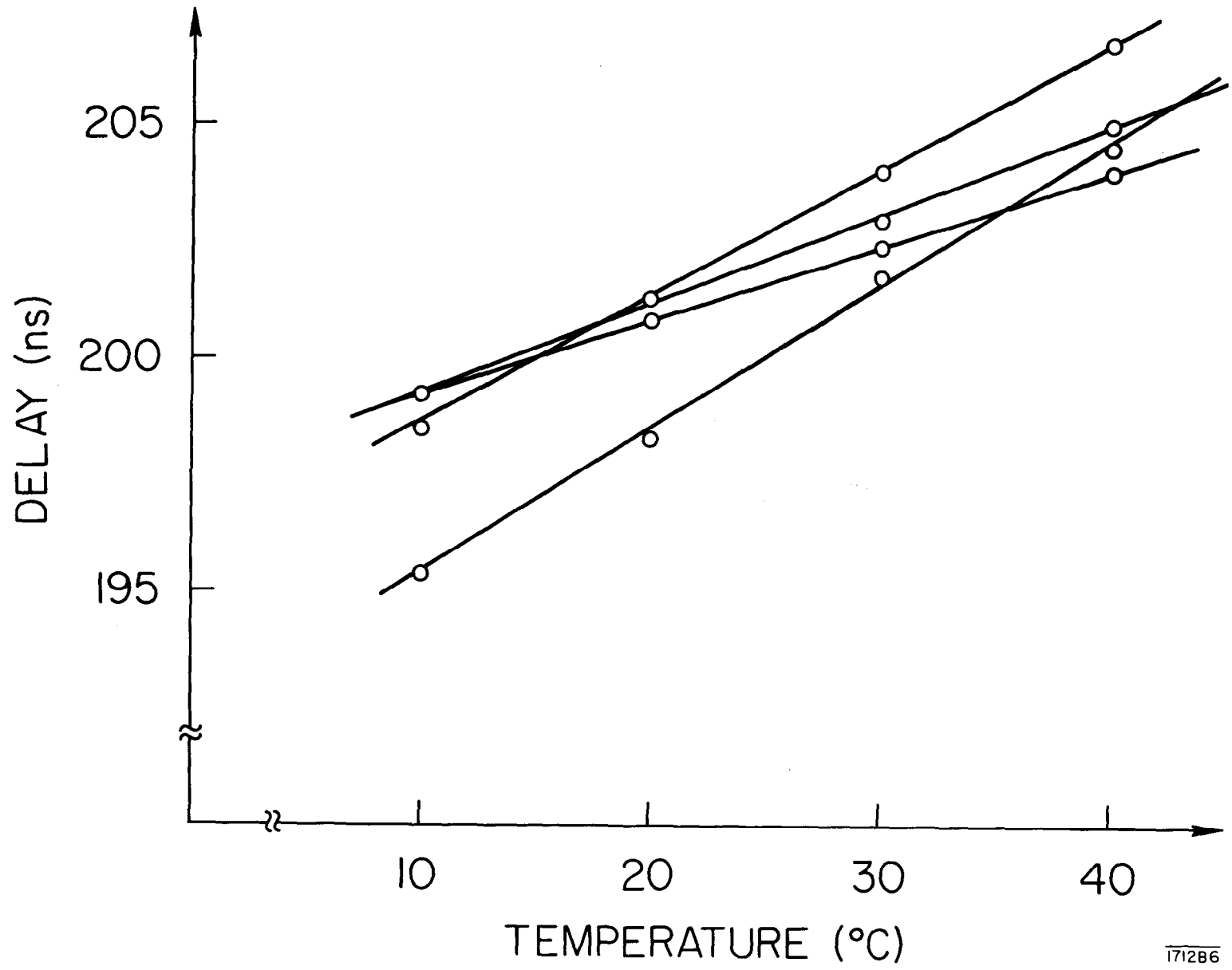


FIG. 4—Variation of delay with temperature.

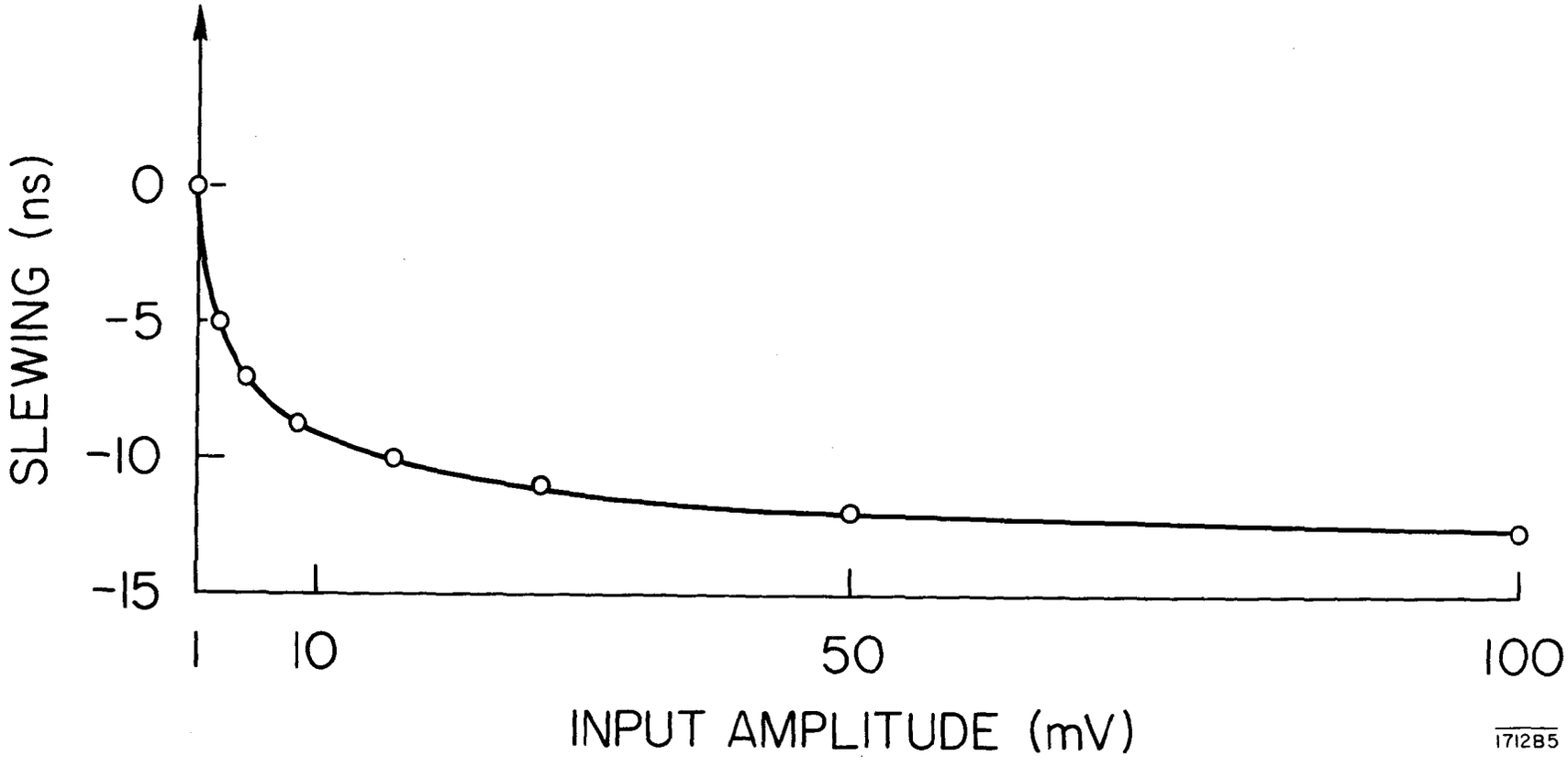


FIG. 5—Circuit time slewing.

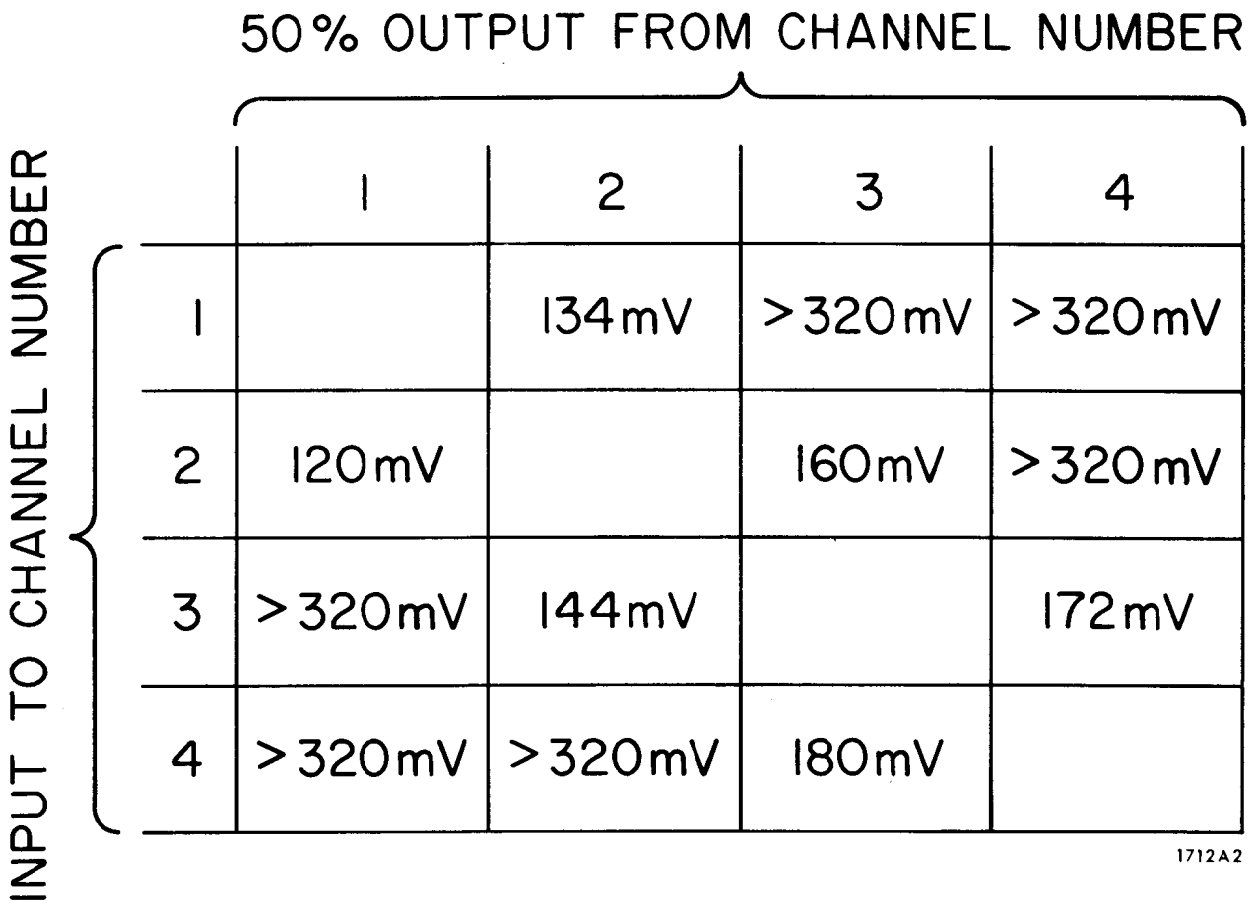


FIG. 6—Crosstalk between adjacent channels.

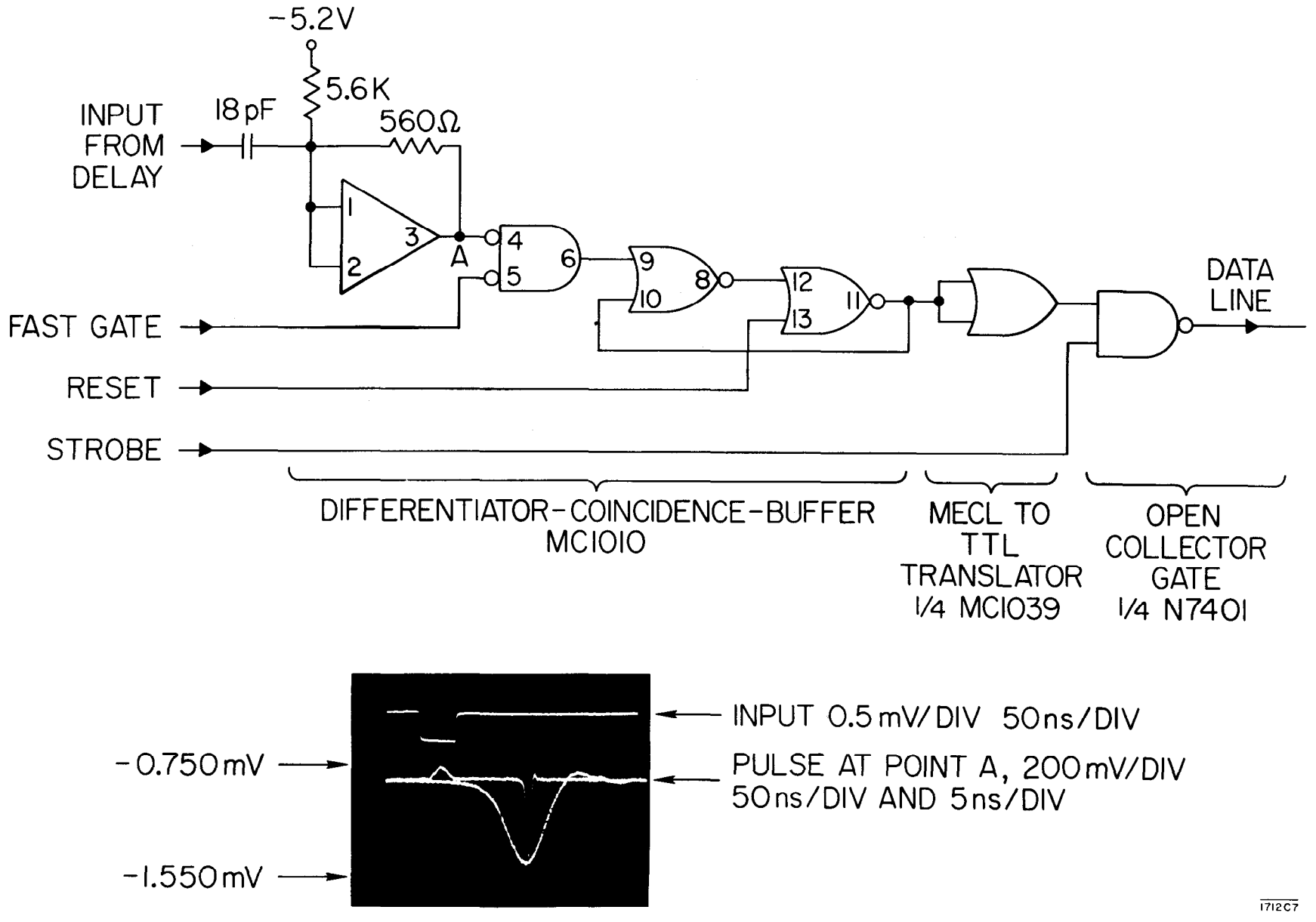


FIG. 7--Differentiator, coincidence gate and buffer circuit diagram.

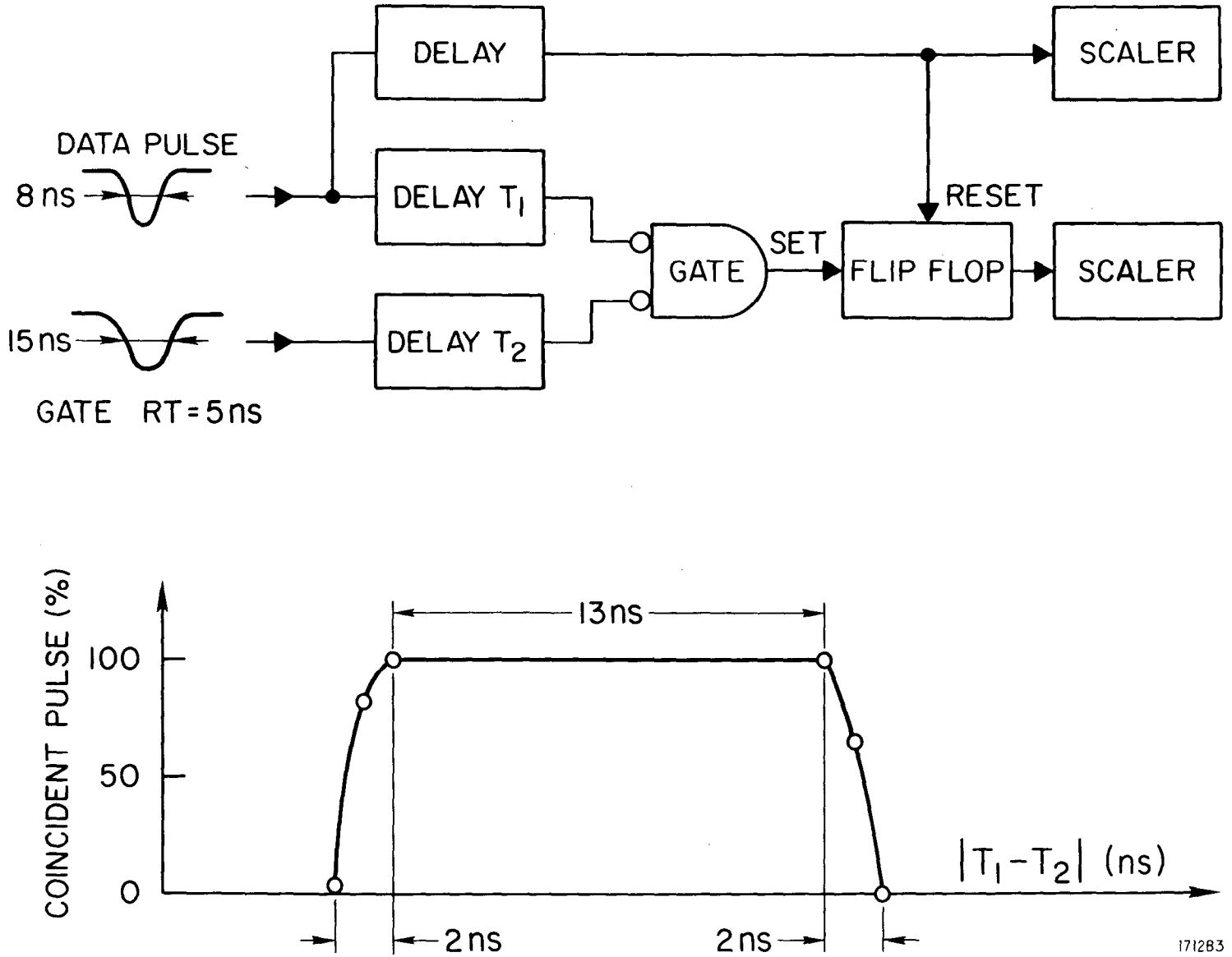


FIG. 8—Coincidence gate efficiency.

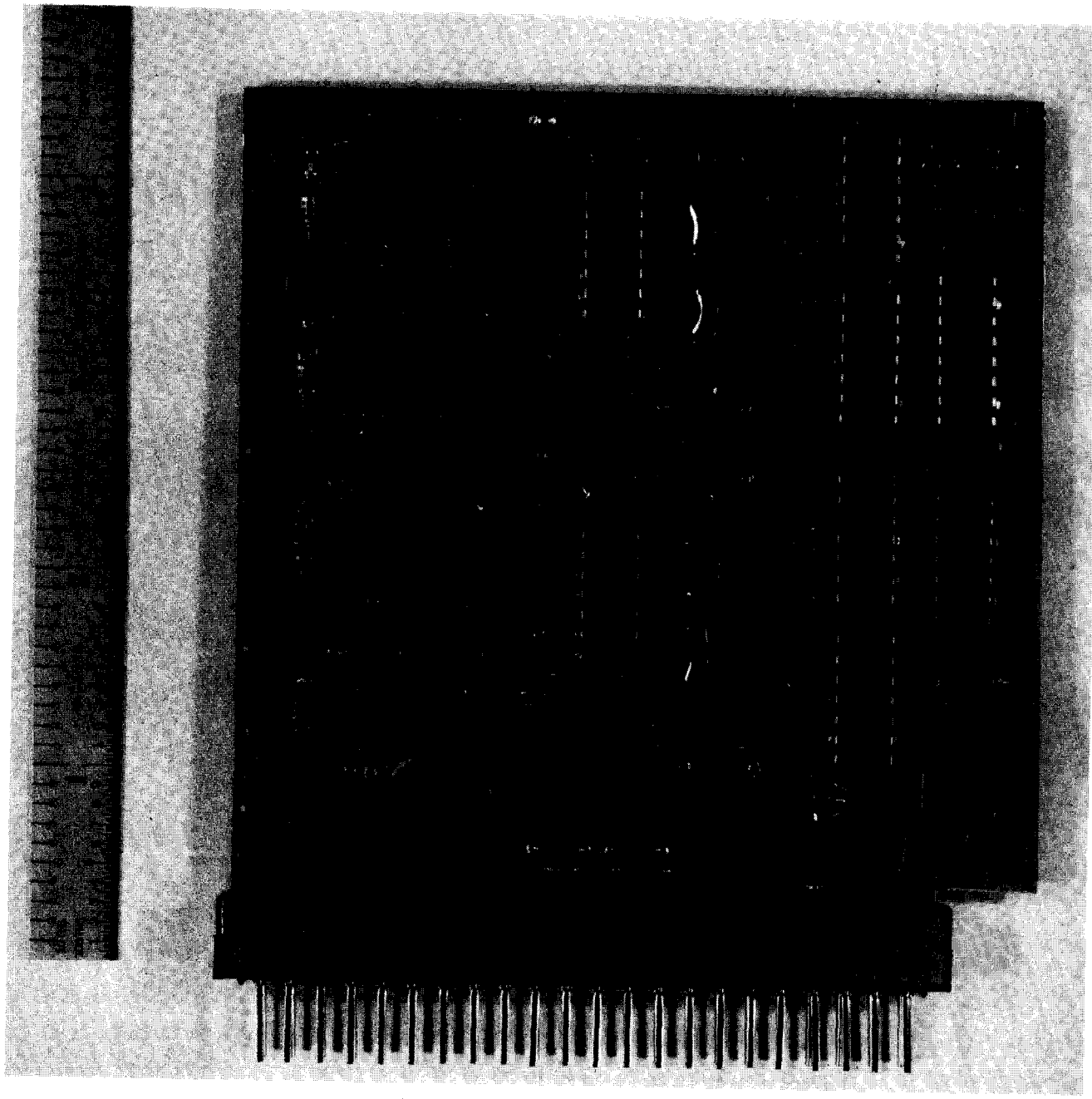
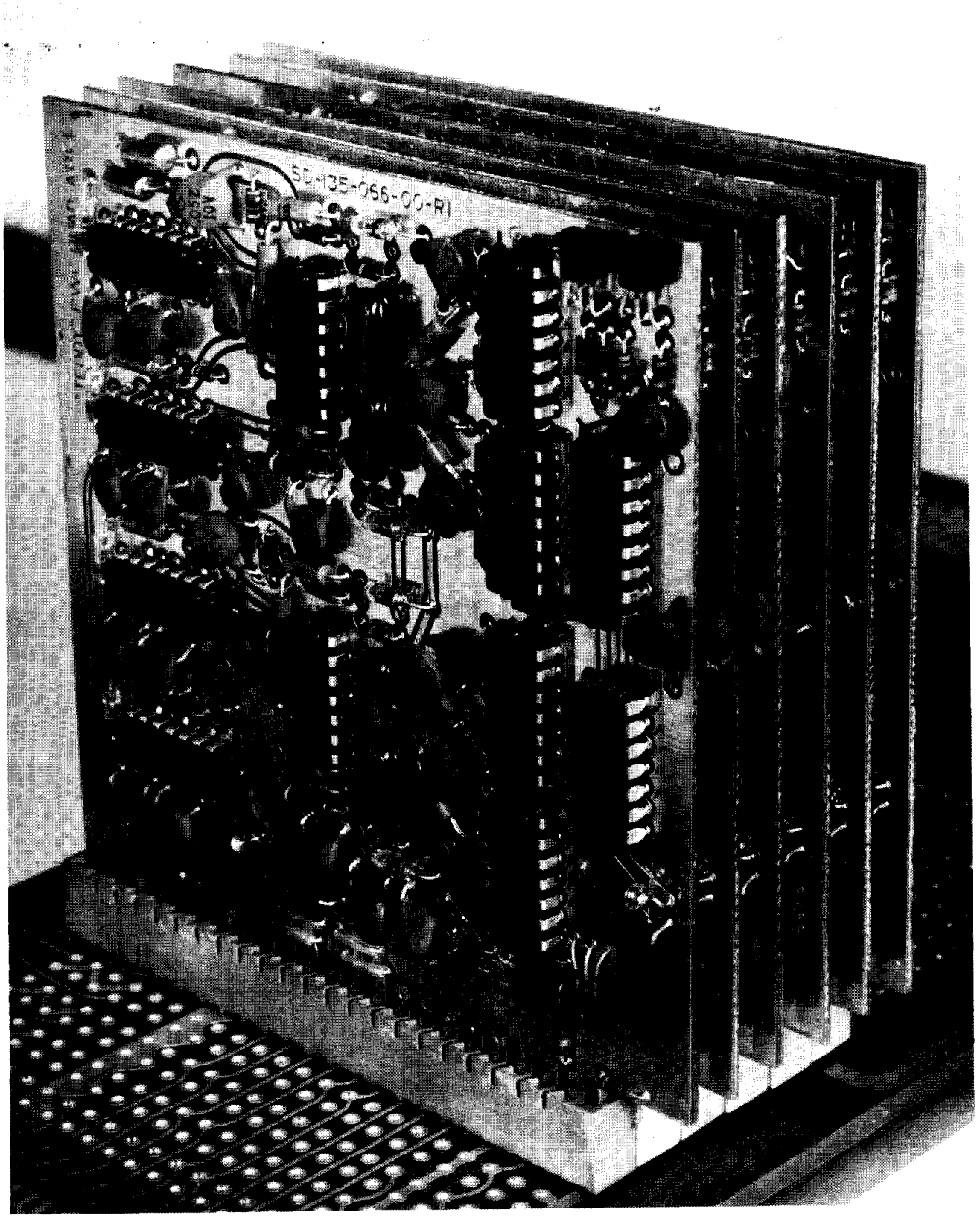


FIG. 9—Photograph of the four-channel module.

1712A9



1712A10