ANALOG SIGNAL PROCESSING FOR THE CMS ELECTROMAGNETIC CALORIMETER.

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I INTRODUCTION.

To accommodate the 16 bits dynamic range of the $PbWO_4$ crystal calorimeter of CMS in the 12 bits of a digital readout, a multi-gain switching topology is used along with a wide dynamic range transimpedance amplifier in front to convert capture the photocurrent signal of a pair of avalanche photodiode as shown in figure 1. As the trigger algorithms are digital, the readout chain must provide each 25 ns quantized data and therefore, sampling, switching and multiplexing process must be performed at a 40 MHz speed. As a result, the bipolar transistor device, known for its high performance in term of speed and gain, seems suitable to implement such functions. In addition the level of radiations (up to 2MRad and $5E^{13}$ n/cm^2) undergone by the electronics imposes the use of radiation hard technology containing bipolar devices.

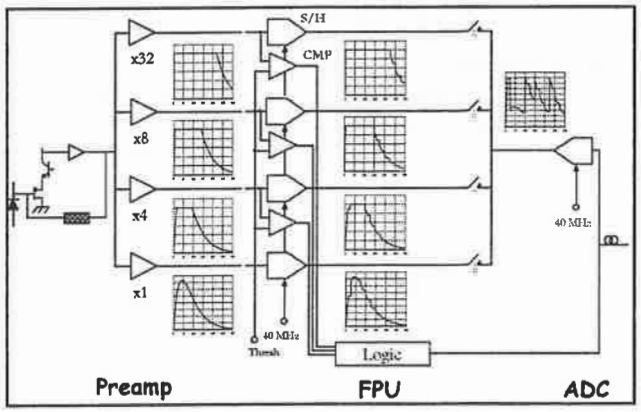

Figure1: Multi-gain switching topology.

To implement the readout chain depicted in figure 1 both BiCMOS and full complementary bipolar technology were investigated along with fitted design techniques. The paper is organised as follows. In section II, the design of the BiCMOS version is presented. Section III is devoted to results obtained on prototypes, while in section IV, the full complementary bipolar design is analysed. Finally, some concluding remarks will be given in section V.

II DESIGN OF THE BICMOS MULTI-GAIN PREAMPLIFIER.

As shown in figure 1, scintillation light from the crystal is converted into a photocurrent by the photodetector, and into a shaped voltage pulse by the preamplifier. The preamplifier has several outputs, each with different gains (1,4,8,32) and a constant bandwidth in order to keep the same delay at all outputs. A second circuit receives the four preamplifier outputs. A voltage value for each of the four inputs is captured every 25 ns by sample-and-hold circuits. Every 25 ns, voltage comparators and digital logic determine which of the "held" voltage values is the largest (highest gain) below a certain 'saturation threshold'. This value is multiplexed and digitized by a 12-bits ADC.

II.1 The preamplifier.

The schematic of the preamplifier [1] is shown in figure 2. This transimpedance amplifier design targets BiCMOS technology. As seen from the schematic, the passive R_fC_f network associated with the compensation capacitance C_c, along with the detector capacitance C_d and the transconductance gm_{M1} of the input stage performs the $(RC)^2$ shaping of the output pulse; therefore no additional shaping stage is needed. In addition, the compensation resistor Rz is used for internal pole-zero cancellation. Design modifications from the preamplifier presented in [1] were performed concerning the maximum input charge. In order to improve the photostatistic and the signal to noise ratio (degraded by leakage current of the photodetector) two avalanche photodiodes (APD) are put in parallel instead of one. Therefore, both the input charge, provided to the preamplifier, and the source capacitance C_d are doubled. The feedback resistor R_f should be halved and other passive components modified accordingly compared to the previous version.

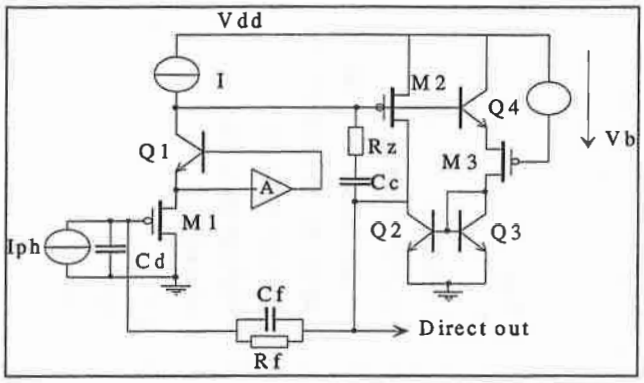

Figure2: Preamplifier schematic.

The full scale input charge is 64 pC, corresponding to a 2 TeV event and the source capacitance C_d is 250 pF (cable capacitance included). The main sources of noise come from the thermal noise of the input transistor M1, which gives an equivalent noise slope of 16e/pF, the feedback resistor R_f, with a noise contribution of 2700 electrons, the thermal noise of the amplifier labelled A, with an equivalent input noise resistor of 20Ω, and the class A/B stage (M2, M3, Q4, Q2, Q3) with an equivalent input noise resistor of 50Ω. All these contributions give a total noise of about 10000 electrons, referred to the input.

II.2) Voltage amplifiers.

Figure 3 is a simplified schematic of the voltage amplifier used to provide gains 1, 4, 8 and 32 between the preamplifier and the sample and hold stage.

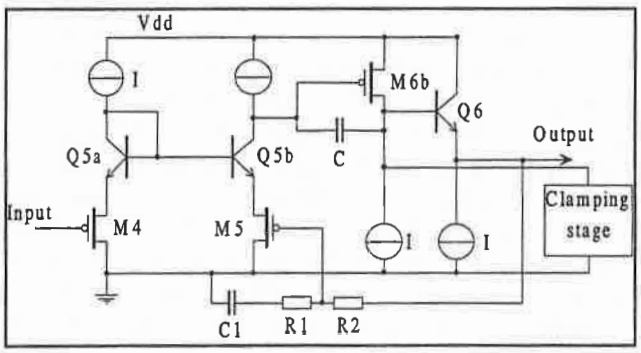

Figure3: Voltage amplifier schematic

A two stage topology was used for this design. The first stage is composed of M5 and Q5b along with a constant current voltage follower Q5a and M4. M4 and M5 are PMOS transistors biased closed to the weak inversion region at a 1mA current bias level. Their equivalent input noise resistor is 70Ω, suitable for a low noise design. The second stage is composed of a PMOS transistor M6b and Q6 which acts as an emitter follower, both biased at 1mA. The key feature of this amplifier is to have different voltage gains, keeping a constant bandwidth. This is mandatory for a precise pulse reconstruction and simplifies circuit calibration. The closed loop bandwidth of the amplifier is given by :

$$BW = \frac{gm_{Q5b}}{C}\frac{R_1}{(R_2+R_1)}$$

where gm_{Q5b} is the transconductance of Q_{5b}, C is the Miller capacitance and R1, R2, the feedback resistors. So for a given gain (1, 4, 8, 32), C is modified accordingly. Precise relative bandwidth could be achieved by capacitor ratios between amplifier. In addition, a clamping circuit is connected on the drain of M6b, avoiding saturation and long recovery time for large signals applied to the highest gain amplifier.

II.3 Sample and hold and multiplexer stages.

In CMOS switches, charge injection hampers the performance at these speeds, so the sample/hold and multiplexing functions are performed with current-switched amplifiers as shown in figure 4.

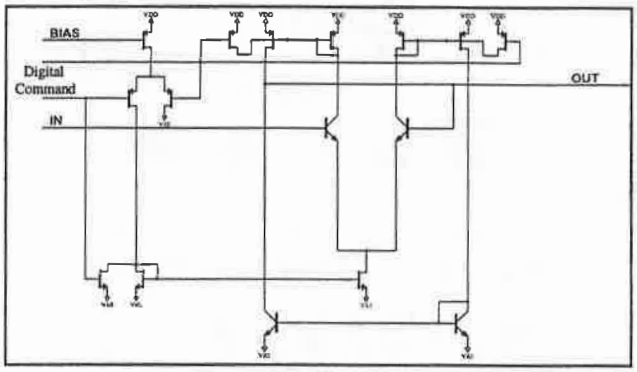

Figure4: Sample/hold and multiplexer schematic.

These amplifiers are configured as OTAs, with an NPN differential pair. The differential pairs are mirrored with PMOS transistors and the mirrored outputs are mirrored with NPN transistors. The amplifier output then charges the hold capacitor (5pF) not shown in this figure. The use of NPN transistors in the pair and mirror ensures that the amplifier switches off gracefully, so that the held signal is not perturbed. In addition, clamping transistors are connected on gates of MOS current mirrors to bleed off charge when switching.

II.4 Clocks and digital logic.

Two clocks, each at 40MHz are employed. The sample/hold clock controls the sample/ hold transitions, and a second clock controls the logic which determine the multiplexer output. All clock input circuitry is implemented with ECL logic cells, while conventional CMOS logic is used for the remaining digital functions.

III RESULTS OBTAINED ON PROTOTYPES.

Both transimpedance amplifier and multi-gain switching circuit, called floating point unit (FPU) were produced in AMS BiCMOS 0.8µm technology [2]. The layout of these circuits are respectively shown in figure 5 and figure 6.

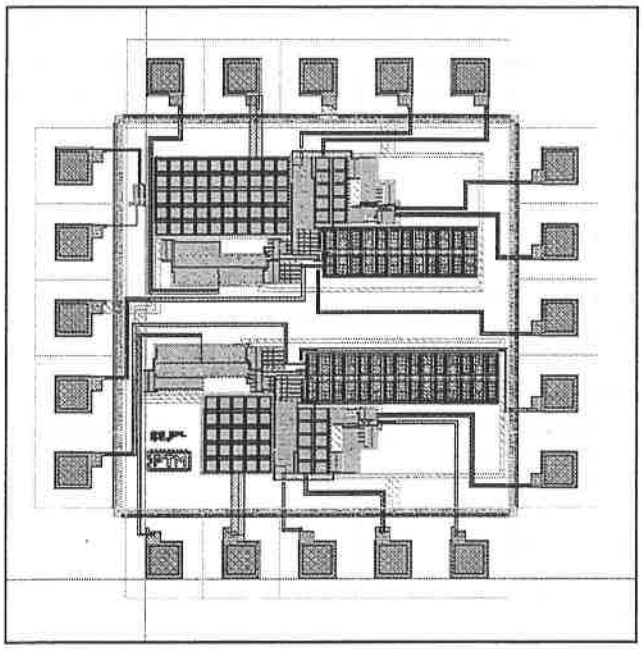

Figure5: Layout of the preamplifier (AMS).

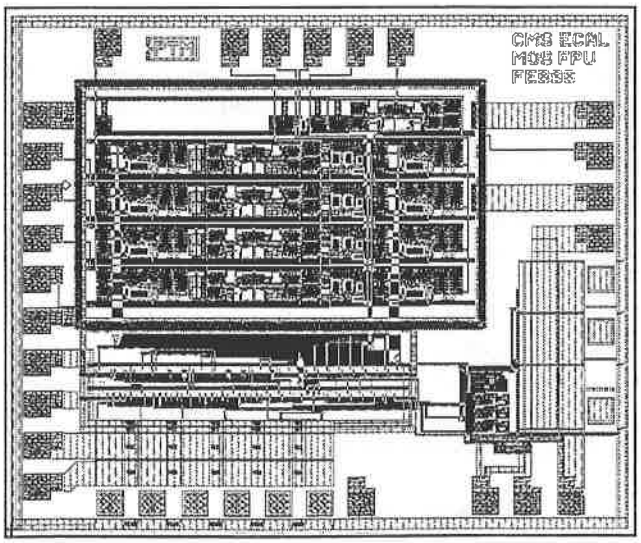

Figure6: Layout of the FPU (AMS).

Functionality tests were performed both in lab and in test beam. Figure 7 shows the measured noise dispersion of 40 transimpedance amplifiers for a total input capacitance of 250 pF. The mean value of 11600e is a bit higher than simulated because the value of the resistor Rz (see figure 2) was higher than expected. The total power consumption of the preamplifier is 80mW.

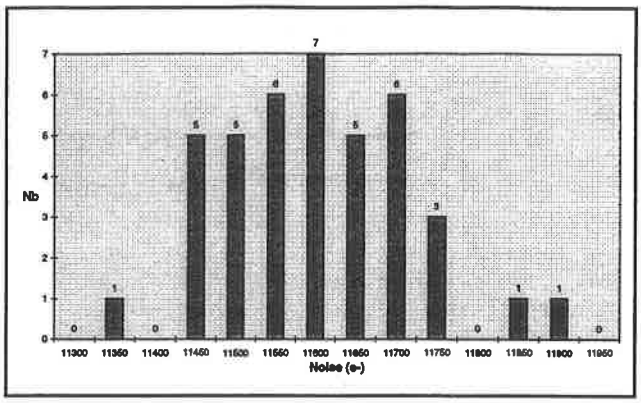

Figure7: Noise dispersion on 40 preamplifier prototypes.

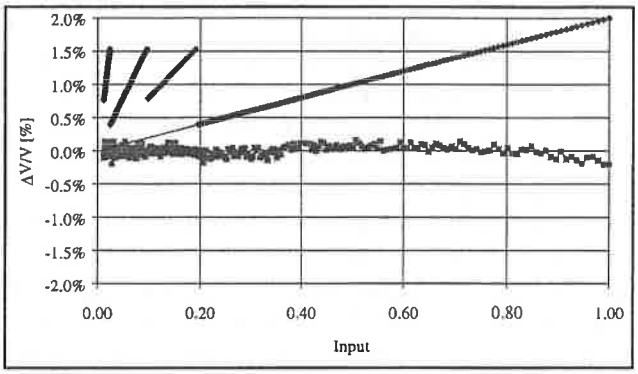

Figure8: Non linearity of the FPU.

Figure 8 shows the linearity tested in lab of the FPU, using a 40 MHz clock and a low frequency ramping signal at the input (<100KHz). A non linearity of 0.08% was measured. Preamplifier and FPU were also tested in H4 beam at Cern on a 36 channels crystal matrix (proto 97). Chip-on-board technology was used to realise this prototype along with encapsulated AD 9042 ADC for analog-digital conversion. Figure 9 shows the digitized output pulse for a 120 GeV electron beam. The upper part corresponds to raw data showing a change in range from the X32 gain output to the X8 gain output. The lower part shows the reconstructed pulse. The total power consumption for both analog and digital part is 150mW each. Test chips in BiCMOS DMILL technology containing a transimpedance amplifier matched for one APD (120pF) along with a FPU test slice (the complete analog chain for one channel) were submitted in 96. Both the preamplifier and FPU functionality have been tested to doses exceeding 2.10^{14}n/cm^2 and 100 kGy with no observed detrimental effects (no statistically significant change in noise or peaking time in the preamplifier or sample/hold performance in the FPU).

New versions of preamplifier and a complete FPU (6 analog channels and digital part) were submitted in March 98 and will be tested soon. Two supplementary analog channels were incorporated to readout the APD leakage current and temperature through the FPU data channel.

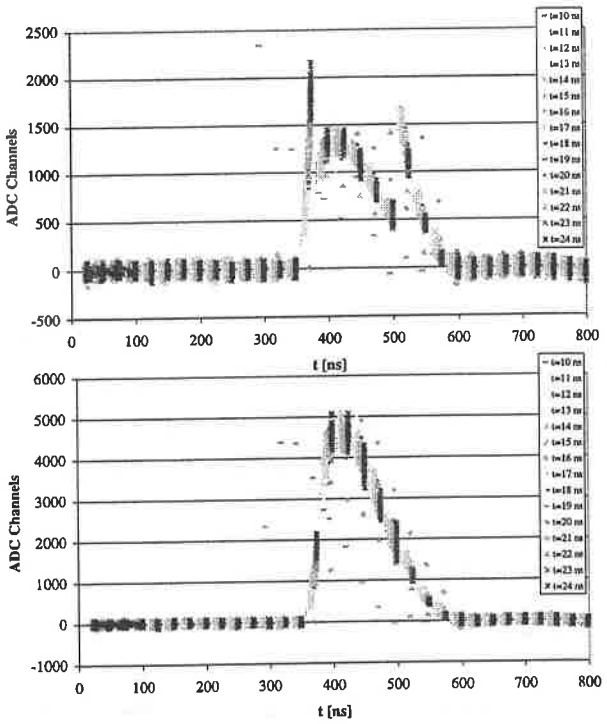

Figure9: Pulse reconstruction of a 120 GeV electron beam signal.

IV FULL COMPLEMENTARY BIPOLAR DESIGN.

Present rad-hard bipolar technologies (up to 3MRad and $5E^{13}n/cm^2$) offer the possibility of designing analog circuits with high f_T NPN and PNP transistors along with integrated high performance passive components. Consequently, we have also undertaken the design of a complete floating point preamplifier in UHF1X process of Harris. We kept the same topology as shown in figure 1 and the following subsections will describe the main part of this design.

IV.1 Transimpedance amplifier.

The schematic of the bipolar transimpedance amplifier is depicted in figure 10. The topology is similar to the BiCMOS counterpart. The input PNP transistor was chosen to have a low base resistor value (rbb') and the highest current gain β. Degenerating resistor Rd was added to improve linearity. Compared to the BiCMOS preamplifier, the input PNP transistor exhibits two main sources of noise, one due to the base current I_B and the other due to collector current I_C. The contribution of them to the total noise is given by :

$$ENC^2 = \frac{2qI_C\tau}{\beta} + \frac{4kT}{\tau}\left(\frac{kT}{2qI_C}\right)\left(C_d + C_f\right)^2$$

where τ is the shaping time constant, C_f and C_d are respectively the feedback and detector capacitance. By taking the derivative of the previous equation with respect to I_C, the optimal collector current is obtained :

$$I_{Copt} = \left(C_f + C_d\right)\frac{kT}{q\tau}\sqrt{\beta} \cong 1.4mA$$

for $C_d = 250pF, C_f = 22pF$, $\beta = 60$, $\tau = 40$ns.

As a result, a total noise of 9000 electrons is obtained (simulation) including the contribution of all sources of noise. The emitter follower Q4, used as level shifter, also increases the input impedance of the class A/B stage.

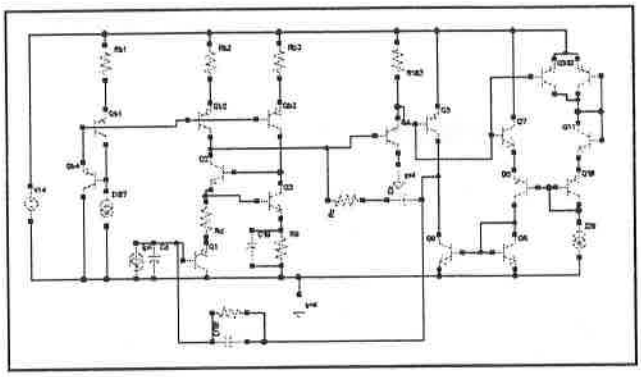

Figure10 : Bipolar preamplifier schematic.

IV.2 Voltage amplifiers.

In order to benefit from the high performance of NPN and PNP, a symetrical architecture like the one used in current feedback amplifier was chosen to implement voltage amplifiers providing the X1, X4, X8, X32 gains (figure 11). As a constant bandwidth is required (see II.2), the same technique of capacitor ratios was adopted. The bandwidth of this current feedback amplifier is given by [3] :

$$BW = \frac{1}{2\pi R_2 C}$$

As the resistor R1 should have a low and fixed value to lower the noise, the resistor R2 and the loading capacitor C is changed accordingly in order to have a constant bandwidth (~50MHz) and four different gains. The simulated noise level is 20μV at the output and remains negligible compared to the total noise of the preamplifier except for the X1 amplifier with a noise level of 45μV. This higher value does not degrade the performance since the resolution of the system is independant of electronic noise for high energy signals. A clamping circuit was also added to prevent saturation and long recovering time for high level signals.

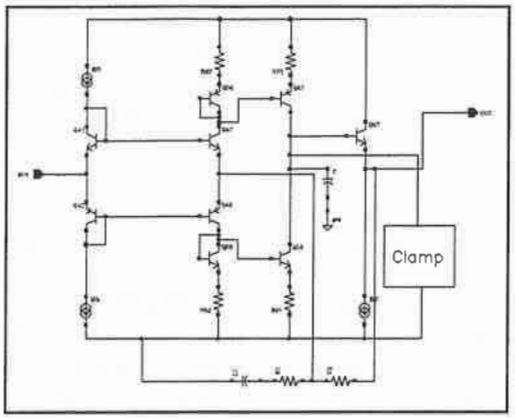

Figure11 : Bipolar voltage amplifier schematic

IV.3 Sample/hold and multiplexer stage.

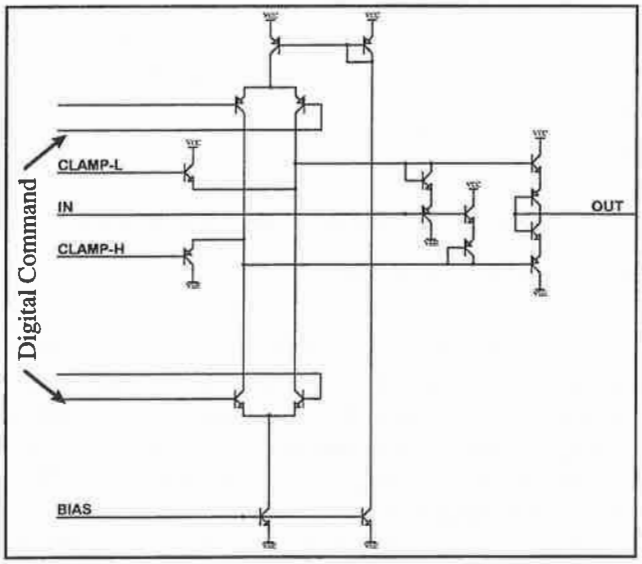

Figure12 : Bipolar sample/hold and multiplexer stage.

The schematic of the sample/hold and multiplexer stage is shown in figure 12. A symetrical switched emitter follower architecture was employed to realise both functions. Digital controlled differential pairs turn on and off unity gain transistors, each 25 ns. A non-linearity of 0.1% is achieved for signal swing equals to power supply rails minus 5V. In addition, clamping transistors were incorporated to improve speed. As a result, figure 13 shows a full scale simulated sample/hold signal superimposed with the continuous signal coming from the preamplifier. As the 12 bits ADC [4], connected at the output of the chip, require a 1V swing within a 1.9V to 2.9V voltage range and is DC coupled, a on-chip buffer, implementing a 0.5 gain function and capable of sinking 2mA in quiescent condition, was designed, based on symetrical current feedback followed by emitter followers architecture [5].

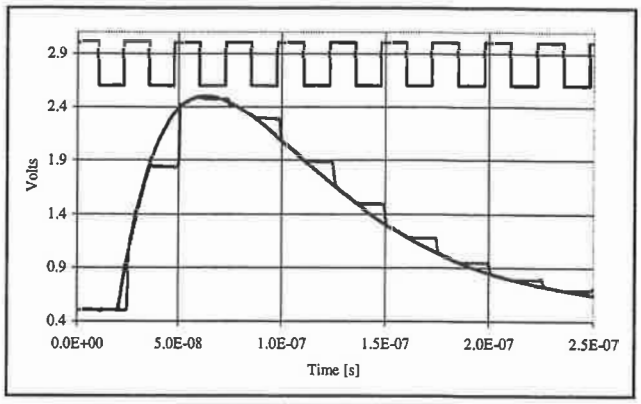

Figure13 : Simulated sample/hold signal.

All the digital logic of the FPU was implemented in CML, trade-off between speed and static power consumption. This design will be submitted to fabrication soon and will be tested next year.

V Conclusion.

A multi-gain switching topology was used to accommodate the 16 bits dynamic range required by the electromagnetic calorimeter of CMS into a 12 bits digital readout. Two design approaches for implementing such a function based on two different technologies, either BiCMOS or full complementary bipolar is described. For the preamplifier part, no major change in architecture or in design constraints appears between the two technologies, except for the input transistor.

On the other hand, switched OTAs design techniques for sampling and multiplexing was used for BiCMOS while symetrical switched emitter follower seems more better adapted for bipolar. Rad hard DMILL BiCMOS design has already shown good performances under irradiation. The analyses and design principles of the bipolar counterpart will be verified under irradiation next year.

REFERENCES

[1] High Dynamic Range and Low Power Very-Front-End Preamplifier for CMS Calorimetry, J-P Walder, Second Workshop on Electronics for LHC Experiments, Balatonfüred, September 1996, p. 61.

[2] CMS electromagnetic calorimeter readout, Peter Denes, Second Workshop on Electronics for LHC Experiments, Balatonfüred, September 1996, p 48.

[3] Analog Functional Blocks, W Sansen, Advanced engineering Course on CMOS and BiCMOS IC Design 97, EPFL Lausanne 1997.

[4] AD9042 Analog Devices data sheet REV A.

[5] Current feedback amplifier, Theory and applications, R Mancini, J Lies, Harris semiconductor, Application note n° AN9420.1 April 1995.