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Study of Indium and Solder Bumps for the BTeV Pixel Detector

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Abstract-- **The pixel detector proposed for the BTeV experiment at the Fermilab Tevatron will use bump-bonding technology based on either Indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. We have studied the strength of the bumps by visual inspection of the bumps bonding silicon sensor modules to dummy chips made out of glass. The studies were done before and after thermal cycles, exposed to intense irradiation, and with the assemblies glued to a graphite substrate. We have also carried out studies on effects of temperature changes on both types of bump bonds by observing the responses of single-chip pixel detectors to an Sr^{90} source. We report the results from these studies and our plan to measure the effect of cryogenic temperatures on the bumps.**

I. Introduction

PIXEL detectors proposed for the new generation of hadron collider experiments will use bump-bonding technology based on either indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. One of these experiments is BTeV at the Fermilab Tevatron. The pixel module is the basic building block of the pixel detector. Each module consists of a single sensor that is bump bonded to a number of readout chips. The total active area of the BTeV pixel detector is about $0.5m^2$ and the total number of pixels will be 23 million, each measuring 50 μm x 400 μm. The modules are supported by a graphite substrate that also provides cooling for the readout chips. Nominally, the pixel detector will be placed at 6 mm from the colliding beams and will be exposed to significant radiation. To keep the detectors in operation for 10 years, it will be operated at a temperature of -5 to $-10\ ^{o}C$. The bump bonds provide both the electrical and mechanical connection between the sensors and the readout chips and are crucial to the assembly and operation of the pixel detector.

The bump bonding technology has to meet the following requirements:

1. Fine bump pitch of 50 μm in the narrow dimension
2. Small bump size, typically 25 μm or smaller in diameter
3. High density, about 5000 bumps/cm^2
4. No thermal cycling effects
5. No loss in strength and connectivity after irradiation

We have previously reported large-scale tests of the yield using both indium and Pb/Sn solder bumps [1]. The conclusion is that both seem to be viable for pixel detectors. We have also carried out studies of various effects (e.g. storage over long period, effect of heating and cooling, and radiation) on both types of bump bonds using daisy-chained parts on a small scale [2]. Overall, these tests showed little changes in the integrity of the bump connections. Nevertheless, questions still remain on the long-term reliability of the bumps due to thermal cycle effects, attachment to a substrate with a different coefficient of thermal expansion (CTE), and radiation.

II. Silicon-Glass Modules

We have two modules, named AIT_1 and AIT_2, each with eight glass chips. They are indium bump bonded to ATLAS tile sensors [3] by AIT (Advanced Interconnect Technologies, Hong Kong). Each chip contains 2934 bumps. Four more modules, each with eight glass chips solder bump-bonded to the ATLAS sensors by MCNC (Research Triangle Park, North Carolina), are named MCNC_1, 2, 3, and 4. Each chip in these modules contains 3060 bumps. We video-scanned these modules before and after every test stages they have gone through and recorded the data on 8 mm tapes and DVD+RW's. The coordinate information from the DAQ was superimposed onto the video image so that we could compare the images before and after any procedure. While having the ability of visually inspecting the changes taking place on these modules, it has to be noted that the bonding was between glass and silicon, and not silicon and silicon, as will be the case in real experiment. The CTE mismatch between silicon and glass, and the possible difference in adhesion of under bump metallization (UBM) to glass were to be considered in the interpretations of the results.

The MCNC modules have gone through the following test procedures:

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1. All: 6 cycles of 16 hours at –25C° and 4 hours at room temperature,
2. 1 & 2: Irradiated to 13 MRad (using Co^{60}),
   3 & 4: 20 cycles of 10 hours at –25C° and 2 hours at room temperature,
3. All: 30 cycles of 6 hours at –25C° and 1 hour at room temperature,
4. 1 & 3 glued on a Thermal Pyrolytic Graphite (TPG) substrate. All: 105 cycles of 1 hour at –10C° and 1 minute at room temperature (Rapid Thermal Cycling)

The AIT modules have gone through the following test procedures:

1. Both: 5 cycles of 10 hours at –10° C and 4 hours at room temperature,
2. AIT_2 glued on TPG. Both: 105 cycles of 1 hour at –10C° and 1 minute at room temperature.

A. AIT Modules

Fig. 1 shows actual and schematic views of indium bumps. The dark circle in the center is the UBM. The indium bump, which is a cylindrical shell, appears as a light ring adhered to the glass. We observed that the indium at some of the bumps degenerated during thermal cycling. Fig. 2 shows two such bumps before and after each of the two thermal cycles. Degeneration progresses in one bump from one cycle to another. Some bumps had this degeneration before any thermal cycling. Table I lists the count of such degenerated bumps before and after each cycle. While the bump bonds remain intact, this effect might cause a change in capacitance of the corresponding electronics channel resulting a noisy readout.

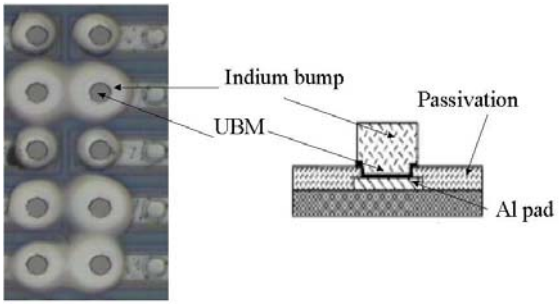

Fig. 1: Indium bumps

We also observed that the glass chips shifted around during thermal cycling. In Fig. 3 we show one corner of the first chip on AIT_1. The inset in each picture indicates the procedure for which the image is taken. Locations of the bumps relative to the structure on the sensors clearly indicate the shift. By studying the other corners of this chip, we concluded that it was originally misaligned during the flip-chip mating process. It then moved sideways about 50 μm and rotated counter- clockwise during the first thermal cycling. During the second cycle, it shifted back to almost its original position with a slight clockwise rotation.

The glass chips on the other module, which was glued to TPG before the second thermal cycling did not shift at all, indicating that the CTE mismatch between the TPG and the silicon did not matter in this case.

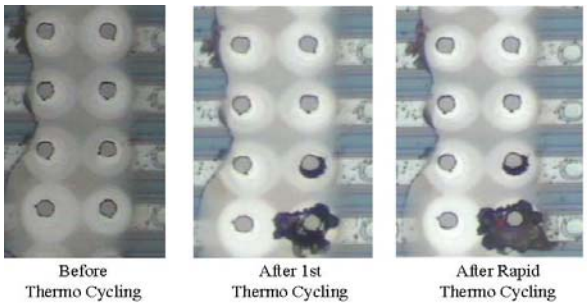

Fig. 2: Degeneration at indium bumps

TABLE I. COUNT OF DEGENERATED INDIUM BUMPS

	Existed Before T-Cycling	Created During 1st T-Cycling	Created During Rapid T-Cycling
AIT_1	225 (0.96%)	23	95
AIT_2	255 (1.1%)	28	69

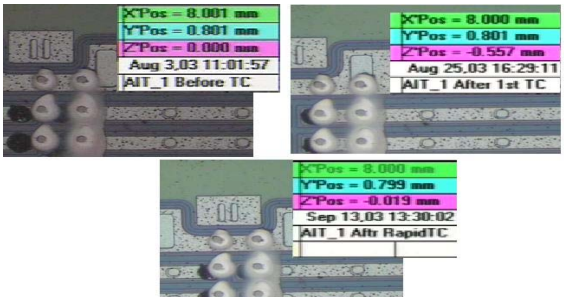

Fig. 3: Location of one corner of a chip

B. MCNC Modules

Fig. 4 shows actual and schematic views of the solder bumps in these modules. The manufacturer used a chemical product called BCB (Benzocyclobutene) for plating and it remained over the UBM. The UBM and the BCB cover the center and the walls of the via and extends over the flat passivation layer. At the center of the via, the light is reflected up, but not on the walls of the via. This forms the bright circle in the middle and the first dark ring. The light is reflected on the flat part of the UBM again, forming the bright ring. The last dark ring is the solder bump, which is a cylindrical shell.

We observed in some of these bumps that the first dark ring changed color to blend into the bright circle at the center.

Fig. 5 illustrates this color blending. It occurred on ~2% of the bumps as received mostly on the chip edges. The new occurrences appeared with the second thermal cycling and the irradiation processes. One disappeared during the rapid thermal cycling. Table II shows the counts of new occurrences after each step. The module MCNC_1 is excluded because it was partially damaged during the flip-chip assembly.

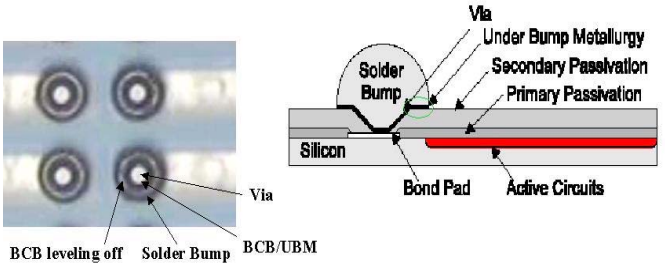

Fig. 4: Solder bumps

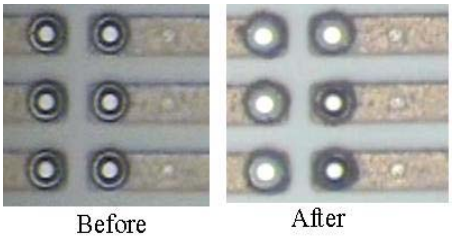

Fig. 5: Color blending of first dark ring

TABLE II. COUNT OF NEW OCCURRENCES OF FIRST RING COLOR BLENDING

MCNC Module	After 1st Cycling	After Radiation	After 2nd Cycling	After 3rd Cycling	After Rapid Cycling
2	0	124	N/A	0	7
3	0	N/A	93	16	99
4	0	N/A	0	3	-1

A possible explanation to this is as follows: The BCB is lifting off on the walls of the via (because of change in temperature) and partially reflecting the light causing the color blending. In one case, the BCB shrinks back to re-create the dark ring. This phenomenon, occurring on electrically insensitive part of the bump, should not cause any problem to the electrical characteristics of the bump.

The other phenomenon that we observed in some of the bumps is the development of dark extrusions as shown in Fig. 6. These also begin to appear during the second thermal cycling and after the irradiation processes at a rate of ~ 50 per module. They seem to be on the surface (glass side) and mostly on the edge bumps of the chips. The vendor suggested they might be due to ionic contamination (BCB originated), not completely removed during final cleaning.

We are still investigating with the vendors on the causes of these observed changes. While the bonds seem to remain intact despite these changes, we will do a pull test to study these bumps. We did not observe on these modules any shift of the glass chips due to thermal cycling or any effect after gluing to the TPG.

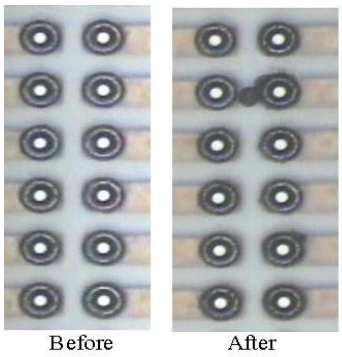

Fig. 6: Extrusion developing at solder bumps

III. SINGLE CHIP HYBRID

We studied the temperature dependence of the operation characteristics of the pixel detector at temperatures below and above room temperatures. For this study, we used an earlier version of the pixel readout chip developed at Fermilab (FPIX1)[4]. Two different detectors were tested in a thermal cycle. The first one was assembled on a flex circuit [5] and had a p-stop sensor from SINTEF (Oslo, Norway) [6] mated to a FPIX1 chip by indium bumps. The second detector used solder bumps and was assembled on a printed circuit board. To vary the temperature, we used two thermoelectric coolers (Peltier coolers). The settings and duration of the runs were controlled automatically by a LabView program.

The main goals of this thermal cycle test were to verify the effect of temperature changes on the bump-bonded connections, and on the behavior of the flex circuit attached to the detector, as well as on the noise and the threshold characteristics and dispersion of the readout chips. The details of this study are presented elsewhere [7]. Here we present in Tables II-VI the effect of a temperature scan on the performance of the chips. The quantitative details of the scan for the indium bump detector are shown in Fig. 8. The scan was composed of five runs (cycles) of rising and falling temperatures, varying between 7° C and 69° C for the indium-bumped detector and between 7° C and 42° C for the solder-bumped detector.

TABLE III. PERFORMANCE OF INDIUM BUMP DETECTOR AFTER FIRST CYCLE

% of channels	at 7° C	at 69° C
Working	96.25	61.88
Not Responding	3.20	32.81

Very Noisy	0.55	5.31

TABLE IV. PERFORMANCE OF INDIUM BUMP DETECTOR AFTER ALL CYCLES

% of channels	at 7° C	at 69° C
Working	96.02	61.95
Not Responding	3.28	32.27
Very Noisy	0.70	5.78

TABLE V. PERFORMANCE OF SOLDER BUMP DETECTOR AFTER FIRST CYCLE

% of channels	at 7° C	at 42° C
Working	91.25	86.54
Not Responding	8.75	13.17
Very Noisy	0.0	0.29

TABLE VI. PERFORMANCE OF SOLDER BUMP DETECTOR AFTER ALL CYCLES

% of channels	at 7° C	at 42° C
Working	91.25	86.54
Not Responding	8.75	13.22
Very Noisy	0.0	0.24

From these data, we conclude that the detector using indium bumps shows a slightly bigger permanent effect of the thermal cycling compared to the one using solder bumps. As we have seen in the glass-silicon module tests, the temperature cycling might be damaging some of the indium bumps causing a change in the capacitance of the corresponding electronics channels. This in turn results the very slight increase (<1%) in the non-responding and/or noisy pixels that we observe here.

IV. CRYO TEST

The BTeV pixel detector will be operating in a vacuum and be cooled by liquid nitrogen (LN_2). In the event of an accident, the detectors, and therefore the bumps and the wire bonds, might possibly be exposed to cryogenic temperatures. In order to study the effects of such an exposure, we built a cryo vessel that houses a printed circuit board (PCB) on which we installed a dummy hybrid. This hybrid contained 5 channels each with a daisy chain of 32 solder bumps. The channels were wire-bonded to the strips on the PCB and the strips were accessed from outside of the vessel by flat cable connectors. We then measured the electrical resistance of the channels. An open channel (infinite resistance) would indicate a break in either at the bumps or at the wire-bond. The hybrid was glued on a TPG, which was glued on a copper plate. The copper plate, and therefore the TPG and the hybrid, were cooled in the vessel by conduction. Fig. 7 shows the PCB and the hybrid assembly. We had two test cycles of exposing this PCB-hybrid assembly to LN_2 temperature to check out the hardware and test procedure. We have built another PCB-hybrid assembly with 40 channels and will build a few more to extend this study with higher statistics. In the future, we also plan to test pixel detectors operating at cryogenic temperatures.

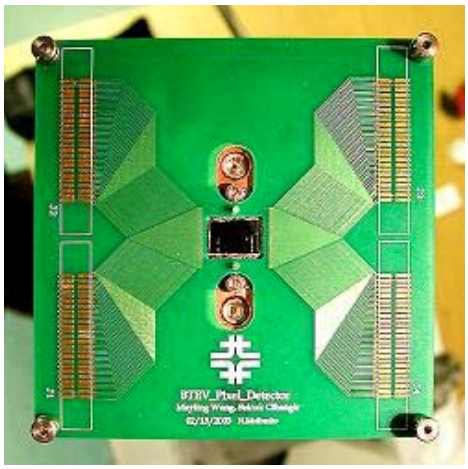

Fig.7: PCB-hybrid assembly for the cryo test

V. CONCLUSIONS

The bump bonding technologies with indium and solder are both viable for pixel detectors. The indium bumps look somewhat more susceptible to temperature variations. We visually observed the degeneration of these bumps at cold temperatures. The shift on some of the glass chips we observed can be attributed to the production errors (misalignment) rather than the temperature changes. The solder bumps on the other hand, were not affected by temperature changes or by radiation. The visual changes we observed on the solder bumps are superficial in origin and are not expected to cause any operational problems. The CTE mismatch between the TPG and silicon seems to have no effect on the structural integrity of the bump bonds of either kind.

VI. REFERENCES

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