PULSED LOW-LEVEL BASEBAND RF CONTROL OF CH-CAVITIES FOR P-LINAC AT FAIR*

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Abstract

At the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany a high intensity antiproton beam will be produced. To provide the necessary 70 mA proton beam a dedicated proton linac (p-Linac) is under construction. The main acceleration will be provided by 9 novel CH-type cavities, of which 6 will be coupled in pairs to share the same klystron. To test the rf properties of these novel cavities, a test stand is under construction. An rf control system for the pulsed operation of these cavities has been developed at TU Darmstadt. It is based upon the digital cw rf control that is successfully in operation as part of the S-DALINAC at IKP Darmstadt. The latest developments will be presented.

THE P-LINAC TEST-STAND AT FAIR

The *Facility for Antiproton and Ion Research* (FAIR) will be an international research infrastructure connected to the *GSI Helmholtzzentrum für Schwerionenforschung* (GSI) at Darmstadt, Germany. One of the main features of FAIR will be research using antiproton beams. In order to produce an antiproton beam that meets the needs of the experiments and the limitations of the beam transport, a pulsed proton beam of an energy of up to 70 MeV and a peak current of up to 70 mA is needed. This proton beam will be provided by a dedicated linac, the p-Linac, for injection into the SIS18 synchrotron.

The main acceleration of protons in the p-Linac will be provided by normal conducting, crossed-bar, h-mode (CH) cavities with a frequency of 325 MHz. These cavities will be driven by pulsed 2.5 MW klystrons [1]. These novel cavities and their peripheral devices have to be tested. Therefore an RF test stand is under construction at GSI.

For this test stand a pulsed RF control system is needed. It has to achieve an amplitude stability of 10^{-3} and a phase stability of 0.1°. An RF control system that meets this requirements has been developed at TU Darmstadt. It is based on the digital RF control system of the **S**uperconducting **Da**rmstadt **Lin**ear Electron **Ac**celerator (S-DALINAC) [2].

THE S-DALINAC RF CONTROL SYSTEM

The control system for the superconducting and normal conducting cavities at the S-DALINAC operates at 3 GHz in cw mode [3]. As shown in fig. 1, it consists of two components, an RF board and a low-level baseband control

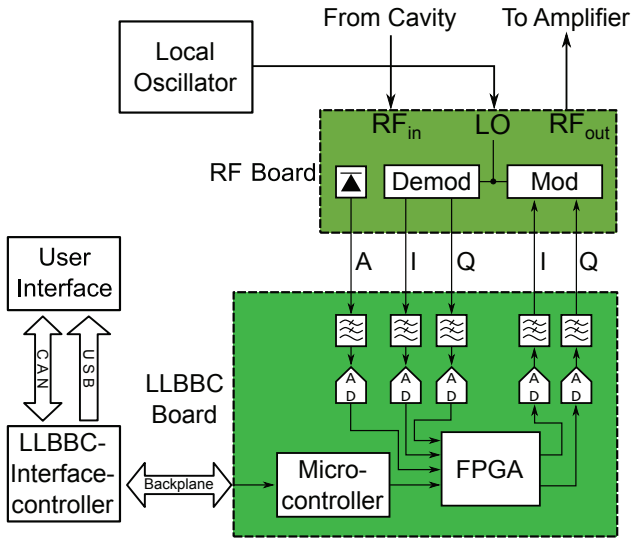

Figure 1: Diagrammatic overview of the low-level baseband control system used at the S-DALINAC.

(LLBBC) board. The RF board (de)modulates the RF signals from/to baseband as an (I,Q) vector. An amplitude detector on the board provides the amplitude of the incoming RF signal. The LLBBC board processes the baseband signal from the RF board.

The controller is implemented as a repeating algorithm, executed by a custom made Digital Signal Processor [4]. The latter is implemented in an FPGA. The algorithm is stored in the memory of the FPGA and may be changed, even at runtime. The output of the control algorithm is fed to a digital-to-analogue converter (DAC) which provides the signal for the quadrature modulator on the RF board.

Figure 2 shows a signal flowchart representing the control algorithm for normal conducting cavities. The phase of the signal is computed from the (I,Q) vector using the CORDIC

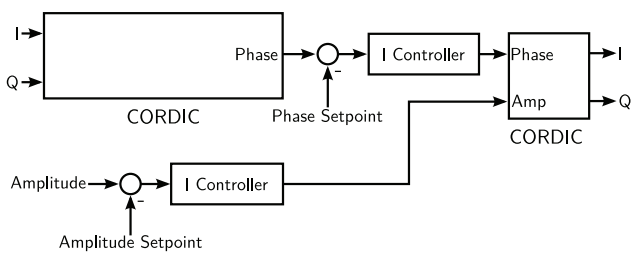

Figure 2: Signal flowchart of the control algorithm used for normal conducting cavities at the S-DALINAC.

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ISBN 978-3-95450-132-8

algorithm [5]. The amplitude is directly provided by the RF board's amplitude detector, for higher accuracy. The amplitude and phase errors are calculated and fed to controllers. Both controllers are implemented as proportional-integral (PI) controllers. A second CORDIC algorithm computes the outgoing (I,Q) vector from the phase controller and amplitude controller outputs. See ref. [3] for further details.

SETTLING-TIME IMPROVEMENT

Settling time is defined as the time a controller needs to hit the error margins after a step response. It is thus a good measure to describe the time a control system needs to react to fast changes like the slope of an RF pulse or beamloading of a pulsed beam. Various measures to improve the settling time of the pulsed control system will be presented below.

Filters

Low-pass filters are used in front of the ADCs and after the DACs (fig. 1). They serve as anti-aliasing filters for the ADCs and as reconstruction filters for the DACs.

The filters for the superconducting 20 cell cavities of the S-DALINAC need an attenuation of -50 dB at 500 kHz in order to prevent the excitation of near pass-band modes. Thus 3rd order filters with an edge frequency of 100 kHz are used for the S-DALINAC. As the next mode in the coupled CH cavities is about 900 kHz away [6], there is no need for 3rd order filters at the p-Linac. In order to prevent the signal deformation of a 3rd order filter, the filters have been reduced to 1st order filters with the same edge frequency, still providing an attenuation of about -24 dB at 500 kHz [7].

In order to test the impact of the new filter on the settling time, a full control loop including amplifier and cavity has been put to test at pulsed operation. The control parameters have been iterated to the fastest possible settling time for every filter. Figure 3 shows the step responses of the relative amplitude errors with 3rd and 1st order filters. The settling time is reduced by about 40%, according to this measurement.

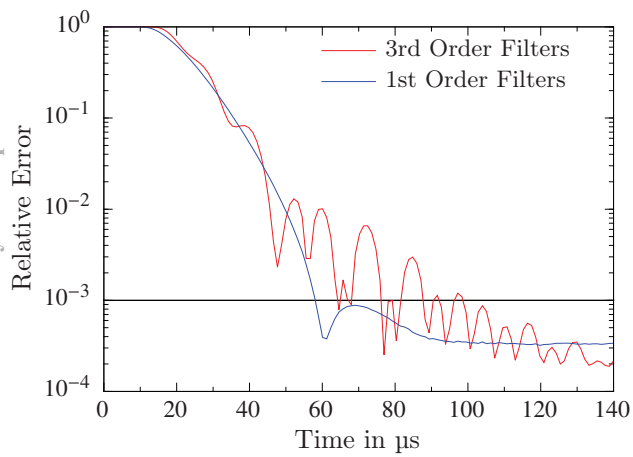

Figure 3: Relative error over time of the step response of a closed loop control system, measured with 3rd and 1st order filters.

Amplitude Detector

The amplitude detector on the RF board uses a low-pass filter for averaging and thus shows an insufficient response time (see [7]). Computing the amplitude from the (I,Q) vector is a faster method to get the amplitude. In order to do so, the first CORDIC algorithm has been reconfigured to provide an amplitude output. For technical reasons it is impossible to provide the output of the amplitude controller to the second CORDIC. Thus the amplitude controller is set up to run in parallel to the second CORDIC and its output is used to scale the I and Q outputs of that CORDIC. The resulting control algorithm is shown in fig. 4.

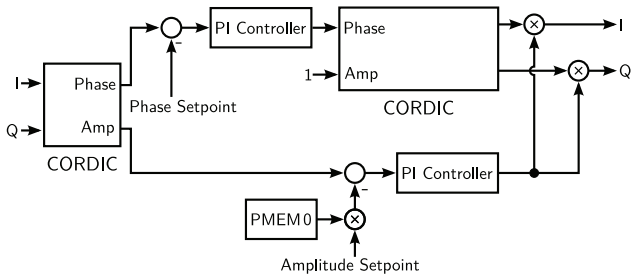

Figure 4: Flowchart of the control algorithm that uses the CORDIC to calculate the amplitude from the (I,Q)-signal instead of using the amplitude detector.

The impact of the replacement of the amplitude detector on the settling time has been investigated via the same experiment as used for the filters. The results have been plotted in fig. 5. The settling time was further improved in comparison to the effect of the filters alone. The main effect of using the CORDIC seems to be, that the integral controller starts early, as the error graphs have approximately the same slope.

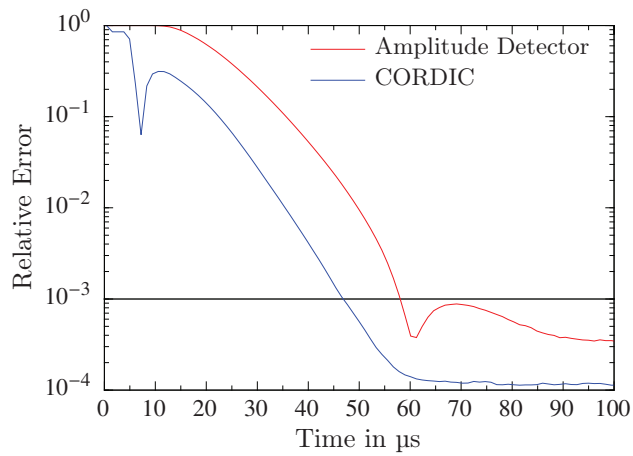

Figure 5: Measured step response of a control system using the amplitude detector and one using the (I,Q)-signal to determine the amplitude.

Feed Forward

To further improve the settling time a feed forward controller has been implemented in addition to the feedback controller. It is implemented as a second PMEM instance, that holds a pulse shape of its own. The output of this feed forward controller is added to the output of the amplitude controller, as shown in fig. 6.

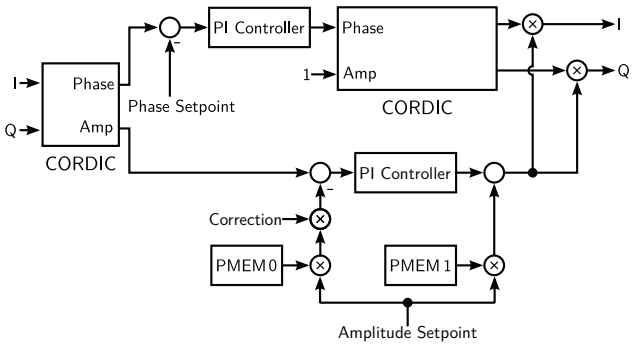

Figure 6: Signal flowchart of the control algorithm with feed forward.

The impact of the feed forward has been tested with the same experimental set up as described above. The feed forward pulse used in this experiment has the same shape but started 4 µs in advance of the pulse shape used by the feed back controller, as this seemed to generate the shortest settling times. The results are shown in fig. 7. The amplitude

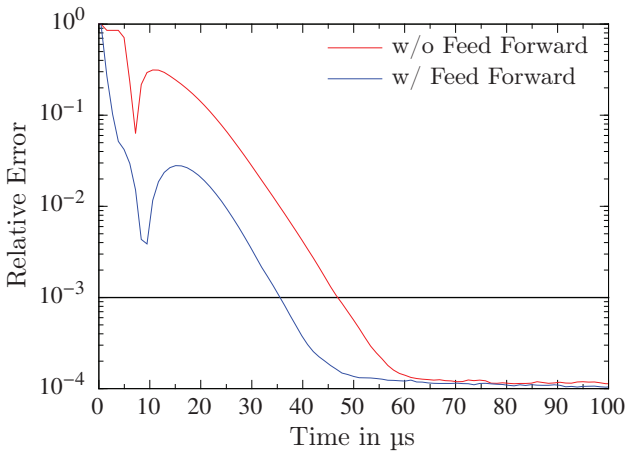

Figure 7: Measured step response of a control system using feed forward and one that does not.

error starts to decrease as soon as the step hits the cavity due to the feed forward. As the feed back controller kicks in, the error is already decreased so that the integral controller has less error to compensate and thus leads to a decrease of the settling time.

SUMMARY

The measurements presented in this paper have shown that the reduction of the filters, the replacement of the amplitude detector and the implementation of a feed forward have decreased the settling time of the pulsed RF control system considerably. As fig. 8 shows, the combined effects of all measures have decreased the settling time to about 40% of the initial settling time.

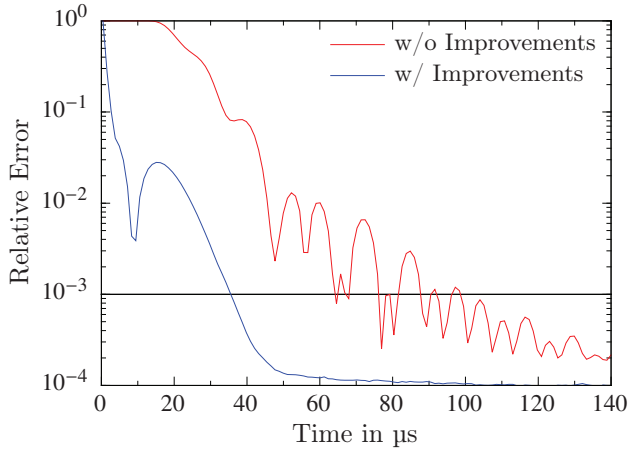

Figure 8: Measured step responses of a control system using 3rd order filters, feed forward and amplitude detector and one using 1st order filters, no feed forward and determines the amplitude from the (I,Q)-Signal.

Further experiments at the RF test stand at FAIR with a CH-cavity and a pulsed klystron are needed, in order to determine absolute settling times for the whole RF system.

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ISBN 978-3-95450-132-8