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A 2 Gsps waveform digitizer ASIC in CMOS 180 nm technology

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ABSTRACT:

The design and measurement results of a waveform digitizer based on the Switched Capacitor Array (SCA) architecture, fabricated in CMOS 180 nm technology, are presented. The prototype ASIC containing two channels inside is fully functional at a sampling rate of 2 Gsps with an analogue -3 dB bandwidth of about 450 MHz. Each channel integrates 128 sampling cells and a ramp-compare ADC. With this ASIC, sine waveform and reconstructed PMT waveform recording tests were conducted. We also evaluated its performance on fast pulse timing, and the timing precision is proved to be better than 20 ps RMS after a series of correction strategies.

KEYWORDS:

Switched Capacitor Array; ASIC; Waveform sampling; Time interval; Timing precision.

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1. Introduction

In modern particle physics experiments, waveform digitization offers maximum possible information, such as arrival time, charge, waveform shape, and so on. As for fast detectors used for precise timing, e.g. Multi-gap Resistive Plate Chamber (MPRC), a high sampling rate up to Gsps (Giga-samples per second) is required. The traditional solution employing fast Analog-to-Digital Converters (ADCs) in the Gsps level suffers from power dissipation, and especially high cost. The above disadvantages preclude it from application in modern particle physics experiments, in which a huge volume of channels are often employed. An alternative approach to tackle these requirements is Switched Capacitor Arrays (SCAs). SCAs use a series of capacitors, connected via switches to an input bus to sample an analogue signal, and this architecture has the advantage that they can operate at several Gsps with low power consumption.

Heavy ion research facility in Lanzhou (HIRFL) is the biggest heavy ion experimental facility in China, and the T0 detector, consisting of MRPCs, is one of the key components in HIRFL CSR (Cooling Storage Ring) external target experiment. Precise time measurement is required for T0 detector with a time precision of 25 ps RMS, and the waveform digitization method based on SCA architecture is a viable solution. In this paper, we describe a 128-cell two-channel sampling ASIC architecture and present the measurement performance.

2. Architecture

This is a two-channel SCA ASIC prototype, and each channel has a depth of 128 sampling cells. An overview of the major functional blocks of one channel is depicted in Fig. 1. The shared sampling clock is generated by an on-chip Delay-Locked Loop (DLL), in which the time delay of each stage is made from a CMOS current-starved inverter and the adjustable range is between 0.5 ~ 2 ns. Because of the feedback operation mode, the sampling rate is determined completely by the external input reference clock, almost independent of temperature, power supply and process. In the sampling circuit, to obtain a high input bandwidth and to reduce the distortion caused by switch's on-resistance, a careful tradeoff is made. Finally, a dual CMOS switch and a 110 fF MOS capacitor are used. After waveform capture, parallel digital conversion of all sampled signals is done on-chip with a ramp-compare ADC which consists of a global ramping voltage, a comparator for each cell and a 12-bit Gray-code counter. The digitized data is serially read out using a shift register 'token' architecture.

3. Performance

The ASIC is fully functional at the sampling rate of 2 Gsps. Tests in terms on DC offset, noise, frequency response, sampling intervals correction and fast pulse timing are carried out. The input voltage range is 0~1.1 V with an uncorrected Integral Non-Linearity (INL) 1% over a 900 mV dynamic range, and the offset among each cell varies between -15.62 ~ 25 mV because of process. Noise, after on-chip digitization, is equivalent to ~1.5 mV RMS. The frequency response result indicates that the analogue -3 dB bandwidth of the chip is about 450 MHz. A novel sampling intervals calibration method and the results on fast pulse timing are presented in the following.

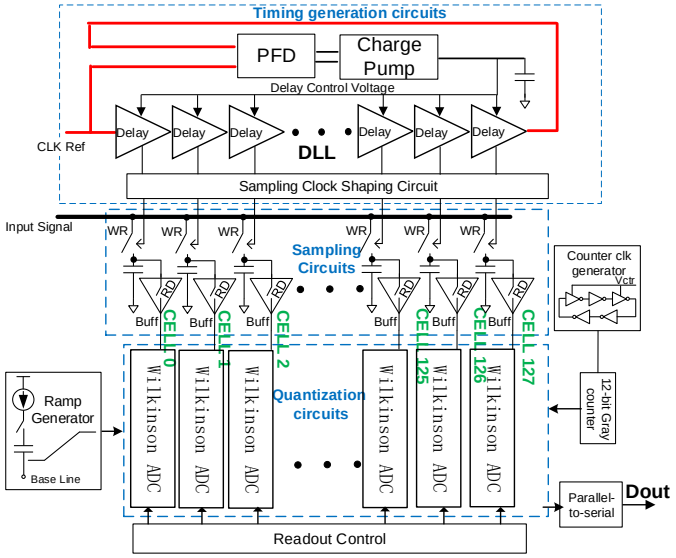


Fig. 1. Block diagram of the SCA.

3.1 Sampling intervals calibration

For SCA ASICs, variation of sampling intervals is inevitable because of process variation, so careful calibration is required to improve the timing resolution of such systems. The 'zero-crossing' time-interval calibration method is widely employed to find the intervals variations and compensate the waveform samples [1-2], it is also called 'local' time calibration in [2]. This method can be briefly described as following.

$$p = \frac{\Delta V_1}{\Delta t_1} = \frac{\Delta V_2}{\Delta t_2} = \cdots = \frac{\Delta V_i}{\Delta t_i}, i = 1, 2...N \tag{1}$$

$$\sum_{i=1}^{N} \Delta t_i = N \cdot \frac{1}{f_{CLK\_REF}} \tag{2}$$

$$\Delta t_i = \frac{\Delta V_i}{\sum_{i=j}^{N} \Delta V_j} \cdot N \cdot \frac{1}{f_{CLK\_REF}} \tag{3}$$

where N is the cell number of one channel, ΔV_i is the amplitude difference between two 'zero-crossing' samples cell i and cell i+1, Δt_i is the sampling interval between them, f_{CLK_REF} is the reference clock of the DLL, and p is the slop of input sine signal at the 'zero-crossing' point. However, because of the gain variation of each cell caused by the process and bandwidth limitation, the hypothesis in (1) is not strictly correct. So a 'global' time calibration is also conducted to refine the sampling intervals further, as mentioned in [2].

In this paper, we proposed a new time calibration method base on the ideal of 'global' time calibration. The principle is illustrated as shown in Fig.2. A 50.3 MHz sine wave is fed into the ASIC, and the period of the recorded waveform is determined by the time difference between a and b, which can be expressed as:

$$T_s = \alpha \Delta t_9 + \sum_{i=10}^{48} \Delta t_i + \beta \Delta t_{49} \tag{4}$$

We get α and β by linear interpolation:

$$\alpha = \frac{V_{10} - V_{DC}}{\Delta V_9}, \beta = \frac{V_{DC} - V_{49}}{\Delta V_{49}} \tag{5}$$

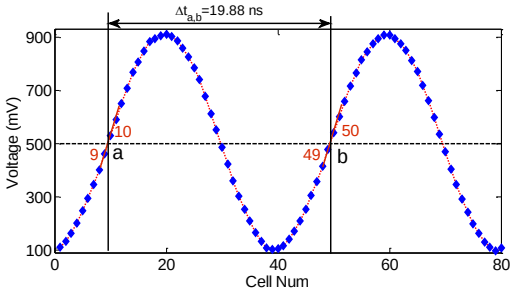


Fig. 2. Sine wave used for time calibration.

where T_S is the known period time of input sine signal, V_i is the voltage measured at cell i, and V_{DC} is the DC voltage of the sine wave. 2000 digitized sine waves are applied to the calculation, and we get an over-determined linear system expressed as a matrix function as shown in (6). The root of the function is the sampling intervals matrix. Compared to the method mentioned in [2], we don't need to get the 'local' time calibration result firstly, and boost the efficiency considerably without loop iteration.

$$\begin{pmatrix} 0 & \cdots & 0 & \alpha_1 & 1 & \cdots & 1 & \beta_1 & 0 & \cdots & 0 \\ 0 & \alpha_2 & 1 & \cdots & 1 & \beta_2 & 0 & 0 & 0 & \cdots & 0 \\ \cdots & 1 & \beta_3 & 0 & 0 & \cdots & 0 & 0 & \alpha_3 & 1 & \cdots \\ & & & & & \vdots & & & & & \\ 1 & \cdots & 1 & \beta_{2000} & 0 & 0 & \cdots & 0 & \cdots & 0 & \alpha_{2000} \end{pmatrix} \cdot \begin{pmatrix} t_1 \\ t_2 \\ t_3 \\ \vdots \\ t_{128} \end{pmatrix} = \begin{pmatrix} T_s \\ T_s \\ T_s \\ \vdots \\ T_s \end{pmatrix} \tag{6}$$

Fig.3 shows the sampling intervals after calibration.

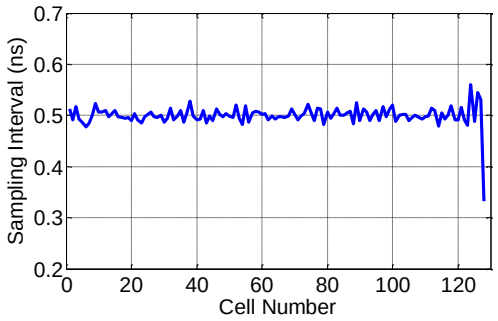


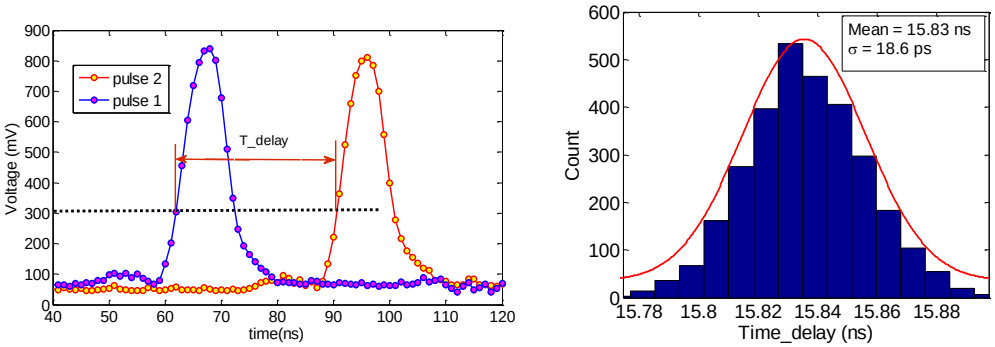
Fig. 3. Sampling intervals after calibration.

3.2 Waveform timing

The cable delay of fast pulse was used to evaluate the precision of waveform timing. In the test, a fast pulse generated by a function generator is split into two branches, which are connect to two channels via two different length cables, and the time difference between the arrivals is measured.

With a same trigger, the two signal were captured by two channels at the same moment, and typical waveforms after voltage calibration are shown in Fig. 4(a). A polynomial functional fitting is applied to the leading edge of each pulse, and a global threshold of 300 mV was used to get the time information. Since two channels are used to determine this difference, and the two channels are identical and independent, so the timing precision per channel is 1/√2 of the standard deviation

of the time differences. Fig. 4(b) shows the delay distribution of the pulse delay with time intervals calibration. The cable delay is found to be 15.83 ns, and the timing precision per channel is about 19 ps RMS after time intervals calibration.



(a) (b)

Fig.4. (a) Split pulses recorded by two channels. (b) Distribution of the pulse delay.

4. Conclusion

We presented a SCA ASIC prototype with an analogue bandwidth of about 450 MHz, capable of being sampled stably at 2 Gsps. A new sampling intervals calibration method was proposed, and with this new calibration, it is possible to extract precision timing information with a timing resolution below 20 ps RMS.

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