

The 100,000 Amp DC Power Supply for a Staged Hadron Collider Superferric Magnet

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Abstract— A 1.5 volt 100,000 amp DC switcher power supply was developed for testing a superferric magnet string at FNAL. This supply was used during testing as both the ramping supply and holding supply powering a single magnet load with a total load resistance of 0.7μ Ohms. The supply consists of ten paralleled switcher cells, powered by a 400 volt/600 Amp DC power supply. Each cell consists of an IGBT H-bridge driving a step-down transformer at a switching frequency of 2 kHz. The transformer has an effective turns ratio of 224:1. The secondary consists of 32 parallel single-turn full wave rectifier windings. The rectification is done with 64 Shottky diodes. Each cell is rated at 1.5 volts/10,000 amps. During this test each cell was operated as a constant power source without load current or field feedback. This paper will describe the design of the switcher cell and control system used during testing. We will also describe the next level of improvements to the current feedback system to improve the ramp control.

Index Terms— Accelerator power supplies, DC-DC power conversion,

I. INTRODUCTION

THIS document describes the design of a 100,000 amp DC-DC converter constructed for the purpose of testing a Superferric Magnet and Power Lead. A ring magnet system would consist of a holding power supply and a ramping power supply: the DC-DC converter would be used as the holding supply. The magnet and power lead tests were performed using only a single small sample magnet, so only the holding power supply was constructed and used for both the ramping and holding operations.

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II. HOLDING POWER SUPPLY DESCRIPTION

A. System Layout

The holding supply is constructed by connecting ten-1.5 volt/10,000 amp switcher power supplies in parallel. Two copper current collectors in the shape of a half moon and 10cm thick sum the current, and connected directly to the input of the Power Lead. Each switcher cell is a 10,000 amp bridge converter operating from a 0-400 volt bulk power supply. With the holding power supply only being able to supply 1.5 volts, the system is self limiting; the quench protection for the test performed was a simple temperature monitor that would bypass the supply.

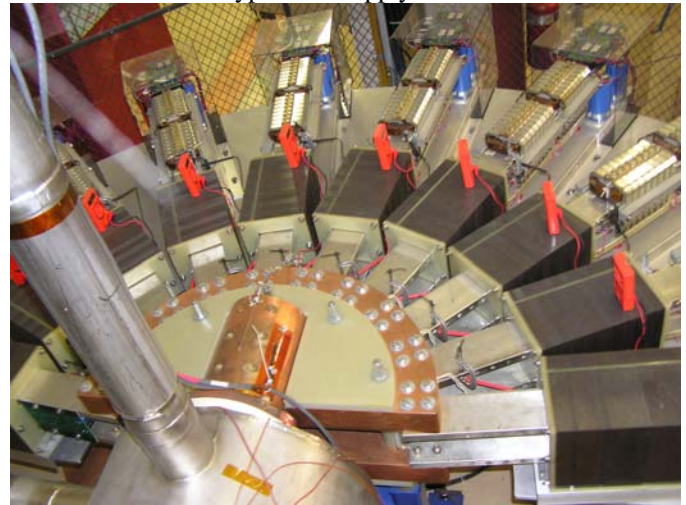


PHOTO 1 Power Lead with 10 Cells connected

B. Topology of the DC-DC converter

The rectifier assemblies consist of two 112:1 transformers with primaries driven in series and secondaries in parallel. See Figure 1. Each primary consists of 112 turns of 0.625cm magnet wire. Each secondary consists of 16 parallel single-turn full-wave rectifier windings made of copper sheet and wound over the primary in a low leakage-inductance configuration. Each of the 16 secondary sums through 32 Shottky rectifier diodes.

We determined that current sharing in the parallel diodes would be adequately maintained by the diode characteristics and the copper sheet winding resistance without the need for sharing resistors.

The windings are on a 1 mil tape-wound core of 2.54x2.54 cm

cross section with a window of 21x11cm. The core was wrapped with Kapton tape to prevent winding abrasion. To keep noise low, we used a gapless core.

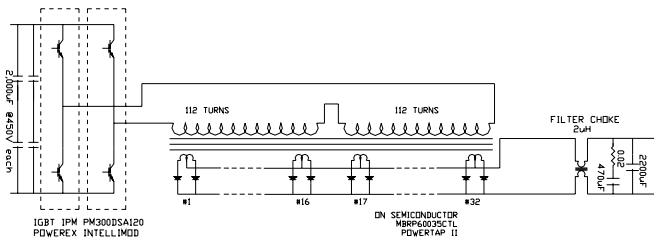


FIGURE 1 Cell schematic

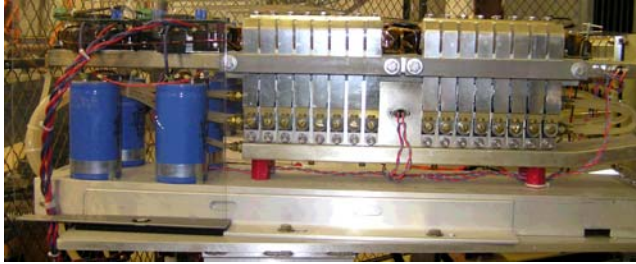


PHOTO 2 10,000 amp cell assembly

C. Current Regulation

Since we had no effective 10,000 amp current monitors that fit into the assembly, we chose to regulate each cell using feedback from a Hall device current monitor installed in the input current lead to the cell. See Figure 3. This made each cell function as a programmable power source, assuming that the bulk supply voltage was constant. For stable current regulation this requires that the magnet system load be a constant or have a small resistive and inductive dynamic range.

During these tests one cell was used for injection level at 3,000 amps, and the other nine were ramped together. When the magnet system was cold (30-50) K but not superconducting the total load resistance was under 18 μ ohms. This allowed us to startup the first cell and ramp to 3,000 amp level with little or no load on the cool down. Low level operation allowed us to verify that the instrumentation was all operational and ready for high current operation.

The ramping computer was a laptop with a National Instruments NI-DACCard-6036 which has 16 analog inputs and two analog outputs that were used as a reference to the first cell for the injection level and then one reference for the other nine cells. The ramps were simple EXCEL files loaded into a custom National Instruments LabviewTM application and played out of the DAC card. Chart #1 displays the two ramp programs used for the first cell and then the other nine and the total desired current.

While ramping up in power mode we measured the output current on each cell using the buswork as a shunt with a DVM readout. We used these measurements to verify the total current operation for all of the tests.

The power in each cell was regulated through feedback to an industrial standard PWM switcher control chip (UC3846)

operating at 2k Hz.

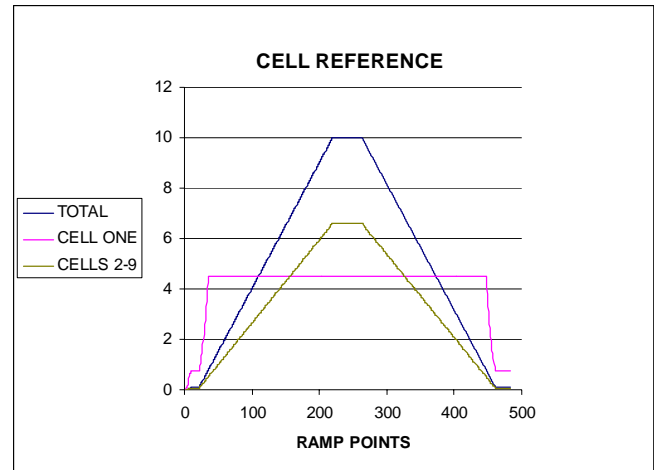


CHART 1 Ramp program for ten cells.

D. Input switcher front end

The H-bridge front end is constructed using POWEREX IGBT-IPM IntellimodTM modules, PM300DSA120, driven through fiber optic cables. Each IGBT is rated for 300 amps and 1200 volts with two transistors in each package. These modules have the gate drive internal to the package making the gating simple and fast. The IGBT assembly is mounted on the 2.5x10cm copper bus that is the return bus for cooling.

To minimize the switching electrical noise each cell is supplied power using an RG220 coax cable. The local high frequency current is supplied from a 2,000 μ F series-parallel cap bank mounted close to the H-bridge, see figure 2. To limit the interference of the switching noise from cells we installed a ground plane with a 25x0.15cm surface cross section from the power lead to the control racks. The entire system has a single point ground at the power lead for all the control and monitor signals. All the control circuits for the cells are either opto-coupled or use a fiber optic cable.

E. Bridge Diode

The diode bridge is constructed using ON Semiconductor PowertapTM low V_F Schottky barrier rectifier devices, MBRP60035CTL. Each diode is rated for 300 amps with a 0.57 ON voltage and 35 volt reverse blocking. There are 64 diodes installed on each 10,000 amp cell with a total of 640 in parallel for the 100,000 amps. At 10,000 amps in a cell each diode is operated at 156 amps DC and 89 watts. The PowertapTM devices have a strict mounting requirement due to the long thermal conduction path of the assembly. Each diode assembly is mounted to a large copper-water cooled heat sink with spring loaded washers and torqued to the required values. One concern we had during operations was the failure mode for the diodes. With 640 diodes in parallel the question we had was how much damage would we get if one failed? We ran a diode pair until it failed short on a test bench. The failure was very mild and only a little smoke was let out and then the diode opened. During early testing we had one diode fail in operation at less than 10,000 amps total current. The result was the same; a little smoke was let out and the cell kept running.

F. Filters

This power system has three filters installed: the output of the bulk power supply, the input to each cell and the output of each switcher cell. The 0-400 volt bulk power supply has a damped LC filter with a corner frequency at 60 Hz. The front end filter to each H-bridge uses a 1mH inductor for isolation between cells and 2,000 μ F electrolytic low ESL energy discharge caps to provide the fast local current during switching.

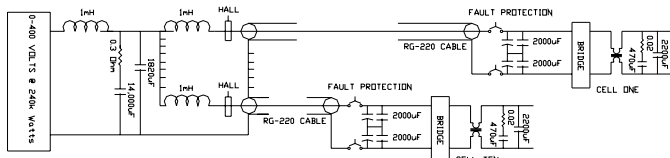


FIGURE 2 Filter schematics.

The output filter from each of the switcher cells is a damped LC filter with a 2400 Hz corner frequency. The output choke is constructed using “E” laminations stacked over the 2.5x10cm bus creating a 2 μ H filter choke. A damped filter is installed on a circuit board mounted directly to the bus work at the output of each cell.

G. System Protection

There are two distributed ground / ground fault detectors installed, one on the output of the bulk power supply filter and the second installed at the Power Lead. These systems keep the voltage to ground applied to the switcher cells and power lead equal to $\pm 1/2$ the output voltage respectively. A ground fault is considered to be an average voltage greater than $\pm 20\%$ of the absolute value of DC output. When a ground fault is detected we stop switching and bypass the main power supply.

The front end of each switching cell has a DC circuit breaker installed. These breakers are used as a local lock out device during maintenance. In conjunction with the 1mH inductors they provide fault current limiting from the other cells and main cap bank energy in the event of a cell short circuit.

Thermal protection on each cell is installed to prevent over heating of the diodes and IGBTs. These trips bypass all the switcher cells.

H. Calibrating and Testing

Each of the ten cells were constructed and tested to 10,000 amps using a 2,000MCM cable as a load. Then the ten cells were connected to the half moon copper current collectors that sum the current before connecting to the power lead. A copper shorting block was installed in place of the power lead to allow testing to 100,000 amps without the superconducting load. We ran the system at 100,000 amps DC for more than two hours and concluded that the supply was ready for a superconducting load.

The superconducting load was run from dewars of helium which limited the amount of time that we could operate at 100,000 amps. We ramped in steps to full current with short flattop times (5-10 seconds) at 2500A/s for more than 20

cycles, which was long enough for magnet field measurements. The maximum ramp current in to the superconducting load was 103.8k amps.

III. NEXT STEP FOR IMPROVEMENT

The large dynamic range and scale of the magnet system, 3,000-100,000 amps will need a specification for the regulation that can be constructed. The measurement of the current will require a high quality DCCT system with very stable long term drift. The construction of the DCCT may need to be an element on the superconducting bus due to the size and difficulty in creating a device large enough for warm bus. A reasonable design for air cooled warm bus would use 645cm² (air channels may require twice this volume) and 258cm² for water cooled. Aperture for superconducting bus would require a DCCT head to be 3 to 4 cm in diameter.

Designing and testing a cryogenic DCCT head will have system issues during quenching and cool down because it will be used for the feedback into the regulation. If the cryogenic DCCT is not able to function through to the warm environment of a quench then two could be used. One would be used for cold operation regulation the other could be of low accuracy and be used for monitoring the current during de-acceleration and MI^2t calculations.

All of the current regulation electronics will also be needed to be developed in support of the DCCT and current reference. The support electronics will need to be low noise and stable enough to meet the regulation specification. This level of system regulation may require that all signals become digital as soon as possible. The on going work to design a 24-32 bit ultrastable ADCs and DACs should be extended for use in this system. Even though the inductance of this magnet system is low the bit resolution may be necessary for absolute accuracy.

IV. ACCELERATOR SYSTEM LEVEL ISSUES

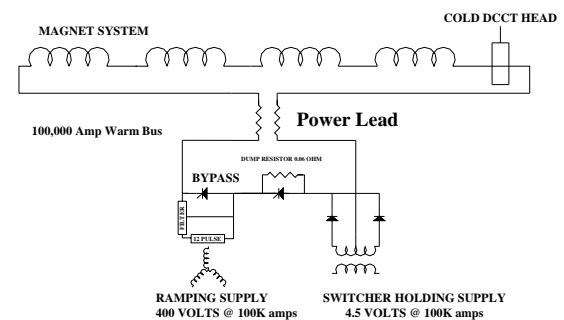


FIGURE 3 Accelerator Layout

V. RAMPING POWER SUPPLY DESCRIPTION

The accelerator power supplies are expected to ramp from an injection current level of 3,000 amps to the flattop level of 100,000 amps at a rate of 1,000 amps/second. During injection the holding supply will provide the current using only one of the ten DC-DC converter cells. The ramping

supply will be brought out of bypass just before the acceleration with the holding supply still being used by the current regulator for the fine control of the current. As the acceleration cycle starts the ramping supply will take over and provide the current to flattop, then the holding supply is then brought back ON to provide current while the ramping supply is returned to bypass. It may be possible to use the holding supply as a fine regulator during ramp but with only a 1% dynamic voltage range it would require a Learning Regulator to use it effectively in an accelerator system.

The configuration of the ramping supply will be tied strongly to the accelerator physical plant and configuration as well as the location of the power distribution plant. With the power demand at 40MVA peak and the RMS power being 500k Watts the system will require an electrical plant with a harmonic filter that can support a 100 second pulsed load at the start and end of every cycle. A possible concept for the ramping supply would be to construct 4-10MVA peak transformers with 4-25,000 amps RMS bridges connected in parallel through filter chokes to limit fault current.

VI. HOLDING POWER SUPPLY DESCRIPTION

The size of the holding supplies assumes that the power lead will be 0.7μ ohms with a total splice resistance of 0.1μ ohm. The holding power supply bypass and dump resistor bypass voltage will need to be less than 4 volts total. This leaves a maximum of 4.2μ ohms for the warm bus section. A reasonable level of over head voltage will also be needed to maintain regulation.

The holding power supply will need to be changed to a higher voltage system to meet the 4.5 volts needed for the accelerator. The present supply has a 900 volt limit on the input filter for the H-bridge and IGBTs. For 4.5 volt operation the H-bridge will need to be reworked for a 1400 volt operating level on the input to the transformers. The insulation on the primary winding provides the isolation from the bulk power supply and also ground. This will need to be improved to meet the higher voltage to ground levels during a quench and the 6kV from the dump resistor. Even though the testing showed that a diode failure was not catastrophic for the system, a detection circuit should be developed for monitoring the health of the diodes.

Development of a plan for the ramping supply could begin to deal with the low level voltage drop needed to keep the holding supply size under control. We use a design limit on large ramping power supplies that the supply needs to be rated for $\frac{1}{2}$ the difference of the peak Kva to RMS power, 20MVA. With 5% impedance transformers this could result in a bridge fault current of 200,000 amps and may be difficult to contain. If the ramping power supply is constructed using parallel high current supplies, the filter chokes can be used to help limit fault current. With parallel bridges and filters there may be a place for 4-25,000 amp DCCTs in the bypass SCR leg of the output at the expense of a larger voltage drop in the bus. The five current monitors would need to be summed and used for the regulation system feedback; this has the benefit of using a

proven DCCT technology. A risk to this system is that if a bypass device is not switched in then one of the DCCT is left out of the circuit and the others will saturate.

The ramping supply needs to be constructed for two quadrant operation to allow for de-acceleration of the bus. Taking the holding supply out of bypass is simple because the supply has 400 volts to use for this before it ramp to negative voltage. This means that it will need to go positive to disconnect the bypass device before it can go negative. Ensuring that all the bypass devices are on in parallel with limited voltage drop for sharing is difficult and will need design and development time. Using negative filter voltage at the start of a bypass may help to switch all devices ON.

VII. CONCLUSION

The operation and test performed in our superferic magnet test lab has proven that the power system for a large accelerator can be constructed and operated. Even though this system will need a regulation system that is at or above the level that is in use today, it fits into the next generation being designed.

ACKNOWLEDGEMENT

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