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FPGA based Compute Nodes for High Level Triggering in PANDA

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Abstract. PANDA is a new universal detector for antiproton physics at the HESR facility at FAIR/GSI. The PANDA data acquisition system has to handle interaction rates of the order of 10^7/s and data rates of several 100 Gb/s. FPGA based compute nodes with multi-Gb/s bandwidth capability using the ATCA architecture are designed to handle tasks such as event building, feature extraction and high level trigger processing. Data connectivity is provided via optical links as well as multiple Gb Ethernet ports. The boards will support trigger algorithms such us pattern recognition for RICH detectors, EM shower analysis, fast tracking algorithms and global event characterization. Besides VHDL, high level C-like hardware description languages will be considered to implement the firmware.

1. Introduction

PANDA [1] will be one of the major new detector facilities at FAIR (Facility for Antiproton and Ion Research) to be constructed at GSI Darmstadt. PANDA (see fig. 1) is a general purpose detector for antiproton physics and will be located in the High Energy Storage Ring (HESR) providing high quality antiproton beams with momenta up to 15 GeV/c for fixed-target experiments.

PANDA features two different spectrometers. The target spectrometer comprises a superconducting solenoid, silicon tracking devices, a central tracker (either TPC or straw tube based), a high quality electromagnetic calorimeter, BaBar-style DIRC for pion/kaon discrimination as well as a muon detector. The forward spectrometer is based on a large normal conducting dipole magnet and drift chambers, Cherenkov detectors and electromagnetic and hadronic calorimeters.

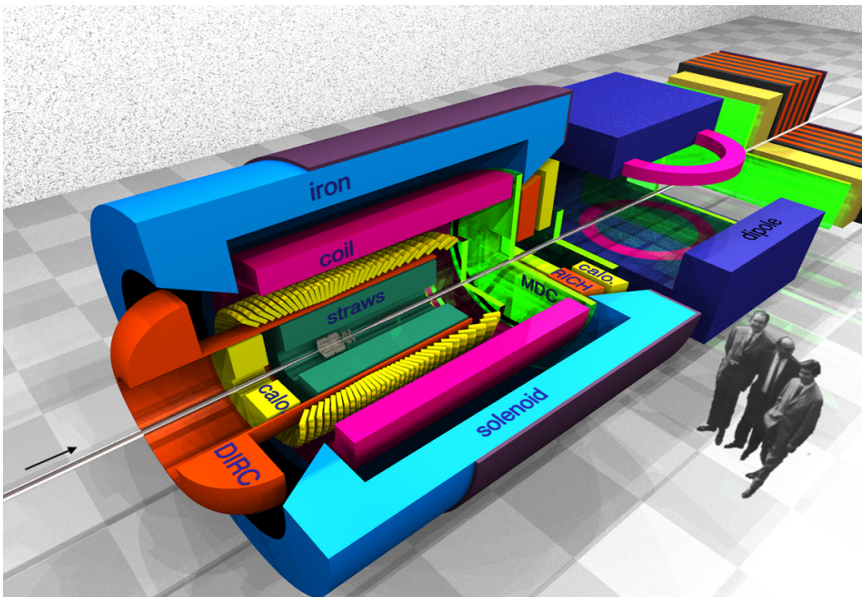

Fig. 1: The PANDA Experiment at FAIR

PANDA has a comprehensive physics programme which includes charmonium spectroscopy, the search for QCD exotica, hypernuclear physics as well as the study of charmed hadrons in nuclear matter. This rich and diverse physics programme requires high luminosity experiments with interaction rates in the order of 10^7/s. Raw data rates of the order of 40-200 Gb/s need to be processed in real time in order to select events of interest in a potentially very large background. The PANDA Data acquisition system (see fig. 2) does not employ fixed

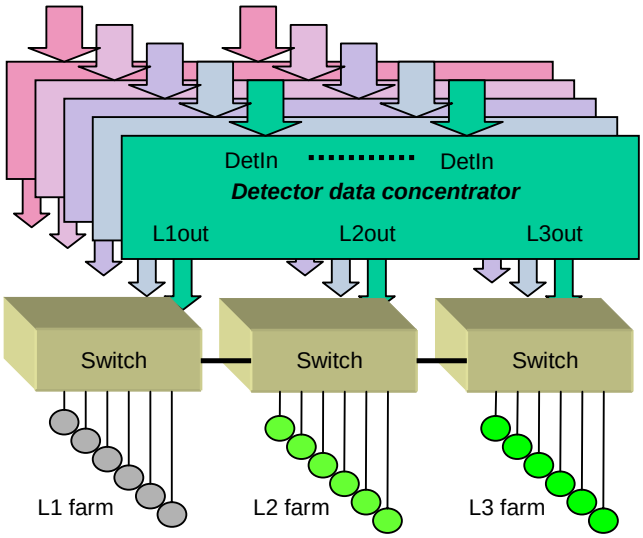

Fig. 2 Schematic overview of the PANDA data acquisition

Hardware based triggers but features a continuously sampling system where the various subsystems are synchronized with a precision time stamp distribution system. Event selection is based on real time feature extraction, filtering and high level correlations.

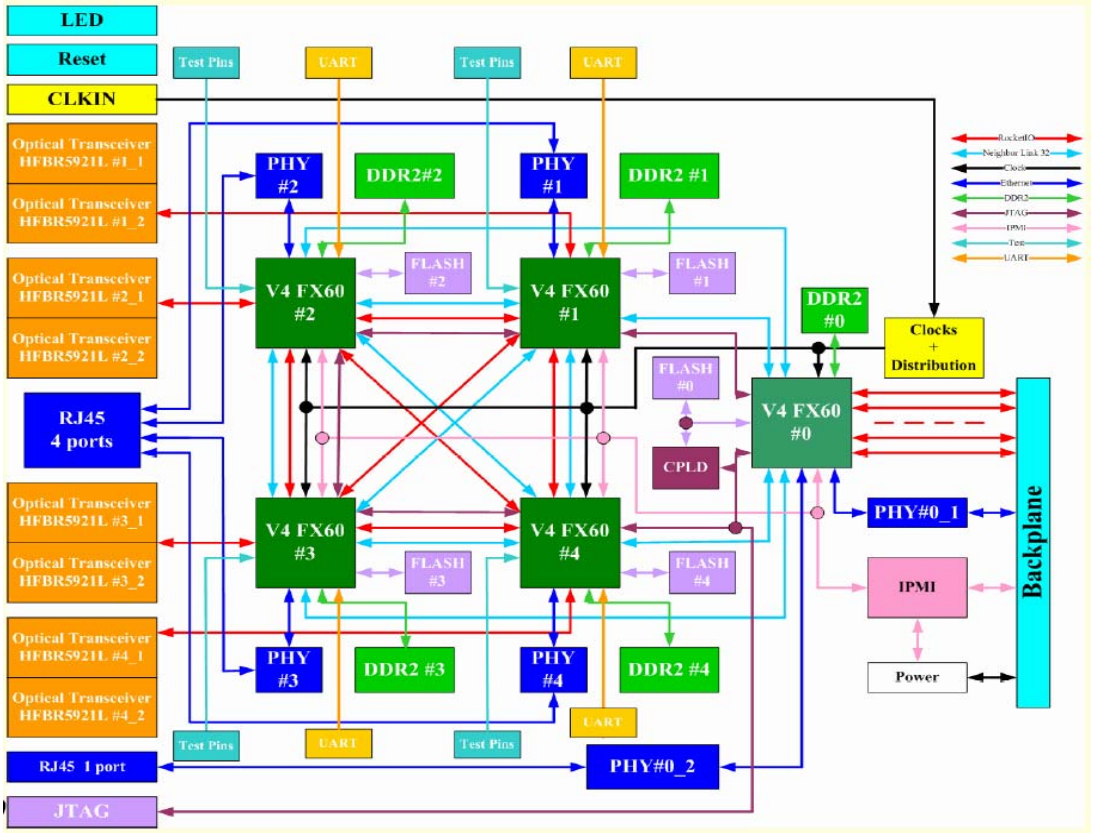

Fig.3: Architecture of the Compute Node

Event building and event selection will be performed in a system of networked FPGA based compute nodes (CN) which will serve as a basic building block for the PANDA DAQ system.

Fig. 3 shows a schematic view of the CN architecture. Its basic building blocks are 5 XILINX Virtex 4 FX60 FPGAs. 4 FPGAs are used to execute the trigger and event building algorithms. The 5th FPGA serves as a switch connecting to other CN modules in the same ATCA shelf via a full mesh backplane. Each of the 4 processing FPGAs is equipped with local DDR2 memory banks for buffering and other purposes such as large lookup tables. Connectivity to the front-end electronics is provided via 8 optical links connected to RocketIO ports on each of the 4 FPGAs. Moreover each FPGA is able to communicate via Gb Ethernet which can be supported either in a standalone mode using the FPGA fabric or using LINUX which is running on the embedded PowerPC (PPC) processors in the FX60 FPGA.

FPGA based architectures are most suitable for a cost-effective solution for parallel and pipelined processing. Moreover, modern FPGAs such as the XILINX Virtex 4 FX series provide high speed connectivity via RocketIO as well as via Gb Ethernet. With such a choice a solution can be built with flexible connectivity both to the detector front-end electronics as well as to conventional LINUX based PC farms for higher level processing.

The use of a powerful operating system such as Linux running in the embedded PPC has significant advantages. Using the XILINX Embedded Device Kit, dedicated IP cores can be developed which execute the filtering and data acquisition tasks. These IP cores can be interfaced to the local PLB bus of the PPC. Custom Linux device drivers can then provide interfaces for communication and configuration of the IP cores, hiding the details of the IP core design from the user application program. Furthermore, the Linux operating system can be

used to move data to and from the CN via Gb Ethernet. As an alternative, parts of the TCP/IP stack could be implemented in VHDL, enabling direct communication between applications written in VHDL and the embedded tri-mode Ethernet interface in the FPGAs.

In order to support the execution of algorithms requiring for more than a single FPGA or even more then a number of FPGAs placed on a single PCB, several CNs could be connected in a way which optimizes the mapping to the data sources. Moreover, the configuration should provide a suitable topology for effective partitioning of the algorithms. The ATCA full mesh backplane is well suited to provide such inter – board connectivity.

Applications for the CN include pattern recognition for ring imaging Cherenkov detectors, cluster search in calorimeters, tracklet search for the TPC, drift chambers and the silicon vertex detectors as well as more global correlations among subsystems. For the PANDA TPC option, a high rate environment is a challenging problem not only for the detector but also for the data acquisition and event selection. Due to the long drift times, several 100 events will overlap in the TPC. In order to assign tracks to corresponding events observed in the other detectors, special algorithms are being developed which employ signals from adjacent fast detectors such as the electromagnetic calorimeter for pointing. The mapping of such algorithms to the CN system will make heavy use of the networking capabilities as well as of the high available bandwidth.

2. Performance of Gb Ethernet

To get an estimate of the data throughput which could be achieved via Ethernet, we have measured the performance of TCP/IP and UDP/IP transfers using a Virtex 4 FX12 chip on a ML403 board from XILINX. Linux (kernel version 2.6) with a driver supporting the on-chip Gb Ethernet MAC was used. Point-to-point transfers connecting the FPGA and a PC running Linux were performed. The results of the measurements are shown in Table 1.

Protocol Type	Direction	Max. Throughput (Mbps)
UDP/IP	Board $\rightarrow$ PC	394.5 (TX)
UDP/IP	PC $\rightarrow$ Board	$\geq$ 394.5 (RX)
TCP/IP	Board $\rightarrow$ PC	297.8
TCP/IP	PC $\rightarrow$ Board	316.6

Table 1: Results of Ethernet performance measurements running Linux on the embedded PPC in an Virtex4 FX12 FPGA

It should be noted that the overall I/O bandwidth provided by a single CN module is of the order of 22 Gb/s and is completely dominated by the optical links and the RocketIO links to the ATCA backplane.

3. Conclusion

We have presented the design of Compute Nodes which will serve as basic building blocks for the data acquisition and trigger system of the PANDA experiment at FAIR. The most important features include flexible I/O with large bandwidth combined with powerful computing engines which can be implemented in the FPGA fabric, providing a scalable system based on ATCA shelves with full mesh backplane.

The first modules will be available by the end of this year and we plan to set up a small scale system which

can be used to upgrade existing experiments such as the HADES experiment at GSI and the BESIII experiment at IHEP Beijing. For detector tests of PANDA subsystems, small- but powerful standalone data acquisition systems will be assembled by combining CNs with a CPU module and ATCA based ADCs. Such systems will provide a realistic environment for the development of the firmware for the full system.

ACKNOWLEDGMENT

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References

[1] PANDA Letter of Intent, PANDA Technical Design Report (http://www.gsi.de/panda)