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DESIGN AND CONSTRUCTION OF THE FRONT-END ELECTRONICS DATA ACQUISITION FOR THE SLD CRID*

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Abstract

We describe the front-end electronics for the Cherenkov Ring Imaging Detector (CRID) of the SLD at the Stanford Linear Accelerator Center. The design philosophy and implementation are discussed with emphasis on the low-noise hybrid amplifiers, signal processing and data acquisition electronics.

The system receives signals from a highly efficient single-photo electron detector. These signals are shaped and amplified before being stored in an -analog memory and processed by a digitizing system. The data from several ADCs are multiplexed and transmitted via fiber optics to the SLD FASTBUS system.

We highlight the technologies used, as well as the space, power dissipation, and environmental constraints imposed on the system.

I. INTRODUCTION

The SLD is an e^+e^- spectrometer designed for Z^0 physics. It consists of five major subsystems for charged particle tracking and momentum measurement, particle identification and total energy measurement [1].

The Cherenkov Ring Imaging Detector (CRID) provides particle identification. Cherenkov photons generated by the passage of charged particles through liquid and gaseous radiators enter drift boxes with quartz windows, and ionize a drift gas mixture. The resulting photoelectrons drift in a uniform electric field and are detected on a 10 cm long 7 μm diameter carbon sense fiber [2].

Two coordinates of the point of origin of the photoelectron are determined by the wire address and the drift time. The third coordinate measurement, the position along the sense fiber, is measured using charge division techniques [3].

This paper describes the design and construction of the front-end electronics used in the barrel CRID to detect single photoelectrons. Details of the amplifier are provided in a companion paper submitted to this conference [4]. This is a large-scale project which requires a very intense design and development effort; yet the production runs for 8000 channels are small by electronic industry standards.

II. SYSTEM ORGANIZATION

Each CRID detector has 93 sense wires on a 0.125 inch pitch. To accommodate charge division, the front-end electronics have 186 waveform digitizer channels, one for each wire end. Each channel consists of a preamplifier, analog storage, digitizer, and calibration circuitry for channel-to-channel gain and pedestal variations.

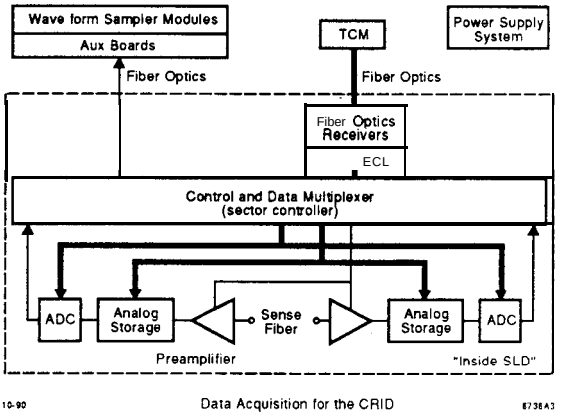

Fig. 1 Block diagram of the data acquisition system for one CRID sense wire.

A FASTBUS plant [1,5,6] controls the system-and processes the data from the CRID detectors. Figure 1 shows a block diagram of the overall acquisition system for one CRID sense wire. The Timing and Control Module (TCM) delivers control and timing information to the detectors electronics via digital fiberoptics. The communication is based on a three-wire protocol [7] with lines named Command, Clock, and Data. A fourth fiber is used to deliver write clocks for the analog storage. For redundancy, there are two sets of such fibers for each end of the barrel and each end cap.

When requested, the digitized data from the detectors are also sent via fiberoptics, to Waveform Sample Modules (WSM). The WSM auxiliary board is used to demultiplex the incoming data.

A. *Circuit* partitioning and packaging

The barrel CRID geometry has ten azimuthal sectors on each side of a high-voltage midplane. Each sector houses two drift tubes and their associated detectors.

The ten azimuthal sectors provide a natural partitioning for some of the circuitry. The second partition is dictated by the two detectors within each sector. Further partitioning is imposed by the component segmentation. We define the ends of the sense wire as "Inner" and "Outer" with Inner being the wire end which is closest to the interaction point.

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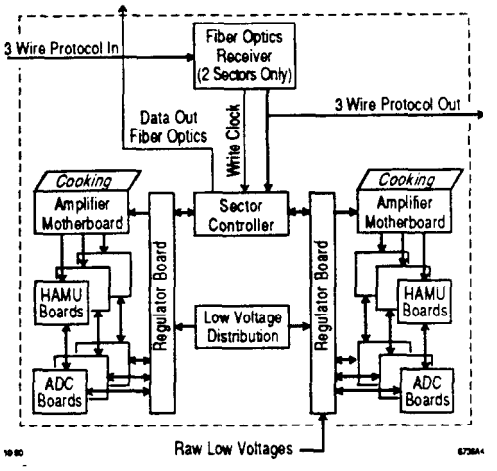

Fig. 2 Partitioning of the electronics within one sector.

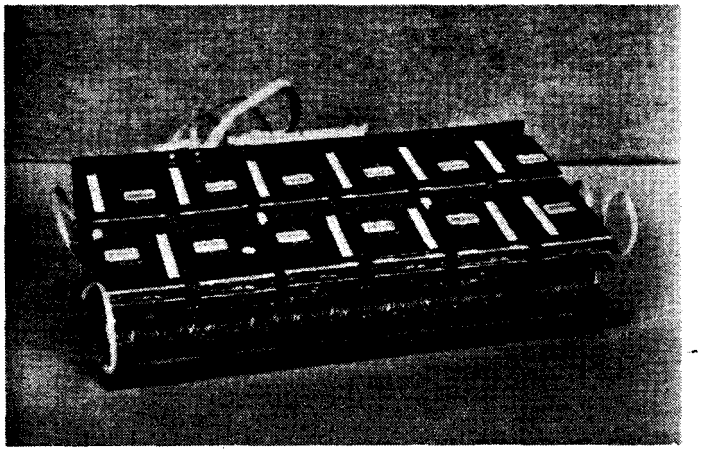

Fig. 3 Photograph of the front-end electronics.

We designed the system to be modular. Since no repair can be done in situ, much attention was paid to failure modes, so that a single component failure would not cause a complete system breakdown. In most cases, component failure diagnosis is possible without ***access*** to the electronics.

Figure 2 shows a block diagram of the partitioning within a sector. The two fiberoptics sets from the TCM are received by the fiberoptic receiver/fan out boards located in sectors near the top of SLD. The optical signals are converted to differential ECL and distributed to the ten sector controllers

To eliminate a cable plant carrying fast, low-level analog signals, the front-end electronics are mounted directly to the detector sense wires. This approach requires that the packaging conform to the mechanical structure of the detector and function at a temperature close to the 40°C of the CRID. Figure 3 is a photograph of this front-end electronics, demonstrating the physical constraints and density of the electronics necessary in this design. Figure 4 is an assembly drawing showing stacked circuit boards, and the water cooling for the amplifiers and the regulators. The motherboard provides the connections to

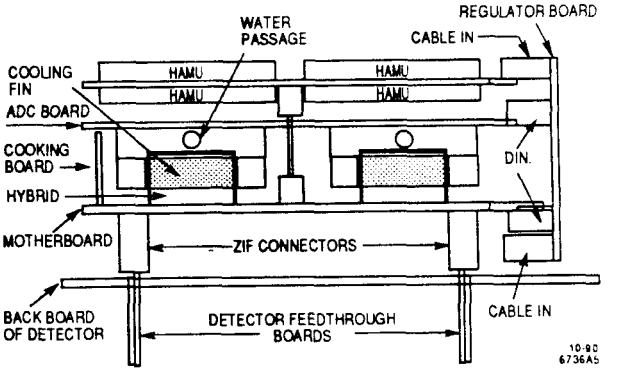

Fig. 4 Assembly drawing of stacked printed circuit boards.

the detector and active circuits for calibration and **power** sequencing. The HAMU boards, three of them per detector, support the HAMUs [8] and associated **circuitry.** The ADC boards provide signal conditioning and regulated power for the HAMUs, as well as the digitization of the HAMUs output during the read operation. The regulator board acts as an interface between the low-voltage distribution, the sector controller and the front-end electronics stack. The wire heating daughterboard **permits us** the option of vaporizing polymer deposits from the sense wires.

This **package,** the size of three CAMAC modules, contains more than 4700 discrete components. To reduce power dissipation, the power supply voltages needed for the amplifiers and the HAMUs are pulsed during data acquisition. The power supplies required to read the HAMUs are sequentially turned on for each HAMU set during the read cycle.

The mechanical packaging design was challenging. The registration between board connections in the stack had to be well specified. This was implemented using Autocad software [9]. The detector dimensions and connections were drawn, and the mechanical placement of the PC boards designed, to accommodate these restrictions. AutoCad's dimensioning features proved to be invaluable, as it was exceptionally easy to use.

III. AMPLIFIER

The CRID amplifier schematically shown in Fig. 5 was designed as a single-channel hybrid for the following reasons:

(1) system reliability;
(2) minimum channel to channel crosstalk;
(3) best technology match for medium size production.

The preampiifier functions are implemented using a low-noise JFET, followed by an analog semicustom integrated circuit **that includes the remaining** bipolar circuitry. **The integrated circuit** consists of a gain selectable amplifier, **load driver,** and power-down circuit. This, with a precision calibration circuit for the amplifier and HAMUs, is packaged on an 11-pin SIP hybrid with surface-mount components.

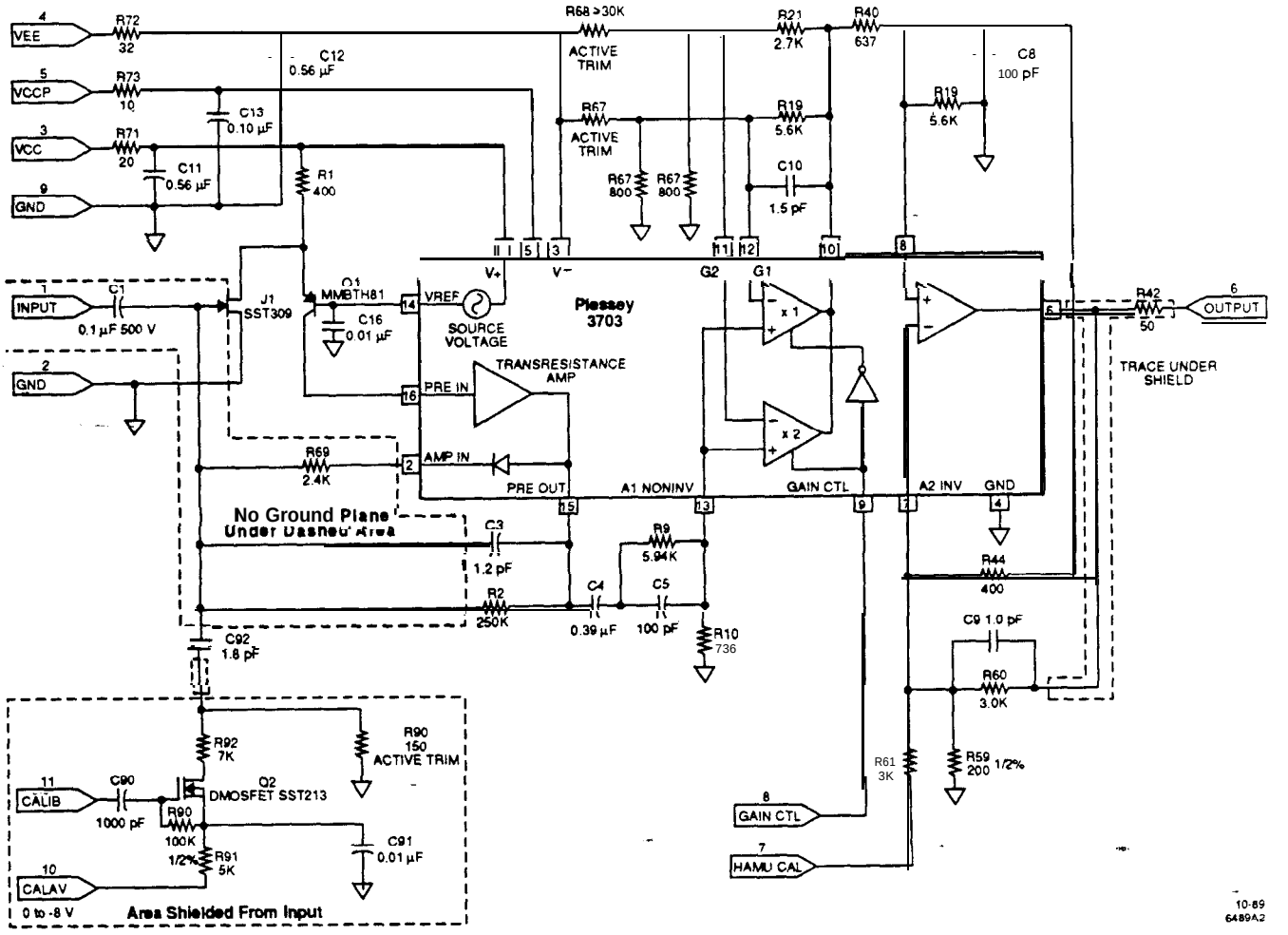

Fig. 5 Schematic of the **CRID** hybrid amplifier.

A. Design

To generate a design of this magnitude requires good tools. In this instance, PSPICE [10] running on a PC was employed, though the computer had insufficient memory to simulate all the circuitry. The best tool, as always, is the ingenuity of the designer, who must simulate the circuit in sections.

Design flexibility for the semicustom integrated circuit is constrained by packaging considerations. The spacing between sense wires requires the same pitch between amplifiers, forcing the use of a 16-pin SO package. Other packages with more pins and transistors are too thick.

The design cycle of the semicustom integrated circuit was very short, taking only one month from final specifications to manufacturer's review. Within a few days, the metallization layout for the integrated circuit was complete and being reviewed. The hybrid layout could then begin.

B. Fabrication

The prototype integrated circuit was delivered in a DIP package,which was inconvenient for system prototyping and led to instability. Compensation capacitors were added to overcome the instability, caused by long leads and bond wires.

Preproduction of 500 surface-mount parts was released in July 1988. They were assembled in Seoul, **Korea,** and unfortunately, delayed because of the closure of the assembly plant during the Olympic games. The prototype hybrid substrates and the integrated circuit preproduction were completed within a few weeks of the games.

Quick turnaround in the testing of our prototype was essential to maintain schedules. Therefore, we chose to modify the prototype hybrids rather than order additional prototypes from the manufacturer. In so doing, we discovered difficulty in making resistor modifications **with** sewing needles and high-speed grinding tools. However. a microscope and diamond scribes were eventually used with great success.

The hybrid circuit is made of an 0.025-inch thick alumina substrate with three conducting layers separated by dielectric and via layers, five resistor paste layers, and a polymer cover on the component side. The back side of the alumina has a ground plane. The component and back side are connected by through holes in the substrate near the ground pins.

All discrete components, IC, transistors, and capacitors are surface mounted. The resistors are printed thick-film resistors that are laser-trimmed to a nominal value before assembly of the hybrid. This passive laser trimming process removes resistor material, thus increasing the resistor's ohmic value.

Three resistors must be actively trimmed to compensate for-hybrid to hybrid component variations. They are the DC offset resistors for both amplifier gains (R67 & R68) and the calibration input resistor (R90). After active trim, these resistors are covered wifh epoxy for long-term stability, and the pins are attached to the hybrid.

Before active trim, a DC-offset-check rejects some of the initially defective hybrids and verifies a successful passive trim.

C. *Trim fixture*

Active trimming is needed (a) to bring the low- and high-gain DC offsets of the hybrid output to the 1.2 VDC necessary for the signal to be within the dynamic range of the HAMU, and (b) to adjust the calibration circuitry.

A trim fixture probe card was designed to condition the hybrid circuit inputs and provide a means to monitor the output of the amplifier while the resistors are trimmed. The design and fabrication of this card became one of the most difficult tasks of this project. Figure 6 is a block diagram of the probe card.

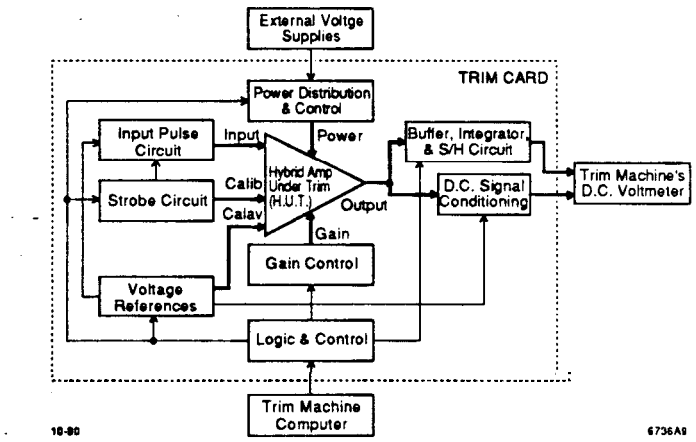

Fig. 6 Block diagram of the trim probe card.

The circuit has its own 1.2 V DC reference which is compared to the buffered output of the amplifier. The resultant error-voltage is amplified, and is read by the voltmeter in the laser trimming machine. Amplifier power is pulsed to minimize DC offset drift due to heating.

The DC offset trim of R.67 and R68 is an iterative process, which is complete when the result is within a few tens of millivolts of the desired goal. Should the measurement result in a value below that desired, the amplifier is rejected as being "over-trimmed." This process is performed in the low- and the high-gain modes, and takes only a few seconds.

To trim R90, thk hybrid calibration circuitry is duplicated on the probe card and connected to the signal input. We then compare the effect of a pulse to the signal input to the effect of a pulse generated by the calibration network itself. Proper attention is paid to the output behavior of a zero-input stimulus in both cases.

To monitor the output of the hybrid and present a corresponding DC voltage to the voltmeter of the trim machine, we integrate the output of the hybrid within a fixed time-window that starts on the application of the input pulse. This need not be done with extreme accuracy; however, linearity, repeatability, and reliability are required.

The integrator is AC-coupled, via a buffer, to the output of the circuit under trim so that the 1.2 V DC offset of the amplifier is not integrated. To avoid the integrator error introduced by bias and leakage currents of the integrator operational amplifier, and the error of using a non-ideal integrator capacitor, the circuit uses a sample-and-hold circuit to get an integrator value at 1.25 μs after the application of the input pulse. The sample-and-hold retains the voltage value long enough for the trim machine's voltmeter to get a proper reading. After the voltmeter reading and prior to the next integration, the integrator capacitor is discharged, the integrator input is grounded, and the sample-and-hold is placed in the sample mode.

The result of pulsing the hybrid circuit creates about 100 mV of noise. The amplifier itself generates noise, and the integrator accentuates the lower frequency components of this noise. Furthermore the XYZ positioner of the trim machine uses an AC electromagnet to hold the platen in the desired position. This AC electromagnet was also a source of electrical noise. Noise problems are reduced by a combination of extensive shielding of the circuit under trim and the sensitive pulse generating and measuring circuits on the trim card, and by making multiple readings and computing an average result in software.

R90 is trimmed until the effect using the calibration input is equal to that measured when the input to the hybrid is pulsed. The difference between the two measurements determines the length of the laser cut, and the number of pulses applied to the CALIB input whose effects are averaged before the next trim. The trim length decreases and the number of samples taken increases in three steps, as R90 increases towards its final value. By making the number of samples measured variable, the overall trim process consumes much less time than if it were constant. Sometimes the noise causes the intermediate trim step to be omitted, but the fine trim step is always performed. A successful trim of an amplifier takes about 30 seconds and is limited by the Z80 microcomputer used by the laser trim machine.

D. Testing

A simple functional tester-based on an IBM compatible PC with a Data Translation I/O card and a custom built interface-was designed and two were built. One was installed at the manufacturer's plant for final inspection; the other is at SLAC for incoming inspection. The unit installed at the vendor was adapted to test the hybrids without pins before they are actively trimmed.

IV. Amplifier Motherboard

Figure 7 is a block diagram of the amplifier motherboard. For clarity this subsystem can be viewed as four different sections; a control and buffer, inner and outer sections, and a wire heating daughter board.

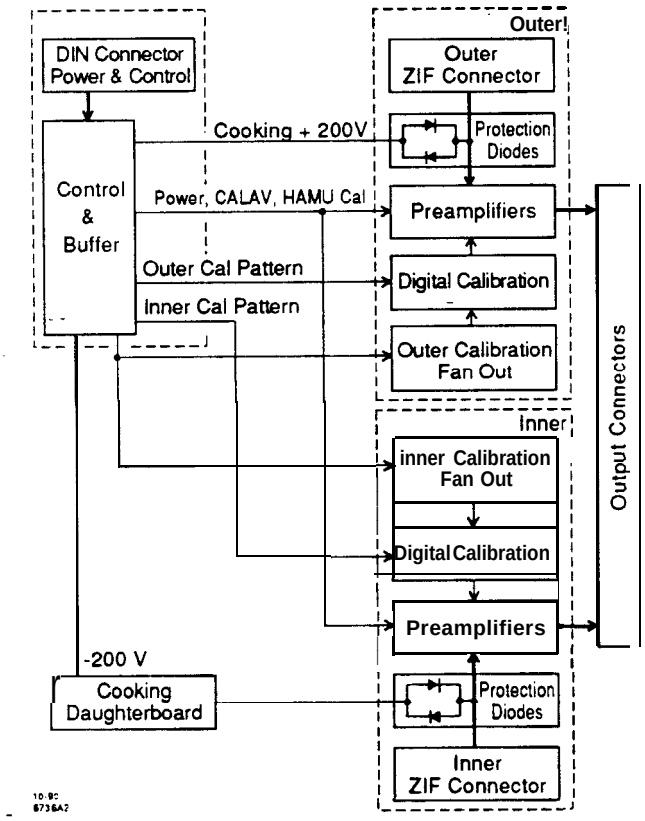

Fig. 7 Amlifier motherboard block diagram.

The signals from the detector are input to the motherboard via Zero Insertion Force (ZIF) connectors on both the inner and outer sides. These connectors were chosen to prevent stressing the PC boards connected to the fragile 7 pm-diameter sense wires. These signals go directly to the amplifier input. Back-t-back diodes, also connected to the input of the amplifier, serve a dual purpose; as protection diodes, should a sense wire become shorted to the high voltage, and as a means of applying a voltage to the sense wires to burn off polymer deposits.

The digital calibration circuits on the motherboard are used to select which channels will be calibrated by a calibration pulse. They consist of a 93-stage CMOS shift register (4094), which selects CMOS double-pole single-throw switches (74HCT4053) that connect the hybrid's CALIB input to either ground or the calibration pulse. A reshaping circuit (called the Fan Out block in Fig. 7) is used to retain the fast rise time of the calibration pulse.

Signals from the sector controller are buffered in the control and buffer section. Instrumentation amplifiers (AD524) drive the CALAV and HAMU-CAL inputs of the amplifiers.

The carbon sense wires may need to be cleaned of polymerized deposits. This is implemented by passing a current of about 10 mA through the fibers. The 400 V required is generated by applying +200 V at one end of the fibers and -200 V at the other. However, the power dissipation inside the detector must not exceed 25 W; therefore, we can apply this current, to no more than six fibers at a time. Should we elect to clean the fibers, the positive voltage is applied to all fibers simultaneously and the negative voltage applied to the selected group. This selection is controlled by a shift register whose output drives a transistor buffer driving the gate of a FET switch.

A. Design

The circuit, design of the amplifier motherboard was straightforward, and the repetitive schematic capture was done by a student working part-time using ORCAD/SDT III [11].

The printed circuit layout was much more challenging. By using both sides of the board to mount components, we were able to fit all of them on the board.

The design uses eight layers; one layer for each of the amplifier's three power supply voltages, and one analog ground; two layers for calibration circuitry; one layer for the amplifier's input and output; and a layer with miscellaneous voltages and buss lines. We specified the manufacturing requirements, such as no buried vias, and to limit the number of blind vias. Additional ground traces were placed between amplifier's input and output traces to reduce channel-to-channel crosstalk.

The CAD system used for this and many other designs for the CRID electronics is a PC-based PADs-PCB package [12]. Using this software, the design took less than two weeks for a partial review, and less than two month for final films.

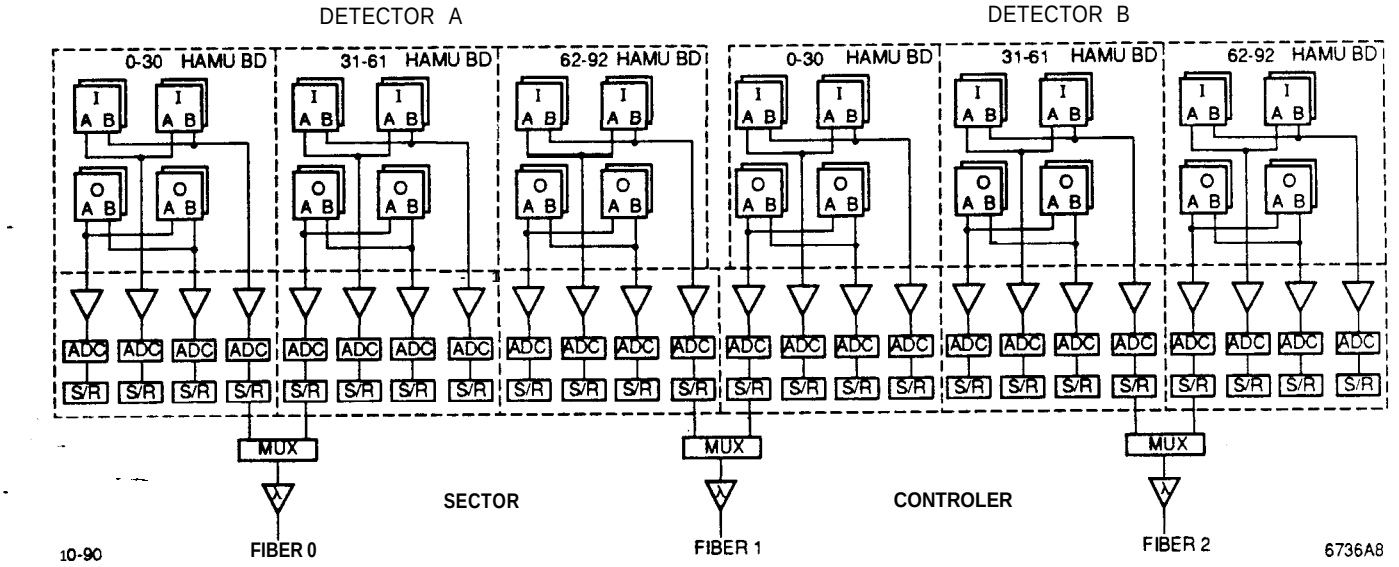

Fig. 8 HAMU/ADC system block diagram.

B. Construction

Two prototype motherboards were fabricated at SLAC. The testing went very smoothly and no layout error was found. However, minor design changes were necessary, such as changing the position of two voltage planes in order to reduce power switching transients at the input of the amplifier, and rerouting the traces for the calibration pulse so that the propagation delay be equalized between inner and outer channels.

The production of 44 boards, including 10% spares, was awarded to a local company. Continuity and short-testing were specified. The production yield was a disappointing 70% due to the density of our design. Standard eight-layer board fabrication will generally have 90% or higher yield.

The shields soldered to the motherboard between each hybrid are 0.15 inches high, 0.015 inches thick and 1.2 inches long. They were individually hand-wrapped with mylar tape. At $0.50 each, this procedure was far less expensive than hi-tech dipping and other solutions proposed.

Component loading of the motherboard proved to be another painful experience. Loading one prototype was done in-house and took nearly two weeks. There were several problems. The output connectors from the amplifiers to the HAMU boards have a 0.050 inch pitch between contacts, and were hard to install due to a PC- board layout error that was not noticed during verification. There are also surface-mount components interspersed with leaded components on both sides of the board, making a standard assembly processes difficult to implement.

The main production problem encountered in testing the motherboard was a serious crosstalk between the calibration strobe and some of the amplifier's input. This was rectified by replacing several printed circuit traces with mini coaxial cables and adding shielding near the ZIF connectors.

V. HAMU/ADC

Figure 8 is a block diagram of the HAMU/ADC subsystem. The output from the amplifiers is fed to the HAMUs via a small PC board with traces spaced 0.050 inches apart, having alternate signal and ground traces. Each HAMU has eight channels. Each channel has two AMUs [13], A and B, which both provide 256 time samples. In write mode, the two AMUs are addressed in an interleaving mode by a TTL shift register located on the HAMU, so that the first time sample is recorded in AMU-A, the second one in AMU-B, and so on. All HAMUs are written in parallel, and read out sequentially at a much slower rate, one channel at a time. The A and B AMUs are read in parallel, and their outputs are digitized by two separate ADCs.

Each detector requires 24 HAMUs, 12 for the inner channels, and 12 for the outer channels. For modularity and manufacturing cost reduction, we packaged eight HAMUs per board. Each board contains buffers, gating for readout sequence, and FET switches for pulsed power.

The ADC boards provide the analog-todigital conversion for the HAMU output, and parallel to serial conversion of the digitized data. The serial data outgoing the ADC board are 12-bit interleaved words from inner and outer channels. It also has the voltage regulators, I/O buffers, and output transimpedance amplifiers for the HAMU current source outputs. The ADC boards also transmits control and clock signals from the sector controller to the HAMU boards.

The circuit design for these two boards was straightforward. One of the specifications that needed change was caused by a system design oversight. When the pulsed power to the amplifier is off, its output drops below zero volts and discharged the data stored in the AMUs. This was corrected by inserting diodes to clamp the HAMU inputs to a small positive voltage.

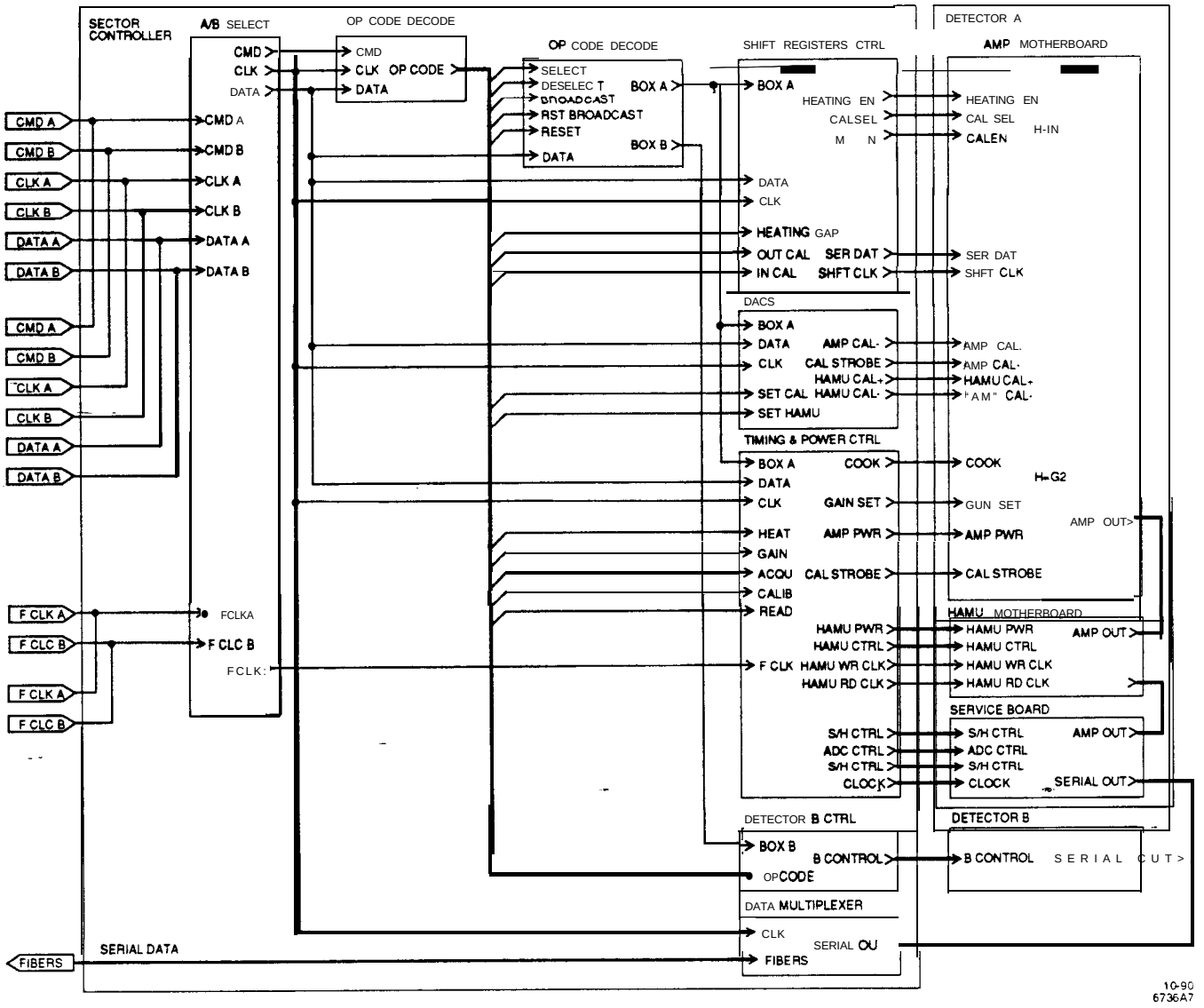

Fig. 9 Sector controller block diagram

Since the HAMUs are sequentially powered on and off during readout, we provide two power planes on the HAMU board to minimize switching transients. Two ground planes, one for analog and one for digital, are also provided with provision for jumpers between them. The analog ground is connected to the amplifier motherboard and the digital ground to the ADC board. The HAMU itself has only one ground plane. At present, the two ground planes are connected together. Support circuitry for the HAMUs (buffers, gates, and FETs) is mounted underneath the HAMUs. During assembly, these components are soldered on the board; the board is then tested at SLAC. After testing, they are shipped back to the assembly house for final assembly with HAMUs and the input connector.

The ADC board is a conventional surface-mount PC board. The components are mounted on one side, so that the back side can rest on a metal plate which shields the amplifiers from the digital electronics.

VI. Fiberoptics Receiver Board and Sector Controller

Digital control signals from the TCM are transmitted to the sector controllers via the fiberoptics receiver boards, which converts the optical signals to differential ECL.

The ECL three-wire protocol signals are daisy-chained to all sectors, and are then terminated on the fiber optics receiver board. The fast clock is distributed to each sector via an individually shielded twisted pair, which is terminated on the sector controller.

A block diagram of the sector controller is shown in Fig. 9. The sector controller serves two purposes. It interprets signals from the three-wire protocol to control the two sets of front-end electronics within the sector, and it multiplexes the data from the two drift boxes and transmits them via fiber optics to the FASTBUS data processing plant.

The sector controller is the interface between the CRID system and the general SLD data acquisition system. It adds three framing and parity bits [14] to the data stream from the ADC boards. It also features a test mode wherein a test pattern, rather than the raw data from the detector, is transmitted to the data processing system.

The sector controller receives the serial data from each ADC board within the sector (Fig. 8). It multiplexes this data and sends it to the WSM auxiliary board on three optical fibers. The data from the six ADC boards is multiplexed onto the three fibers by interleaving bits alternately from adjacent boards. The transmission rate between the sector controller and the FASTBUS plant is 16 Mbits/s

The design of the sector controller makes extensive use of programmable logic devices. An Altera 1800 performs the three-wire protocol decoding, while a faster Altera 900 device provides the read mode sequencing. Programmable Array Logic (PAL) devices are used for parity generation and counting functions. Four Digital-t@ Analog Converters (DAC) are used for the amplifier and HAMU calibration.

VII. Low-Voltage Distribution

The low-voltage distribution within a sector is provided by two PC boards; the low-voltage distribution board and the voltage regulator boards. The first receives and filters the raw voltages from outside SLD, and provides energy storage for amplifier and HAMU pulsed power. Overcurrent protection on this board is provided by Raychem [15] polyswitches. The second board, connected to the low-voltage distribution board and to the sector controller, serves two purposes. It regulates the voltages required by the amplifier motherboard, including pulsed power. It also passes signals from the sector controller to the amplifier motherboard, and to the ADC boards. This board is mounted vertically, as shown in Fig. 4, and provides mechanical support for the PC board stack.

VIII. Grounding and Shielding

The design of the grounding and shielding began early in the design phase. The CRID electronics reside within an effective Faraday cage. Each sector has a single-point star ground.

Figure 10 is a schematic of the grounding scheme. The sector and the Faraday cover are shown with heavy lines. All cables entering the Faraday cage are shielded with the shield terminated at the entry point with SUNBANK [16] bulkhead adaptors. The Faraday cage described above is a copper mesh, with RFI gaskets coupled to the SLD steel structure. The final test of the effectiveness of the grounding and shielding scheme will take place during SLD commissioning.

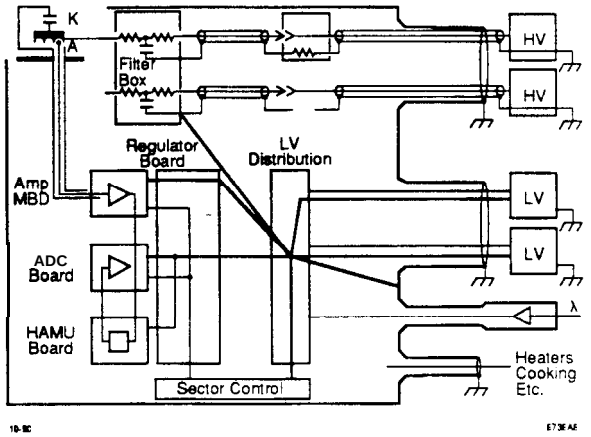

Fig. 10 Grounding and shielding schematic.

IX. Cooling

The power dissipation in each sector is about 100 W. Packaging density does not permit convection cooling of the circuits. A low flow-water system cooling has, therefore, been developed to remove the heat generated by the electronics.

A compact water distribution systems has been designed. The cooling water is in contact with anodized metal fins, as shown in Fig. 4. These fins, placed between amplifier hybrids, provide low-temperature conduction cooling to each amplifier and serve as additional RF shields. The water flows to the sector through plastic hoses so that the water pipes used in the manifold do not act as antenaes, which would bring RF signals to the sensitive front-end electronics. A steady-state operating temperature below 40°C is expected.

X. Conclusion

We have sucessfully developed and constructed an electronics system for the CRID. A number of challenging circuit and packaging problems were solved, using a mixture of common and state-of-the-art technologies. The performance of the system meets all of the electronic and mechanical specifications.

Acknowledgments

The authors gratefully acknowledge all the members of the CRID collaboration for their numerous contributions. We would like to extend special thanks to J. Va'Vra and A. Bean for their technical contribution, and to D. Leith and L. Paffrath for their continued support.

Disclaimer

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