The readout system based on the ultra-fast waveform sampler DRS4 for the Large-Sized Telescope of the Cherenkov Telescope Array

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Abstract. The Cherenkov Telescope Array (CTA) is the next-generation ground-based very-high-energy gamma-ray observatory. By using three types of telescopes CTA can cover a wide energy range (20 GeV–300 TeV) with an order of magnitude higher sensitivity than the current telescopes. The Large-Sized Telescope (LST) is designed to detect 20 GeV–1 TeV gamma rays thanks to the large light collection area, sensitive photosensors, a fast trigger system, and readout electronics. The camera readout system must have a high signal-to-noise ratio and a linear signal sampling with a large dynamic range in order to efficiently detect dim and low-energy atmospheric showers. To meet this requirement we use the Domino Ring Sampler version 4 (DRS4), which also enables ultra-fast sampling with low power consumption. Some of the intrinsic characteristics of DRS4 chips require software corrections. These procedures lower the effect of non-Gaussian noise contribution and improve the timing resolution of the system. In this contribution we discuss the calibration algorithms and the resulting performance.

1. Introduction

The Cherenkov Telescope Array (CTA, [1]) is the next-generation ground-based observatory for gamma-ray astronomy at very-high energies, and Large-Sized Telescopes (LST) are the largest telescopes planned for CTA. The camera for an LST has 1855 Photomultiplier Tubes (PMTs) and each cluster of seven PMTs is connected to a readout board [3] (See Figure 1). The pulse width of Cherenkov signal is very narrow (a few ns), so we sample those signals with 1 GHz frequency using DRS4 chip[2]. Each DRS4 chip has 8 usable channels, each being an array of 1024 capacitors. Input voltage is sampled by using an inverter chain, which then can be read out at 33MHz and digitized by an external ADC chip for low power consumption. We use a cascade of four channels to read out a single pixel for increasing the depth of the readout. Each pixel is read out with two gains for a larger dynamic range.

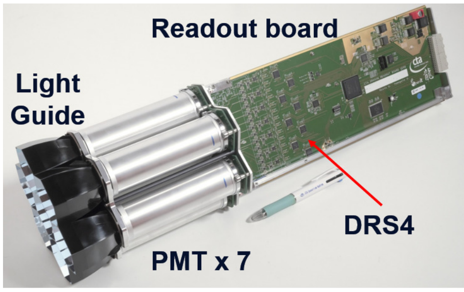

Figure 1. One of 265 PMT modules of LST camera. Each readout board is connected to seven PMTs with light guide. 8 DRS4 chips are used in each module.

2. Low level calibration of DRS4 analog output

DRS4 has non-Gaussian noise contribution even after the subtraction of the offset for each capacitor. The first noise component might be due to the residual electrical charge resulting from the last readout with respect to each capacitor. Figure 2 (Left) shows the relation between ADC counts and time lapse from the last readout of each capacitor, which can be expressed by a power-law function [4]. The second component is a spiky ADC feature which could be generated by remaining read bit at the last readout, so the spike position depends on the last capacitor of the last readout. These features appear without exception, so we can compensate for them (See Figure 2 (Right)). The readout voltage is affected by temperature. During regular operations the readout is powered at least an hour before the observations to stabilize the temperature. The cooling system allows us to maintain the temperature within $\pm$ 5 degrees, which allows the baseline offsets to be kept stable at the level of 0.1 photoelectron (p.e.). Those features affect multiple slices, so charge integration by a few slices could catch a somewhat bigger effect.

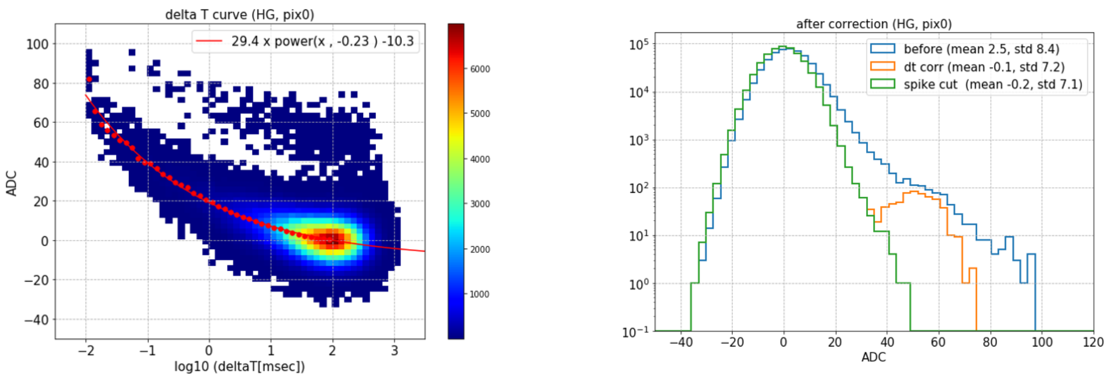

Figure 2. Results of low level calibration of a given DRS4 chip. The pulse height of single photoelectron corresponds to 30 ADC (0.26 mV/ADC). (Left) The relation between readout voltage and time lapse from the last readout with respect to each capacitor. Outliers above the power-low distribution are spike events. (Right) Noise distribution before correction (blue), after time lapse correction (orange) and also with spike cut (green). The noise level of this chip is 7.1 ADC (0.24 p.e.). See Section 4 about the mean noise level for all pixels.

3. Timing calibration of DRS4

The frequency at which DRS4 samples waveforms is not constant and changes from one capacitor to another by about 10%. The arrival time of signals also depends on the absolute position of capacitors due to this effect and it can be calibrated with calibration laser(See Figure 3). We can also calibrate the intrinsic time lapse for each capacitor by counting the pulse peak position at given capacitor in the data with calibration pulse. If the lapse is longer, the pulse signal can be stored in that capacitor with higher probability. This calibration can improve the charge resolution because it corrects for waveform distortion due to uneven sampling.

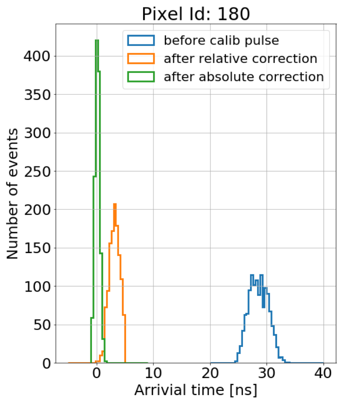

Figure 3. Arrival time distribution of calibration pulse before correction (blue, standard deviation(std)=1.7 ns), after relative correction(orange, std=1.0 ns) and absolute correction(green, std=0.4 ns). The pulse signal is located at the position of 28.5 ns in the readout window (40 ns). This pulse position depends on the position of DRS4 capacitors, so it can be calibrated by Fourier expansion of the arrival time (relative correction)[4]. It also depends on the fluctuation of calibration laser and trigger system, so those effect can be compensated by comparing the data of all pixels (absolute correction).

4. Noise level in CTA-LST

We studied the contribution to noise level from each component in CTA-LST. The data for this study was taken when the telescope was at parking position (zenith angle=95°) with different conditions (High Voltage on/off, shutter close/open). Then we found the total noise is 0.98 p.e. level, which comes from electronics (0.20 p.e.), High Voltage ($\leq$ 0.01 p.e.) and Night Sky Background (0.96 p.e.).

5. Conclusion

We are in the commissioning phase of CTA-LST and have developed the low level calibration algorithms for coming scientific observation. The analysis procedures are currently being finalized, and performance of the readout board has been presented.

Acknowledgments

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