A Digitization Scheme of Sub-microampere Current Using a Commercial Comparator with Hysteresis and FPGA-based Wave Union TDC

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ABSTRACT: A digitization scheme of sub-microampere current using a commercial comparator with adjustable hysteresis and FPGA-based Wave Union TDC has been tested. The comparator plus a few passive components forms a current controlled oscillator and the input current is sent into the hysteresis control pin. The input current is converted into the transition times of the oscillations, which are digitized with a Wave Union TDC in FPGA and the variation of the transition times reflects the variation of the input current. Preliminary tests show that input charges <25fC can be measured at >50M samples/s without a preamplifier.

KEYWORDS: Front-end electronics for detector readout; Digital electronic circuits.

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Contents

1. Introduction

Digitizers interfacing directly to current sources are particularly useful in high energy physics since signals from many commonly used detectors are fast charge movements. In accelerator protection instrumentations, on the other hand, signals could be relatively slow changing small currents that also favour a direct connection to a current sensing digitizer.

Most modern digitization systems consist of three circuit stages: (1) the front-end electronics, such as pre-amplifiers, shapers/filters, etc., (2) the digitization or analogue to logic level conversion devices and (3) the digital (logic level) data processing FPGA. Given that the data processing FPGA stage is indispensable, it is more convenient to place more digitization functions into the FPGA so that the front-end and the digitizer stages can be simplified.

One of such possibilities is to implement time-to-digital converters (TDC) inside the FPGA [1-6] while translating signals to be measured into time using analogue-to-time converter (ATC). Popular ATC schemes include the Wilkinson ADC, ramp-compare ADC, recycling integrator, etc. [7-12] and many ATC schemes simply use comparators, either separate IC chips or even the FPGA LVDS receivers to transform the analogue information into the times of the logic level transitions. It is also commonly seen that a comparator-based scheme significantly reduces requirement for the front-end electronics stage, if not completely eliminates the front-end stage.

In our scheme, a current controlled oscillator is built using a comparator (Analog Device Inc. ADCMP605 [13]) and its oscillation frequency is determined by the input current into its hysteresis pin. The LVDS output of the comparator is sent to an FPGA and the oscillation logic transition times are digitized with the Wave Union TDC inside the FPGA. There is no preamplifier in our test.

Wave Union TDC [5] is a scheme developed in our previous work to improve the resolution of the TDC implemented in the FPGA beyond its cell delay. Multiple 0-1 and 1-0

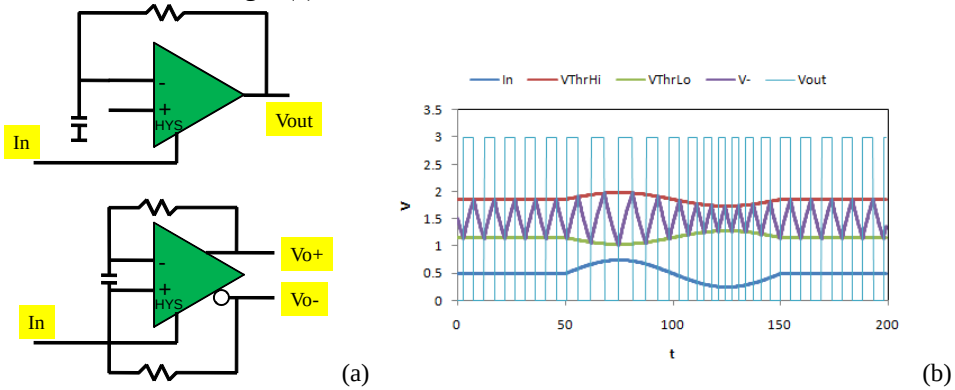
transitions are generated in the delay chain in the Wave Union TDC and registered for encoding, which effectively provides multiple measurements with one set of delay chain and register array structure and thus improve time measurement resolution. (Note that regular TDCs make one measurement with a single 0-1 transition.) Intrinsically, the Wave Union TDC is a low-resource and low-power consumption scheme since less logic elements are used comparing to typical TDC schemes in order to achieve a finer resolution. A time measurement resolution better than 30 ps (standard deviation) can be achieved in low cost FPGA devices carrying multiple channels, which exceeds requirement for this application.

In this paper, the current-to-frequency converting oscillator implemented with the comparator is first discussed in Section 2 followed with a short description of the Wave Union TDC in Section 3. Test results of the standard deviation of the measurements and the sampling rates are presented in Section 4. The vision of comparator-based ADC scheme as a deviation from deep negative feedback analogue design practice is discussed in Section 5.

2. The Current-to-Frequency Converter

2.1 The Oscillator Circuit

Current-to-frequency converting oscillators are built with comparators plus a few passive components as shown in Fig. 1(a).



(a) (b)

Fig. 1. The current-to-frequency converting oscillators (a) and the oscillation frequency changes according to the input current (b)

The comparator device accepts a small current and converts the current into the hysteresis that causes variation to the high and low thresholds of the comparator. The oscillator circuit can be in single-ended version (using ADCMP601) as shown in top of Fig. 1(a), or in differential version (using ADCMP605) as shown in bottom.

The oscillation frequency changes according to the input current as shown in Fig. 1(b). For simplicity, the single-ended configuration is shown, but the operation of the differential version is similar. When the output of the comparator is in the low state the capacitor discharges toward lower voltage. Once the input voltage at the negative input pin (V-) passes through the low-state threshold (VThrLo), the comparator flips to high state. The capacitor then charges to higher voltage until it passes through the high-state threshold (VThrHi). The process repeats and the oscillation frequency is correlated with the input current. The transition times of the comparator output are digitized and from the transition times and the circuit time constant, it is possible to reconstruct the input waveform.

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2.2 Hardware Details

The control range of the current input in HYS pin is from 0 to -18 μA which provides a hysteresis voltage from 0 to around 230 mV. In our tests, the differential version built with ADCMP605 is used to reduce noise of the ground plane and there is no pre-amplifier used. The input is biased with a DC current of around -6 μA. The resistors and the capacitor values and the nominal bias current are chosen so that the oscillating frequency of the oscillator operates in a range of 10 to 60 MHz, corresponding to sampling rates of 20 Ms/s to 120 Ms/s. The outputs of the oscillator are sent out through a 50 Ohms serial resistor in each output pin that matches the impedance of the printed circuit board traces. The response of the oscillator to a waveform of the input current is shown in Fig. 2.

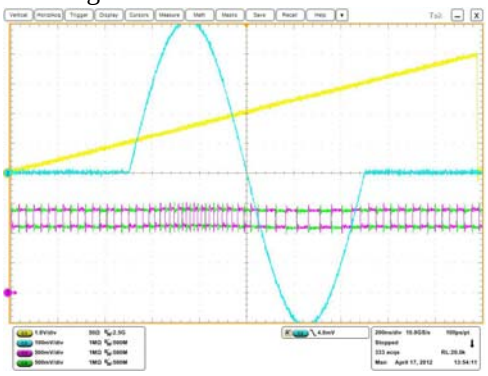


Fig. 2. The response of the oscillator to a waveform of the input current: Ch1: a sweep voltage indicating the pulse time, Ch2: the input signal, Ch3, 4: comparator outputs.

It can be seen that when the input current stays at its nominal bias, the oscillator runs at its nominal frequency of approximately 16 MHz, corresponding to 32 Ms/s. A relatively low oscillation frequency is chosen here to get a better clarity in the oscilloscope screen capture for demo purpose. If input current changes, the output oscillating frequency deviates from nominal oscillating frequency. The input amplitude (5 μA, peak-to-peak) used here is significantly larger than normal operation to show larger oscillating period change again for demo purpose.

3. The Wave Union TDC

A special feature of the FPGA TDC is its large differential nonlinearity (DNL) as shown in Fig. 3(a) which is represented as apparent width of each TDC bin.

The most significant origin of DNL is the logic array block (LAB) structure. When the input signal in the carry chain passes across the LAB boundaries (and also the half-LAB boundaries in some FPGA families), extra delays added cause periodic “ultra-wide bins.”

In our previous work [5], an approach called the “wave union TDC” was developed to sub-divide the ultra-wide bins and to improve measurement resolution. The key part in the wave union TDC is the “wave union launcher” as shown in Fig. 3(b). A wave union launcher creates a pulse train or “wave union” with several 0-to-1 or 1-to-0 logic transitions for each input hit and feed the wave union into the TDC delay chain/register structure, making multiple measurements. As shown in Fig. 3(a), effectively the “ultra-wide bins” are subdivided using the wave union TDC scheme.

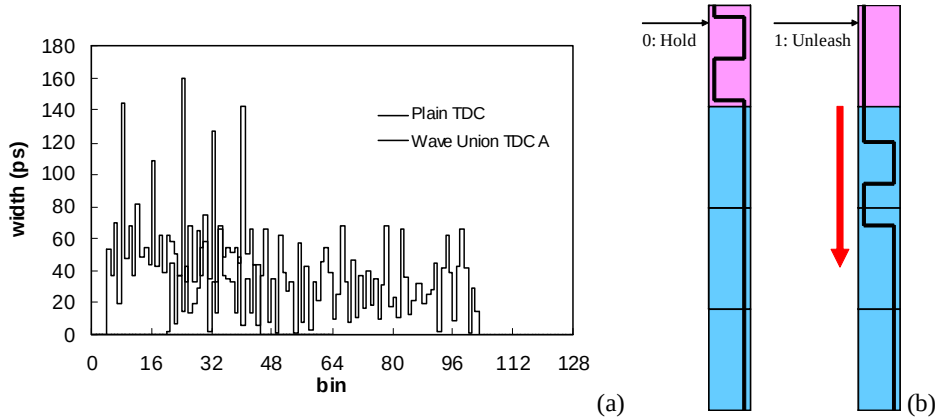


Fig. 3. The bin width plot (a) and a wave union launcher (b)

A time measurement resolution better than 30 ps (standard deviation) can be achieved in low cost FPGA devices with multiple channels.

4. Test Results

The digitization scheme has been tested in various configurations including single pulse digitization, measurement of timing jitters and other aspects of measurement precision. These tests are discussed in this section.

4.1 Waveform Digitization

In the waveform digitization test, times of oscillating transition edges are measured. The test input pulse is a single cycle sine wave with peak current 200 nA and base width 2x200 ns as shown in Fig. 4. The charge transported in the pulse is +-200 nA x 200 ns x 0.64 = +- 25 fC.

The test system is first calibrated during which both periods between upward and downward edges are measured at various known input DC current. The converting factor between the input current and the deviation of the oscillating period is then calculated. At 53 Ms/s, the converting factor is approximately 5.9 ns/μA.

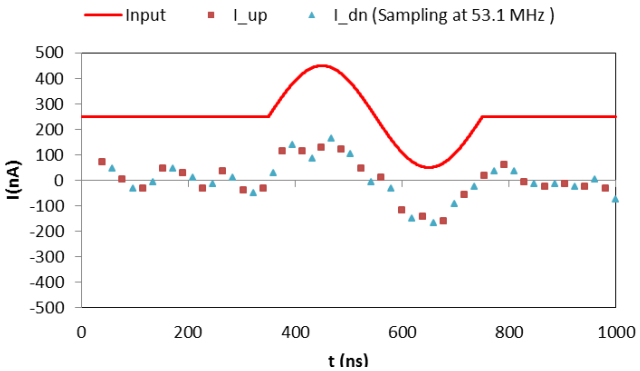


Fig. 4. Digitization of a single pulse

The periods between pairs of upward and downward edges deviating from the nominal values are converted into unit of current and plotted in Fig. 4 as squares and triangles marked with “I_up” and “I_dn”. It can be seen that the charge movement is clearly visible above the baseline noise with nominal sampling rate of 53.1 Ms/s.

4.2 Measurement Precision and Trade-off Between Sampling Rates and Precisions

To understand measurement precision of this scheme, the timing jitters of the oscillator transition edges are measured with DC current inputs. The measured pulse width jitter is 280 ps (standard deviation) for the oscillator configuration at 53 Ms/s. Clearly the FPGA TDC's with measurement resolution better than 30 ps satisfies the requirements easily. With conversion factor 5.9 ns/μA, the current measurement jitter is approximately 47 nA. We can further define a product of the 3-sigma current X sampling interval as an estimate of minimum detectable charge movement (if the charge profile is sufficiently fast). In our test this value is 3*47 nA* 19 ns = 2.7 fC.

Depending on the specific applications, the users may wish to optimize their measurements for finer precisions or faster sampling rate. An example is shown in Fig. 5.

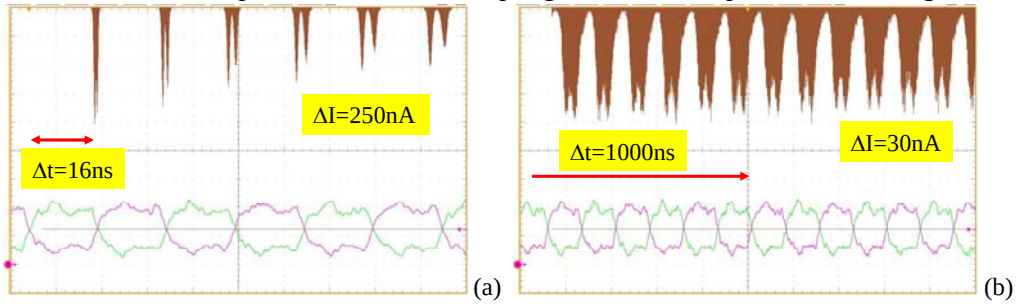


Fig. 5. Measurement resolutions with different sampling intervals: (a) high sampling rate cases and (b) low sampling rate cases.

In the test, two values of currents are alternatingly sent into the oscillator and histograms of the transition times of various transition edges are booked. The current value differences are 250 nA for Fig. 5(a) and 30 nA for (b). It can be seen that the precisions of the two peaks becomes better and better as the sampling interval becomes longer and longer.

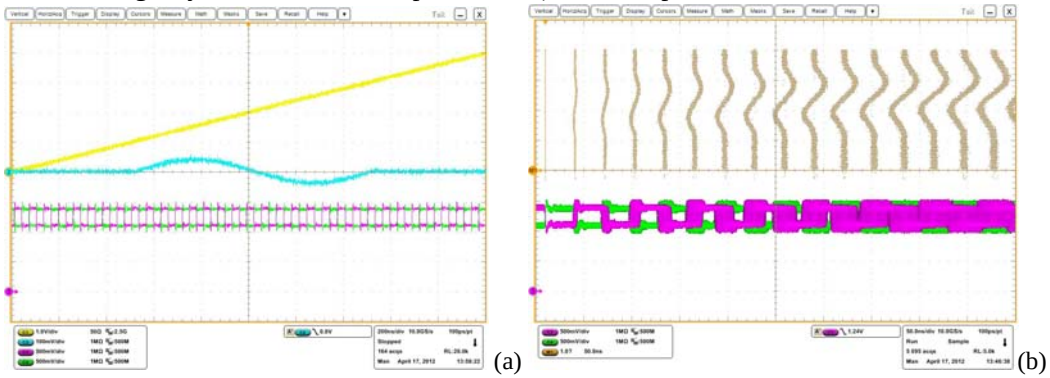
Consider time interval T(n) between edge 0 and edge n, the measurement sensitivity: $\Delta T(n)/\Delta I$ is proportional to n. On the other hand, the timing jitter of the edge $\sigma(T(n))$ also increases with n, but relatively slowly, usually is with square root of n.

When the users need a finer measurement precision for a DC or slowly changing current, a slower sampling rate can be chosen which can be done with the post process inside FPGA or offline analysis. The simplest approach is to use time differences between transition edges of multiple oscillating cycles apart. For example, the edges shown in Fig. 5(b) are >60 oscillating cycles away from the previous sampling edge (the trigger edge of the oscilloscope). In real post processing firmware, information provided by the transition edges in the middle can also be better utilized for even better measurement precision by using low-pass digital filter based post process methods (the decimation process). In the example given in our test, the anticipated current measurement precision is 6.5 nA (standard deviation) at 1 Ms/s, improving from 47 nA at 53 Ms/s.

When a faster sampling rate is chosen, the current measurement precision is coarser. However, faster sampling rate provides a finer charge measurement precision (if the charge profile is sufficiently fast).

4.3 Precisions and Sensitivities of Different Transitions

As mentioned earlier, the timing precisions and measurement sensitivities for sampling between different transition edges are different. For better understanding and visualization, a "group dance" plot of an input pulse is produced from the oscilloscope as shown in Fig. 6. The input pulse is a single cycle sine wave with period of 1 μs, and amplitude +- 200 nA.



(a) (b)

Fig. 6. Oscilloscope traces of the input pulse (a) and the "group dance" plot (b).

The transitions of the oscillator outputs are fed into channel 3 and 4 while a sweep voltage synchronized with the input pulse are fed into channel 1. The Math channel M1 is set with M1 = CH1*AND(CH3>1.24,CH3<1.26) (Note that the 50% level of CH3 is 1.25V).

With this setting, each logic transition edge produces a dot in a 2D area with horizontal axis being the transition time of the logic transition edge while the vertical axis being the input pulse time. The display of the oscilloscope is set to infinite persist mode. After sufficient long acquisition time, each band of the M1 plot represents the transition time of a transition edge and the vertical axis scale of M1 is 2 μs, which is the full scale of the sweep voltage feeding into CH1.

It is clear that the timing precisions of transition edges become coarser when the time differences between edges become larger, so that the vertical M1 bands become wider and wider from left to right. On the other hand, the waving amplitude of each band is proportional to the sensitivity which becomes larger and larger from left to right. It can be seen that the increasing of the waving amplitudes is more significant than the increasing of the widths of the bands so that it is easier to see the pulse shape for the bands far from the trigger edge.

Note that the "group dance" plot shows the results of many acquisitions. It is a tool to visualize the relationship between measurement precisions and sensitivities but is not to be used to evaluate single shot digitization performance.

5. Discussions

It is useful to review the intrinsic advantage behind this and other ADC schemes using comparators. We subconsciously apply deep negative feedback when we design analogue circuits. However, the benefits of negative feedback such as better gain stability, linearity and bandwidth are secondary in digitization tasks since all waveform distortions can be calibrated in digital domain. The primary goal of processing weak signals is to amplify them before they are contaminated by the noise. Using a comparator, the difference of the input signals is fully amplified with its open loop gain near the voltage crossing point. So a design strategy deviating from negative feedback is the primary reason of this achievement.

Acknowledgments

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