ARCHITECTURE OF THE BABAR ELECTRONICS SYSTEM

A.J. Lankford, Department of Physics and Astronomy, University of California, Irvine, CA 92697-4575 (email: lankford@lankford.ps.uci.edu)

and the *BABAR* Collaboration

Abstract

An overview of the Electronics System for the *BABAR* Experiment, emphasizing architectural issues and development of new components, is presented. The *BABAR* architecture is quite similar to the architectures planned for the LHC. It is multilevel, pipelined, and nearly deadtime-free. An unusual level of standardization has been achieved across front-end electronics subsystems. Buffer architecture, links and protocols, readout module, and interfaces to timing, DAQ, and controls are all standardized. Seven custom integrated circuits have been developed to tailor the architecture to the detailed characteristics of, and to realize the full performance of, the *BABAR* detector systems.

1. INTRODUCTION

The *BABAR* Experiment will study CP violation at the SLAC B-Factory. Its detector consists of five major systems: a silicon vertex tracker [1], a cylindrical drift chamber with dE/dx capability [2], a particle identification system (DIRC) based on imaging of Cerenkov rings [3], a cesium-iodide crystal calorimeter [4], and a muon identification system (IFR) based on resistive plate chambers [5]. The specialized requirements of each detector system are addressed by front-end electronics customized to the detector technology but integrated into a uniform data acquisition architecture.

2. OVERVIEW OF ARCHITECTURE

BABAR has adopted a two-level trigger and data acquisition architecture. At Level 1, the trigger is optimized for simplicity and speed. It is based on a reduced set of detector data from the drift chamber and calorimeter. It consists of a pipelined, hardware processor and is nearly without deadtime. Its latency is 12μsec, and it is designed to provide an output trigger rate of less than 2kHz. During the level 1 latency, the full detector data sample is held in circular buffers. At the final level, which is referred to as Level 3, the data acquisition system assembles events over a commercial network into the memory of a farm of level 3 processors. The level 3 output rate is expected to be about 100Hz. The level 3 trigger, or Online Event Processor, performs final event selection in commercial CPUs working with the complete set of detector data. The level 3 trigger is followed by online prompt reconstruction in the same farm. The architecture is designed to accommodate an optional Level 2, operating over the same network, if unexpected background conditions demand higher performance.

Although *BABAR*'s architecture greatly resembles those designed for the LHC, it includes some unusual characteristics. The 12μsec level 1 latency is relatively long, but can be accommodated because all level 1 latency buffers are digital. Long latency simplifies and reduces the cost of the level 1 trigger. A minimum level 1 trigger spacing of 2.2μsec is enforced. This spacing simplifies logic design of the readout ICs, because each datum in the silicon tracker and drift chamber is then associated with only one level 1 accept; whereas, it introduces minimal deadtime, 0.4%. *BABAR* has no fast counters for triggering purposes, and bunch crossings are nearly continuous at 4ns. Hence, the timing of the trigger must be derived from the chamber, as part of track segment reconstruction, and from the calorimeter, as part of waveform processing. The resolving time of the trigger is approximately 150ns worst case. A window of data centered on the estimated trigger time, and covering several times this value plus the detector resolving time, is read out for each detector. For instance, this window is about 500ns wide for the silicon vertex tracker and 4-16μsec wide for the calorimeter. The precise event time is determined off line.

3. DETECTOR-SPECIFIC ELECTRONICS SUBSYSTEMS

All detector-specific, or front-end, electronics subsystems of *BABAR* share a common architecture. Each front-end chain consists of an amplifier, digitization (discriminator or flash ADC), a circular buffer (to store data during level 1 latency), and a derandomizing buffer (to store data between the level 1 accept and transfer to a Readout Module). Analog signal processing, digitization, and data readout occur simultaneously. All front-end subsystems except the IFR provide data sparsification. All level 1 latency buffers are digital; hence, it is possible to store data longer than analog buffers would

allow. The buffers of all front-end systems are managed by a common protocol. All level 1 latency buffers function as pipelines of fixed length, and all derandomizing buffers function as FIFOs which are capable of storing a fixed number of events, regardless of the actual implementation of the buffers. Each detector-specific subsystem also shares standard *BABAR* interfaces to the detector-spanning, or common, electronics subsystems. In all cases, the front-end electronics is mounted directly on the detector for performance reasons. This solution also substantially reduces required cable plant. The design of each detector-specific subsystem balances its individual and common requirements in order to achieve a cost-effective, robust, and easy to maintain implementation. Custom integrated circuit solutions have been adopted for most subsystems.

3.1 Silicon Vertex Tracker Electronics

The Silicon Vertex Tracker (SVT) Electronics must record hits with coarse (~4-bit) pulse height resolution for 150,000 silicon strips. A readout IC [6,7], in Honeywell radiation-hard 0.8μm CMOS, integrates all functionality between the strip and 60Mbps serial readout links. It provides low-noise amplification and shaping, with programmable time constants to adjust shaping to detector capacitance and hit rates. It records pulse height using a time-over-threshold technique. It also provides level 1 buffering, sparsification, derandomizing buffer, and readout control logic.

3.2 Drift Chamber Electronics

The Drift Chamber Electronics must measure drift time and dE/dx for 7104 small drift cells. Drift time resolution of 2ns and pulse height measurement with dynamic range of 6 bits are required. In addition, prompt hit cell information must be provided for the level 1 trigger. The electronics is mounted on the chamber endplate opposite the center-of-mass boost. A 4-channel amplifier IC [8] in Maxim CPi semi-custom bipolar provides analog and discriminated outputs. An 8-channel digitizer IC [9, 10] in Hewlett Packard triple-metal 0.8μm CMOS provides a TDC with 1ns bins and a 15MHz, bilinear, 6-bit flash ADC for each channel. The digitizer IC also provides level 1 buffering, derandomizing buffer, and sparsification.

3.3 Particle ID Electronics

The Particle ID (DIRC) Electronics must measure single photoelectrons from Cerenkov light sensed by 10,752 photomultiplier tubes. Time precision of at least 1ns is required in order to reject background. Amplitude resolution of 6 bits is required for gain calibration. Photomultiplier signals are received by Front-end Boards in crates mounted inside magnetic shielding for the PMTs. Eight channel analog ICs [11] in AMS 1.2μm CMOS provide zero-crossing discriminators for timing and a multiplexed analog output for pulse height measurement on a sampling basis. Digital ICs [12] in Atmel-ES2 double-metal 0.8μm CMOS contain TDCs, programmable level 1 latency and readout window, latency and derandomizing buffers, and sparsification for 16 channels.

3.4 Calorimeter Electronics

The Calorimeter Electronics must measure pulse height with very low noise (~500e) and large dynamic range (18 bits) for 13,320 photodiodes on 6,660 CsI crystals. In addition, it must tag the time of event data and provide prompt energy sums to the level 1 trigger. Redundant low-noise, charge-sensitive amplifiers are mounted on the crystals. The amplifier is based on a single-channel amplifier IC in AMS 1.2μm BiCMOS with split-range output. The two outputs of each amplifier are fed to a 4-crystal calorimeter auto-ranging and encoding (CARE) IC [13] in AMS 1.2μm BiCMOS which provides large dynamic range via four amplitude scales multiplexed to a 10-bit flash ADC.

3.5 Instrumented Flux Return Electronics

The Instrumented Flux Return (IFR) Electronics [14] must record hit strips for 50,000 channels of resistive plate chambers (RPCs) and associate the hits with the level 1 trigger. RPC strips are read out via 16-channel Front-End Cards (FECs) which discriminate and delay the signals during the level 1 latency. FECs are read out in groups of 64 by FIFO Boards, which are located in crates mounted on the flux return iron. TDC Boards provide precise timing information on groups of RPC strips.

4. DATA ACQUISITION

4.1 Front-end Links and Protocols

All elements of *BABAR* front-end electronics are controlled via *BABAR*-standard protocols on *BABAR*-standard serial links. 60Mbps control streams are time-division multiplexed in groups of 16 by Readout Modules onto 1Gbps fiber control links which transport the control stream to transition cards on the detector. The transition cards derive the 60MHz system clock, demultiplex the 60Mbps control data, and distribute these signals to the front-end electronics, along point-to-point crate backplanes to the DIRC and IFR and via direct connections to the SVT, drift chamber, and calorimeter. This path transports both timing and slow control. The standard data path from detector-mounted electronics to Readout Modules is parallel to the control path. Groups of 16 serial data streams, up to 60Mbps, are multiplexed by the transition cards onto 1Gbps fiber data

links. Data streams are demultiplexed and buffered on the Readout Modules. The standard readout protocol allows for both fixed and variable length records. This path is used for both event data and read back of registers. The calorimeter uses a separate set of Gbps links for its large data volume.

4.2 Readout Module

A single Readout Module (ROM) design, with two Personality Card types, serves all detectors. It provides the standard interfaces, deep event buffers, and a processor (300MHz PowerPC). Its implementation consists of a commercial single-board VME computer (Motorola MVME2306) with PCI mezzanine slots plus two custom boards. Together these two boards provide a DMA interface between the standard *BABAR* data and control links and PCI, via a PCI/i960-bus bridge. The Controller Card provides a fast control and timing interface and manages front-end buffers. The Personality Card multiplexes and demultiplexes the control and data streams, provides the electro-optical interface, and provides intermediate storage of events. Two types of Personality Card were developed. The standard (triggered) Personality Card receives data from detector-mounted electronics in response to a level 1 trigger accept. It is used by all subsystems for control and by all but the calorimeter for event data. An untriggered Personality Card interfaces to the untriggered Gbps data streams of the calorimeter and provides a triggering mechanism such that calorimeter data is presented in the same way as other detector data to the CPU. The commercial CPU and the two custom boards assemble into a single-slot 9U*x*400mm VME card. The ROM runs a real-time operating system, VxWorks, and provides a well-supported coding environment.

4.3 Event Assembly

ROMs assemble event data from front-end elements into "segments" of the event. Preprocessing of event data, or "feature extraction", is also performed by the ROM. For instance, amplitude samples from the calorimeter are reduced to measurements of energy and time. Segments are read out from ROMs over VME by crate-level processors, the "Slot-1 ROMs", which are standard ROMs, either without links to front-end electronics or performing this data collection function as well as their other functions. Slot-1 ROMs assemble segments into larger event "fragments". From the crates, fragments are assembled into events in Level 3 processor memory over a commercial switching network. The initial implementation of this network uses switched 100Mbps Ethernet. Studies have established that this solution provides adequate bandwidth for *BABAR*'s modest (~65MBps) aggregate bandwidth. The *BABAR* data acquisition system consists of about 165 ROMs in 18 physical VME crates that are divided into 24 logical crates by segmented backplanes. The DAQ system is partitionable at the crate level such that any combination of subsystems or crates can run independently and autonomously with any combination of triggers.

4.4 Event Data Flow Control

Event synchronization is established by a Fast Control and Timing System (FCTS). This system consists of a DAQ master crate plus a Fast Control Distribution Module in each data acquisition crate. A system-wide clock of approximately 60MHz is derived from the PEP II RF system. A 5-bit event id and a 56-bit time (in units of 1/60MHz) are distributed with each level 1 accept signal and are checked at each stage of data collection and event assembly. Transmission to all crates and within all crates is isochronous. Distribution to Readout Modules in each crate is from distribution modules along a custom P3 backplane. The design of this backplane provides for standalone operation of a single crate in a laboratory without a master crate. Only the 5-bit event id is passed to the front-end electronics. The front-end electronics returns the event id and trigger time (typically 5 bits) with the data for each level 1 accept. FIFOs in each module in the fast control distribution chain record the history of all fast control transactions for diagnostic purposes. Fast control modules are read out with each event to corroborate synchronization. Detection of an error in synchronization will result in a request through the FCTS to resynchronize.

Collection of data from the front-end electronics to the Readout Module occurs upon the issuance of a *ReadEvent* command from each ROM via the Clink to its associated front-end electronics. Each front-end element responds by synchronously transmitting data for the next event in its derandomizing (output) buffer. This mechanism simplifies event synchronization and prevents overflow of front-end buffers. Bandwidth of front-end data links and depth of front-end buffers are sufficient to limit the deadtime introduced by this mechanism to a fraction of a percent.

The data acquisition issues a buffer *Full* signal to throttle the trigger whenever any buffer in the system cannot accept an additional event. Each Readout Module monitors the occupancy of its associated front-end buffers, and issues a *Full* signal through the FCTS if either the front-end buffers or its own buffers fill. When a downstream buffer fills, for instance in the level 3 farm, backpressure builds until the ROM buffers fill and *Full* is issued by a ROM.

5. SUMMARY

In order to address the requirements of its detector and operating environment, *BABAR* has designed an electronics, trigger, and data acquisition architecture that is quite similar to architectures being designed for the LHC. For instance, the *BABAR* architecture is multilevel,

pipelined, and nearly deadtime free. It employs detector-specific custom ICs to realize the full performance of detector systems. Front-end electronics is detector-mounted. It simultaneously digitizes analog signals, writes data to buffers, and is read out to the data acquisition system. Although analog front-ends and digital readout circuits are located in close proximity, full analog performance has been realized without digital noise. The trigger system has two levels, with the option for an additional intermediate level. The first level trigger is based on pipelined hardware processors and utilizes tracking and calorimeter data. The higher level trigger is based on an online event processing farm of commercial processors and is integrated with a network-based event builder into the data acquisition system. The online system also includes a prompt reconstruction phase that performs full "offline" processing of the data.

The *BABAR* design incorporates an unusual level of standardization across detector-specific subsystems. Front-end electronics is customized to detector-specific needs; however, front-end buffer architecture and front-end links and protocols, for both readout and control, are standard. All off-detector electronics is standardized. The *BABAR* Readout Module provides standard interfaces to timing, data acquisition, and detector controls systems. It also provides a standard platform and code framework for detector-specific preprocessing and calibration code. Data acquisition crates, fast control and timing modules, and much detector controls hardware are also standard across *BABAR* systems.

All electronics design, fabrication, and testing for *BABAR* is now almost complete, as is installation of the components on the detector. *BABAR* will be commissioned with a cosmic ray run during the Autumn of this year, and will be installed in the PEP II accelerator during Spring 1999.

6. ACKNOWLEDGEMENTS

BABAR Electronics is the product of a large group of talented scientists and engineers, from laboratories and universities in Canada (*Montreal*), France (*LAL Orsay, LPNHE Paris 6-7, X-PNHE Palaiseau*), Italy (*Frascati, Genova, Milano, Napoli, Padova, Pavia, Pisa, Torino*), the United Kingdom (*Bristol, Edinburgh, Imperial College, Royal Holloway, RAL*), and the United States (*UC Irvine, UC Santa Cruz, Caltech, Colorado, Colorado State, Iowa, Iowa State, LBNL, Maryland, Pennsylvania, Princeton, SLAC, Stanford*), who deserve credit for the outstanding work described here. The author's work is supported in part by U.S. Department of Energy Grant DE FG03 91ER40679.

7. REFERENCES

1. J. Richman, *et al.*, The *BABAR* Silicon Vertex Tracker, Nucl. Instr. and Meth. A 409 (1998) 219.
2. F. Ferroni, *et al.*, The *BABAR* Drift Chamber Project, Nucl. Instr. and Meth. A 409 (1998) 46.
3. L. Del Buono, Test DIRC: Beam Test Results and Performances, Nucl. Instr. and Meth. A 409 (1998) 382.
4. A. Stahl, *et al.*, The *BABAR* Electromagnetic Calorimeter, Nucl. Instr. and Meth. A 409 (1998) 615.
5. F. Anulli, *et al.*, The Muon and Neutral Hadron Detector for *BABAR*, Nucl. Instr. and Meth. A 409 (1998) 542.
6. V. Re, The Radhard Readout System of *BABAR* Silicon Vertex Tracker, Nucl. Instr. and Meth. A 409 (1998) 354.
7. I. Kipnis, *et al.*, A Time-over-Threshold Machine: the Readout Integrated Circuit for the *BABAR* Silicon Vertex Tracker, IEEE Trans. Nucl. Sci. 44 (1997) 289.
8. D. Coupal, *et al.*, The *BABAR* Drift Chamber Chip, presented at the 7th Pisa Meeting on Advanced Detectors, La Biodola, Isola d'Elba, Italy, May 25-31, 1997, submitted to *Nucl. Instr. and Meth.*
9. A. Chan, *et al.*, Design and Performance of the ELEFANT Digitizer IC for the *BABAR* Drift Chamber, to be presented at the IEEE Nuclear Science Symposium, Toronto, 1998, and published in IEEE Trans. Nucl. Sci.
10. A. Chan, *et al.*, A Multi-Channel Time-to-Digital Converter Chip for Drift Chamber Readout; IEEE Trans. Nucl. Sci. NS-43 (1996) 1720.
11. J. Ardelean, *et al.*, A Discriminator and Shaper Circuit Realized in CMOS Technology for *BABAR*, Nucl. Instr. and Meth. A 409 (1998) 322.
12. P. Bailly, *et al.*, A 500-ps resolution TDC chip for the DIRC at *BABAR*, Proceedings of the Seventh International Conference on Electronics for Future Colliders, Chestnut Ridge, NY, 1997.
13. G. Haller and D. Freytag, Analog Floating Point BiCMOS Sampling Chip and Architecture of the *BABAR* CsI Calorimeter Front-end Electronics System at the SLAC B-Factory, IEEE Trans. Nucl. Sci. NS-43 (1996) 1610.
14. N.Cavallo, *et al.*, Front-End Readout Development for the IFR Muon Detector at *BABAR*, Nucl. Instr. and Meth. A 409 (1998) 297.