A DEADTIMELESS SHIFT REGISTER STYLE READOUT SCHEME FOR MULTIWIRE PROPORTIONAL CHAMBERS*

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Abstract

A proportional chamber readout scheme has been developed which stores each wire's data in a 40 MHz "shift register" while a decision to retain an event is made. System delay, resolving time and storage time are adjustable parameters and multiple hits on a wire, within the storage time, are retained.

Introduction

The problem of storing proportional chamber information until a decision to retain it can be made is an old one.[1] If, furthermore, deadtime losses are undesirable, the classic solution has been to delay the signal with fast cable.[2] We have developed a system based on a fast random access memory (INTEL P3101) which replaces the fast cable with the equivalent of a 40 MHz "shift register" (loaded serially). When the decision to retain the data is made, the relevant locations within the memory are interrogated and the information passed on to a computer.

The advantages of this system are:

(1) The time necessary to reach a decision to retain the information is an adjustable parameter of the system as a whole. One is no longer concerned about choosing the "correct length of cable" prior to an experiment.

(2) The resolving time is a post hoc adjustable parameter of each wire of the system. We store data for an adjustable but rather large time window for each wire (200-400 nanoseconds typically). Since time information is retained within this window background counts are not a problem. A software cut can be made which selects the relevant time region within the window (50 nanoseconds wide typically) allowing us to achieve the smallest practical resolving time consistent with high efficiency.

(3) The time window for data storage can be as large as 800 nanoseconds, allowing us to detect and retain more than one piece of information per wire within this time. Our front end electronics, described elsewhere,[3] has shaped the input pulses from the chamber so that our pulse pair resolution for a single wire is 125 ± 25 nanoseconds. This feature of the system is especially useful at SLAC where all particles arrive in 1.5 microsecond bursts separated by many milliseconds.

(4) There are no deadtime losses in this system, insuring a uniform-rate independent system. Measurements have been made at 25 particles per pulse—the equivalent of 3×10^6 particles per second per wire—with no noticeable loss of data (neglecting space charge effects).

(5) The expense per wire is considerably below the equivalent fast cable system.

(6) The readout time is less than 10 milliseconds for a 12,000 wire system wherein we retain 300 nanoseconds of information. This time is compatible with the maximum repetition rate of conventional spark chambers.

Electronics

A logic diagram of this scheme is shown in Fig. 1. Data from each proportional chamber wire are shaped and presented to the inputs of two Random Access Memory banks referred to as the A and B memories (INTEL 3101 RAMs). These memories are wired so as to form in effect a 40 MHz shift register for each wire. The address lines for each memory are generated by alternate edges of the same 40 MHz system clock resulting in two sets of 20 MHz address lines separated in time by 25 nanoseconds (Fig. 2). Note that the multiplexers are set to select the A and B address counters at this time. During data taking the "WRITE" line is always on, and both memories are loaded by the data. The address lines continue to change until notification of an "EVENT" (signalled by auxiliary fast logic) stops the clock. Since it takes typically 400 nanoseconds from the passage of the particle through the system to the decision to retain the information, the data lie at some location other than that one at which the clock has stopped. The system controller must, therefore, back up the correct number of 25 nanosecond locations (TIME SLOTS) necessary to start the reading procedure at a time somewhat before the EVENT, and it must then read forward enough locations to completely record all the data (the TIME SLOT WINDOW). These two parameters are set once for the entire system.

A block diagram of the system is presented in Fig. 3. The system has been designed so that each crate of electronics handles 256 proportional chamber wires; sixteen cards per crate—each having 16 input channels.

The readout scheme is to go through a crate (all 256 wires) completely for a particular time slot (memory location), each card being interrogated as the 'SERIAL IN' signal is resident on it. When the last card is encountered we return to card zero of that crate, advance the time slot (by reading the B memory after having read the A memory or perhaps by going from B to A after advancing the memory address by one), and go through the entire crate again, as many times as necessary to cover the desired number of time slots. (The first time through the cards is called time slot '0' even though we may be reading out memory location '13', the second time through, time slot '1', etc.)

Each time a wire is hit within the TIME SLOT WINDOW, a 16 bit word containing the time slot and the wire position (card number and wire number) within the crate are transferred to the PDP-11 computer via DMA transfer. When we've been through the crate the requisite number of times, we transfer a "HEADER" word which contains the crate number and the number of words transferred for this crate.

The system controller then proceeds to analyze the next crate of electronics by issuing an 'ADVANCE CRATE' signal and repeating the above procedure. When all crates have been interrogated, the controller will issue a "DONE INTERRUPT", disconnect itself from the DMA and repeat the entire procedure (without transferring any data) facilitating the implementation of display hardware.

The readout has been designed to take less than 10 milliseconds for a full system scan even though we do it serially. This is accomplished by spending no more than one clock pulse (1 microsecond) on a card containing no data. If one of the 16 wires has data, then an average time of 8 microseconds will be spent on that card in forming the wire address for transmission to the PDP-11. A simplified logic

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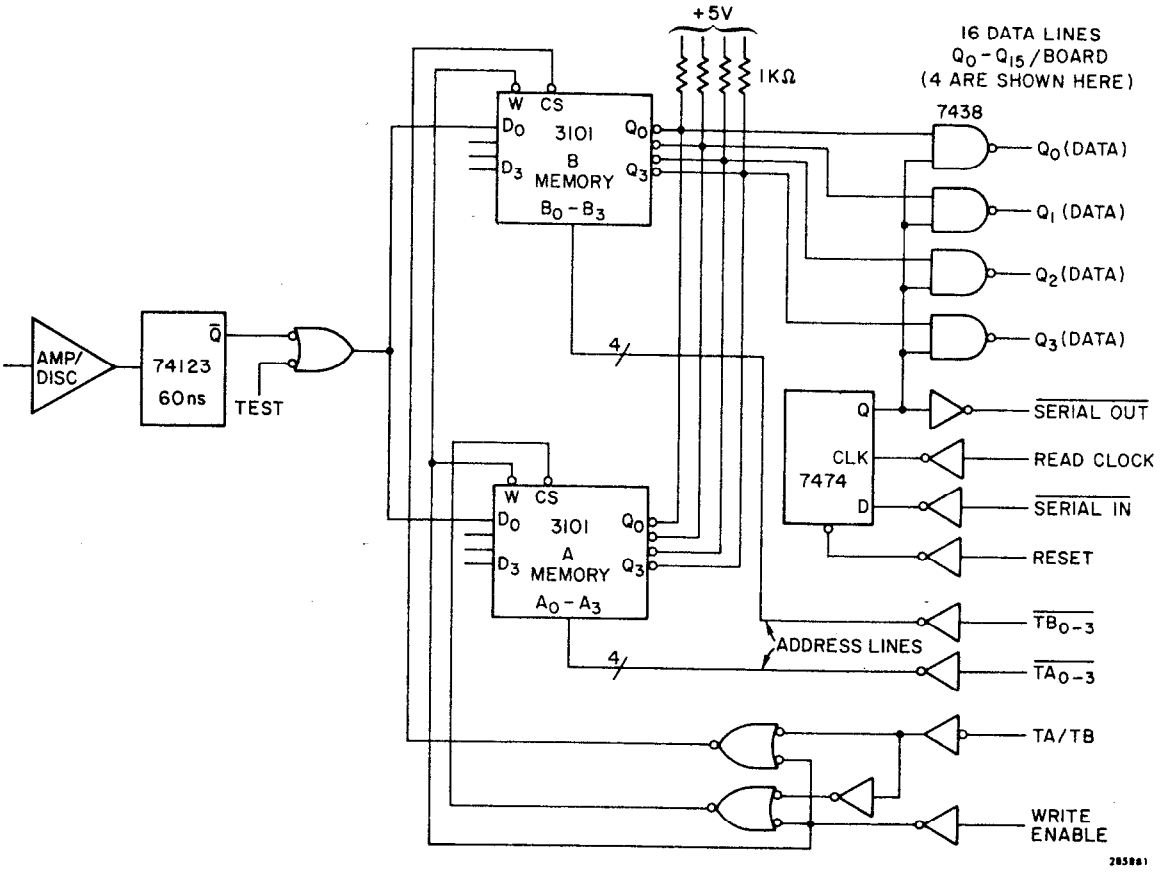


FIG. 1--Logic diagram of readout scheme showing those sections of the readout resident on the amplifier boards.

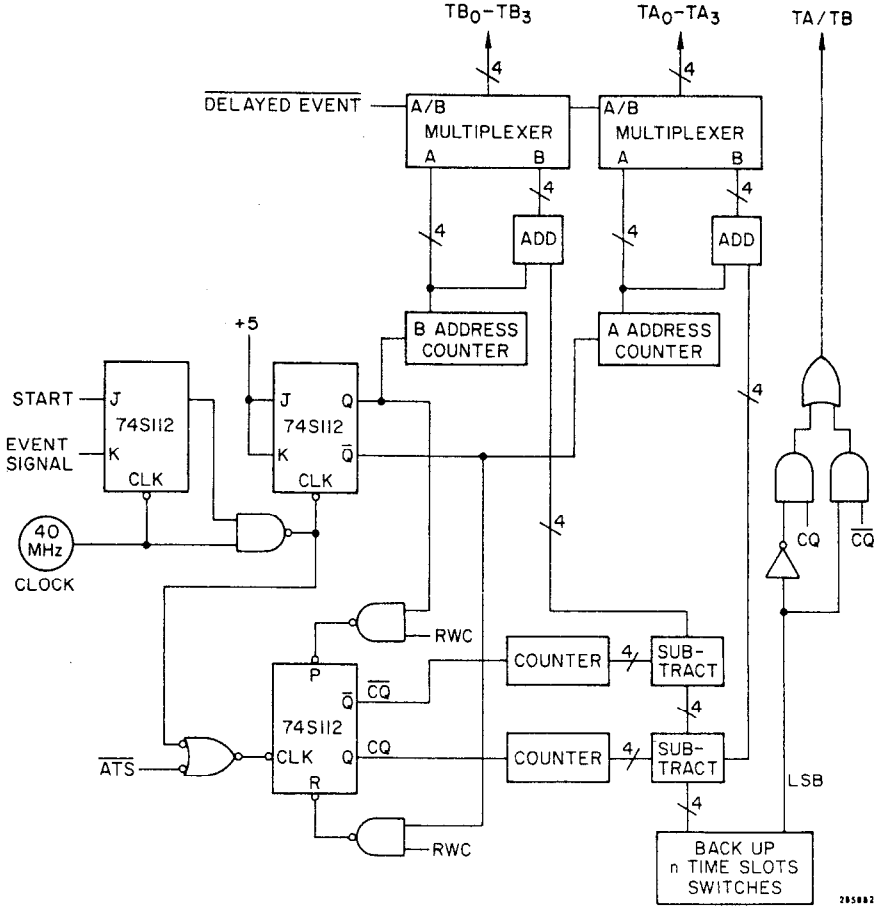


FIG. 2--Logic diagram of the readout electronics which control the recording of the data. Shown also are the circuits which control the setup of the address lines necessary for the readout to begin.

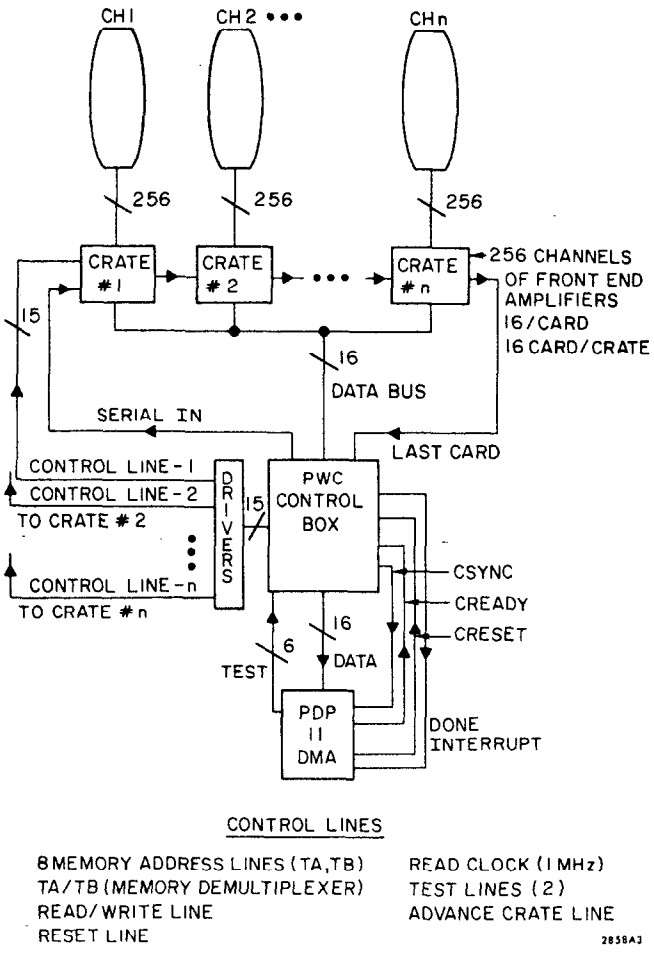


FIG. 3--System architecture for an arbitrary number of chambers showing the interconnections between chamber, control box and computer.

diagram is shown in Fig. 4. A modification of this scheme is presently being designed wherein all the crates are read out in parallel into a buffer memory, and the buffer memory is then transferred to the PDP-11. The advantage of this new scheme is its speed, 1-2 milliseconds, which allows us to further process the data between SLAC machine pulses if we so choose.

System Tests

Not explicitly shown in the above but of immense importance is our readout test structure. In a system of this size, it is crucial to be able to easily implement test procedures to insure the integrity of the system. These tests can be initiated either manually or under computer control. They use digital electronics already built into the system for this purpose. The tests used are three in number. The entire bank of 3101 memories (384,000 bits) are loaded with logical '1's (TEST 1) and '0's (TEST 2) and the results checked. The third test attempts to load a particular memory location with logical '1's. Passage of these tests insures an error free transmission of data from amplifier to computer.

Compatibility

One feature of this system which should not be overlooked is that of compatibility with conventional spark chambers. Often the proportional chamber is bolted directly onto a conventional chamber. When the decision to record an event is made, a signal to fire the conventional chambers is generated. If this signal is also used to convert the READ/WRITE line of the 3101 memories from WRITE to READ, and if this change occurs before the conventional chamber actually sparks, then the proportional wire chamber readout system will be immune to spark chamber induced noise. This effect has been carefully studied statistically and on an event by event basis and no evidence for pickup has been found.

Data

The data presented in Figs. 5 and 6 are representative of information currently being recorded at SLAC by a proportional beam chamber having 1 mm anode wire spacing and 4 mm half gap. Figure 5a shows the number of time slots "hit" per wire for a large sample of incident particles. The multiplexing scheme results in at least two time slot hits per wire; however, if the memories actually have a swifter access time than advertised, three time slots will be loaded. We shape the input pulses to the memories so that they are 60 nanosecond long TTL pulses. Figure 5a is explained if the memories have a data wire overlap time (t_{DW}) of 25 ± 1 nanoseconds (t_{DW} typical for these devices is advertised to be 40 nanoseconds). Using this information we generate the conversion function shown in Fig. 5b and use it to rebin the data against real time rather than time slots. The resulting distribution is shown in Fig. 5c. The observed time resolution is then seen to be 37 nanoseconds full width at half maximum. These data are consistent with our understanding of the source of this time resolution, viz.: (1) least count of the readout system (± 12.5 nanoseconds), (2) drift time of the particles between wires ($\sim \pm 7$ nanoseconds) and (3) electronic time jitter (± 6 nanoseconds).[3]

Finally, Fig. 6 demonstrates that the readout reliably records the passage of a second particle whose time of arrival has been selected to be 50 - 100 nanoseconds after the arrival of the first particle, which triggered the system. We used scintillation counters and TDC's to record the time of arrival of particles traversing our chamber. As we progress towards experiments wherein it is necessary to record two events within one SLAC pulse, the capability of being able to make a one to one correspondence between scintillation counters and proportional chambers becomes more and more important. The proportional chambers are then able to tag tracks recorded in the spark chambers thereby separating the two events.

Conclusion

This system has proved to be reliable, flexible, and easy to set up. The compromise which one makes in using a synchronous readout system is seen to be small in that the overall system time resolution is comparable to that recorded by other techniques under experimental conditions[4] but is a factor of 2 worse than that obtainable in the laboratory.[1]

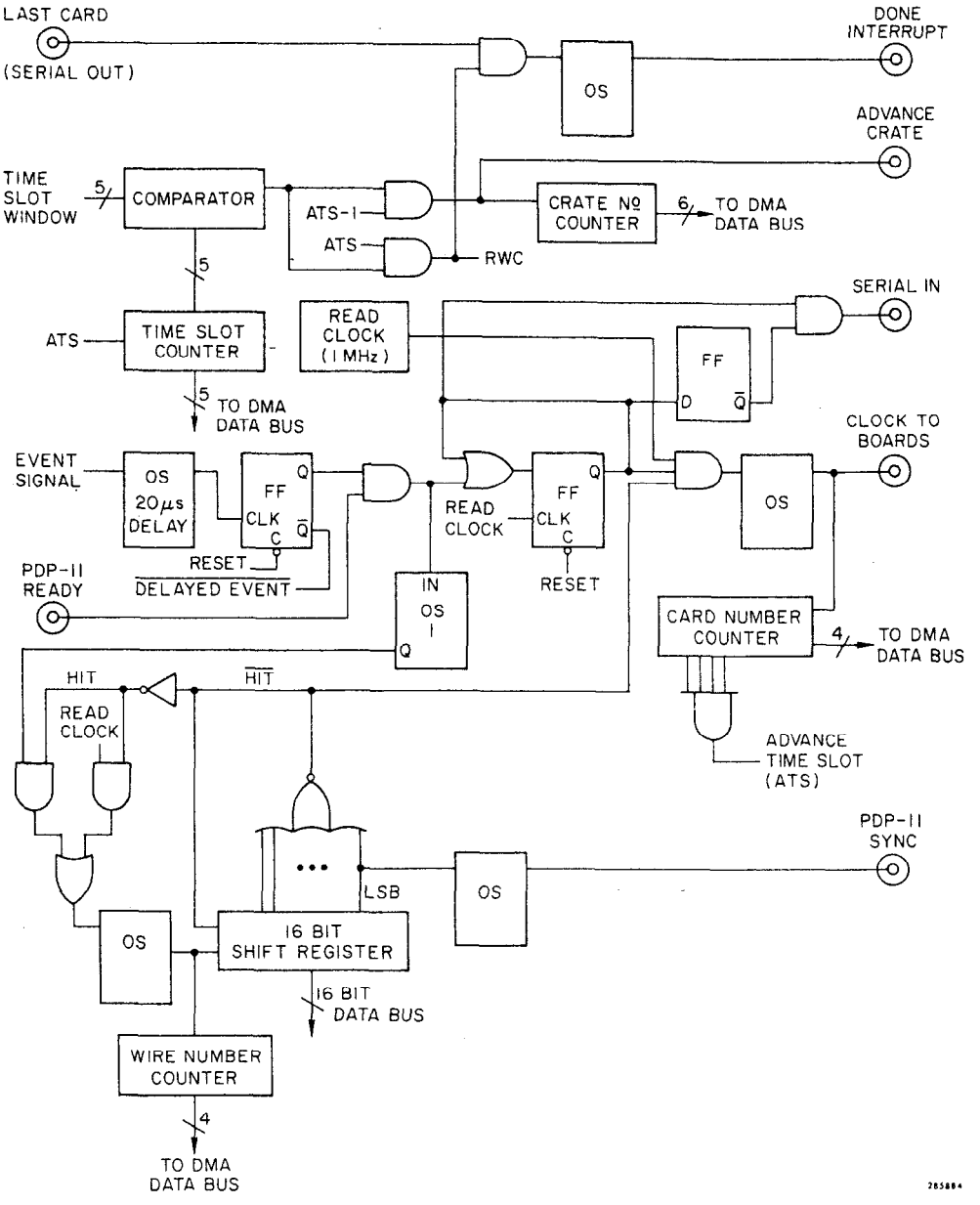
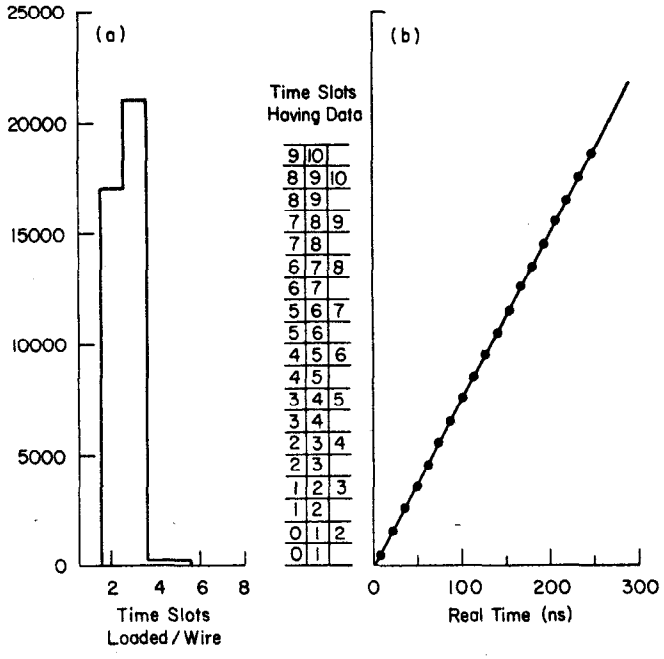


FIG. 4--Simplified logic diagram of the readout electronics which control the data transfer from the amplifier boards to the computer.



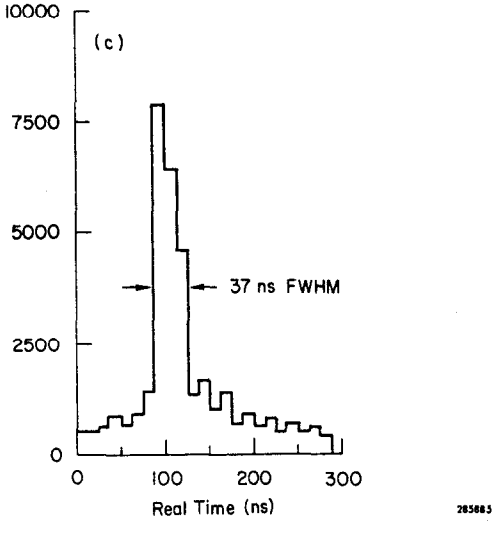


FIG. 5--(a) A typical time slot distribution. (b) The conversion function for an assumed t_{DW} of 25 nanoseconds and an input pulse width to the 3101's of 60 nanoseconds. (c) A real time distribution of the data wherein we have applied the conversion factor of 5b to set the scale.

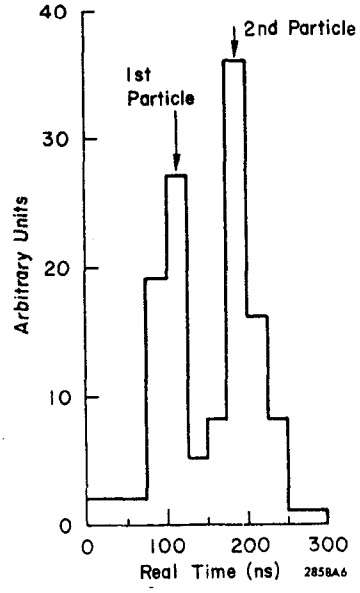


FIG. 6--A real time distribution of data in a 1 mm beam chamber for selected events having a second particle in the chamber 50-100 nanoseconds after the triggering particle.

Acknowledgements

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