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Clock distribution system for large high altitude air shower observatory

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Abstract In this paper, we report a clock distribution system for Water Cherenkov Detector Arrays (WCDAs) in Large High Altitude Air Shower Observatory (LHAASO) project. The designed electronics system is of high performance in implementing the clock distribution among detectors of a large scale of dimension. Based on Serializer/Deserializer (SerDes) and fiber transmission, the clock distribution system is the modules of central back end to distributed front end. The clock distribution system has been evaluated with a two modules system. While all the four SerDes candidates for clock transmission with jitters below 17 ps, the DS92LV16 has a fixed phase relationship between transmission clock and recovered clock, hence its use in LHAASO WCDAs.

Key words LHAASO, Clock distribution, Distributed architecture, Serializer/Deserializer

1 Introduction

The Large High Altitude Air Shower Observatory (LHAASO) project for cosmic ray physics is a large Extensive Air Shower (EAS) particle detector array of 1 km ×1 km, located 4300 m above sea level at Yangbajing, Tibet[1]. The Water Cherenkov Detector Arrays (WCDAs) with an active area of 90000 m^2 are components of the LHAASO to achieve the goal, and locate in four water pools containing 3600 photo multiplier tubes (PMTs) in total. The PMTs are positioned in water of 4-m depth with 5-m intervals, to capture the low energy EAS generated by cosmic rays[2]. The PMTs and associate readout electronics record arrival time and energy of the Cherenkov light caused by EAS, thus ascertaining direction and energy of the primary gamma rays[3]. The required time resolution is 1 ns.

Traditionally, a detector is linked, via a long cable of analog transmission, to a counting room, where the signals are digitalized. This architecture implementing digitalization far from the detector is called the lumped electronics. However, using lumped architecture on LHAASO WCDAs, with cables of about 150-m length, the signal amplitudes would be attenuated, the pulse leading edges be slowed, and the measurement precision be reduced, due to the cable length and bandwidth limitation, even they are of high bandwidth cables.

A distributed architecture, where digitalization is implemented in the front end near every detector, is deemed to be free from disadvantage of the lumped architecture. The key to distributed architectures is to provide an accurate and stable phase relationship of the synchronization clock for all the front-end electronics. But this is not an easy task. The clock jitters increasingly in the distant transmission, and the clock phase shifts with the temperature. Nevertheless, as a distributed architecture with a large scale of dimension can manage the data transmission between modules of distributed front end and central back end in the counting room, indirect methods of clock distribution are preferred, so that every front end module is linked to the counting room via just one pair of channels. Several indirect schemes are available,

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such as synchronous clock distribution, asynchronous clock calibration, and White Rabbit (WR) Project.

In a synchronous clock distribution scheme, the clock and data are combined with serial bit stream in the back end module, and the stream is sent to the front end module, where the clock and data are decoded. The recovered clock, which has the same frequency as the transmission clock, is performed as the system clock of the front end module[4]. The Synchronization of Data Acquisition (SODA) system employs a point-to-multipoint optical network with the interface of bidirectional link, and the 8b/10b SerDeses (Serializers/Deserializers) are used to synchronize the recovered clock phase in receiver modules. The SODA system developed in PANDA experiment was able to provide a common reference time with a precision of better than 20-ps (RMS)[5]. The fixed phase relationship was obtained by a set of dual SerDes, one of which had a fixed recovered clock, while the other was repetitively reset. The system measured the time relation of two recovered clocks, and finds all the 10 phases of the recovered clock. The second SerDes was reset again until it meets the earliest position of clock phases[5]. This reset-measurement procedure, however, needs the more SerDes and takes more time.

An asynchronous clock distribution scheme does not have a distributed common clock because every module has its own clock. The counting room sends the calibration signal to the front end module and receives the returned signal, thus measuring the clock frequency and phase in the front end module. In IceCube experiment, the phase and frequency of each free-running local oscillator in the front end module, which are relative to the master clock, were determined by transmitting a fast bipolar pulse between modules of the back end and the front end. After receiving the pulse from the back end module, the front end module sent back a pulse after a delay interval[6]. The calibration pulses were transmitted in the data channel, and no data were transmitted when a calibration was in progress. The time calibration waveforms were digitized and timed in the back end module, so as to calculate the phase and frequency of each local oscillator. And the 2.5-km cable could slow the rise time[7]. This calibration procedure should be carried out frequently because of the instability of the local oscillator. LHAASO WCDAs has a larger data rate than IceCube, so this scheme, which may decrease the data rate, is not suitable for WCDAs.

The WR Project is developed by CERN using Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE)[8]. Based on SyncE, it sends the clock signal from the WR master module to the WR switch modules, and implements phase measurements and line delay estimation based on PTPv2. It provides deterministic data and timing to around 1000 stations, and automatically compensates for fiber lengths and temperature drift in the order of 10 km[9]. Some principles of the complex project, such as compensation for temperature drift, can be used in LHAASO WCDAs clock distribution system.

In this paper, a high precise clock distribution method among detectors of a large scale of dimension for the distributed architecture is designed for LHAASO WCDAs. The clock distribution system, which is based on SerDes and fiber transmission, is used to distribute the common clock from central back end module to the front end module. An evaluation system is developed to assess the clock distribution method. It shows that all the four candidates for clock transmission have the distributed clock with jitter of less than 17 ps, and the SerDes of DS92LV16 has a fixed phase relationship between transmission and recovered clocks, with a good performance for LHAASO WCDAs.

2 The clock distribution and design evaluation

2.1 The clock design

A high performance clock distribution system for LHAASO WCDAs is shown in Fig.1.

The common clock is generated by a special clock module in the counting room, and distributed to the back end module, via short cables, and to the large quantity of front end modules. Each back end module distributes the common clock, via fiber, to all the front end modules under its control. Compared to common cables, fiber is advantageous in that it reduces channel numbers and signal attenuation as well. The clock is embedded into the data stream in the back end module

and sent to the front end module. The clock and data are recovered in the front end module near the detector. SerDeses are used in front and back end modules to encode and decode the clock and data, respectively.

The time measurement units in the front end module are in good correlation with each other, so the recovered clocks in the front end module have a fixed phase difference even at switching the system on, and the recovered clock of the SerDes have a fixed phase relationship with the transmission clock in the back end module. If the recovered clock has different phases related to the transmission clock, the phase difference is calculated.

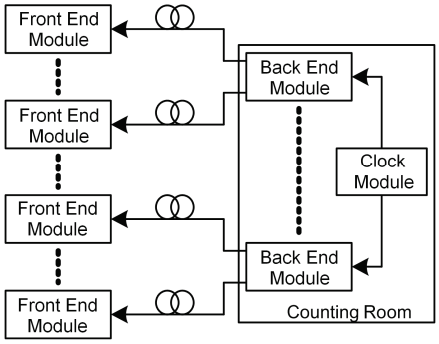

Fig.1 Clock distribution system for LHAASO WCDAs.

2.2 Evaluation of electronics system design

To test and assess precision of the clock distribution system, an evaluation electronics system of the MP (Master Prototype, of the back end) and SP (Slave Prototype, of the front end) modules was developed, based on SerDes and fiber transmission. Fig.2 shows the operation of the clock distribution. According to design of the distributed architecture, the clock for the SP sources from the MP. The common clock and parallel data are serialized to a high speed bit stream and then converted to laser signals by the optical tranceiver in the MP. The SP receives the stream via a long distance fiber, and de-serializes it to the parallel data. The clock is recovered during the de-serialization. In order to improve the precision of the recovered clock, a Phase Locked Loop (PLL) is applied to clean the jitter.

Two kinds of SerDeses are available for the clock distribution system: embedded clock bits SerDes and 8b/10b SerDes. In the embedded clock bits SerDes, two fixed bits are embedded into the bit stream of each cycle, as the start and stop bit of each serialized data stream. The start bit is high and the stop bit is low. The stop bit of the current cycle and the start bit of the next cycle create a periodic rising edge in the serial stream. The rising edge acts as the leading edge of the recovered clock, which has the same frequency and fixed phase relationship as the transmission clock. In the 8b/10b SerDes, each parallel data byte is mapped to a 10 bit code and serializes the 10 bit code into a serial pair. The 10 bit transmission codes guarantee multiple edge transitions in each cycle, and the direct current balance, which helps driving alternating current coupled loads, long cables and optical modules[10]. The deserializer recovers the clock from the bit stream with the help of an external reference clock. The clock can be recovered from any serial bit of the 10 bit cycle, so as to have 10 phases in the recovered clock after reset[11].

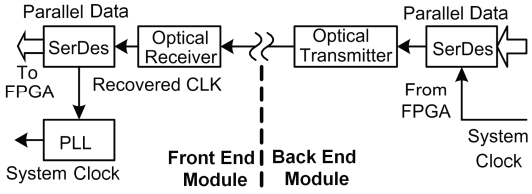

Fig.2 The clock distribution system.

As shown in Table 1, four SerDeses were chosen and organized in four groups for testing data and clock transmission, including the recovered clock jitter, and the phase relationship between the transmission and recovered clock. Groups 1, 2 and 3 were of embedded clock bits SerDeses, and Group 4 was 8b/10b SerDes.

Table 1 SerDeses for testing the data and clock transmission.

Groups	Serializer	Deserializer
1	SN65LV1023A	SN65LV1224B
2	DS92LV16	DS92LV16
3	TLK1521	TLK1521
4	TLK1501	TLK1501

Figure 3 shows the clock distribution components in the MP. An Evacuated Miniature Oven Controlled Crystal Oscillator (EMXO) EX-380 was used to obtain a stable source of clock. It is a good choice to have this small size device of desirable spectral purity, with long term stability and little power consumption[12]. The common clock source

from EX-380 and fanned out to the serialization device. The four SerDes groups and transceivers were used to assess the clock and data transmission. The module is controlled by the Field-Programmable Gate Array (FPGA).

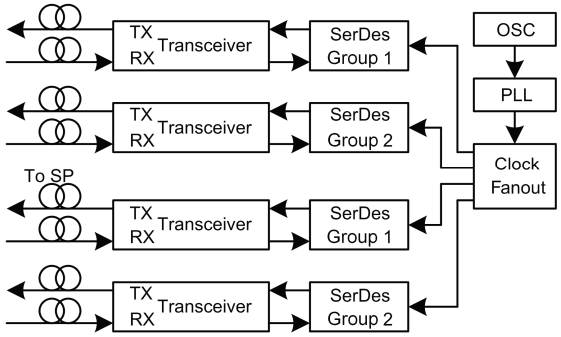

Fig.3 The clock distribution components in the MP.

Schematic of the SP is shown in Fig.4. The clock and data are decoded by SerDeses and performed as the recovered system clock after the PLL. A local oscillator is used in the complexion that the recovered clock does not work. Also, the de-serialization devices are used.

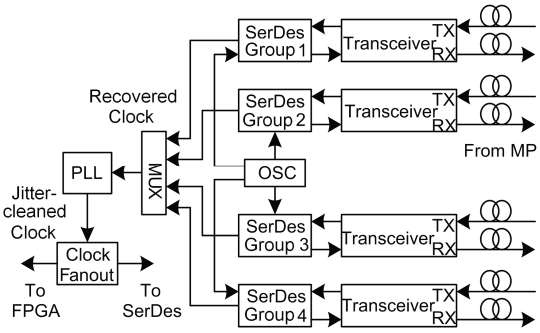

Fig.4 The clock distribution components in the SP.

3 Results and Discussion

The four SerDes candidates were evaluated. The recovered clock jitter and phase relationship between the recovered and transmission clocks are given in Table 2. Every group has a good performance. The jitter of the system clock is below 17 ps in the SP.

Table 2 Clock distribution tests for different SerDeses.

Groups	SerDes	Tt Jitter / ps	Tr Jitter / ps	Tp Jitter / ps
1	SN65LV1023A, SN65LV1224B	25.964	47.900	16.461
2	DS92LV16	25.920	31.391	15.344
3	TLK1521	26.074	21.810	16.885
4	TLK1501	26.312	28.164	16.805

The four SerDes groups were tested for the clock distribution. As shown in Fig.5, the LeCroy WavePro 715Zi oscilloscope, with 1.5 GHz bandwidth and 20 G samples per second, was used to measure the transmission clock (T_t) from EX-380 in the MP, the recovered clock (T_r) from the SerDes and the jitter cleaned clock (T_p) from the PLL in the SP. Phase differences between T_t and T_r after repeated resets were tested. The FPGA reset the SerDeses time to time and the phase relationships between T_t and T_r were measured. Fig.6 shows two random phases of T_r in Groups 1 and 3, ten random phases of T_r in Group 4, but a fixed relationship between T_t and T_r for Group 2. With DS92LV16, the recovered clock is of jitters below 16 ps, having a fixed phase relationship with the transmission clock, hence its use in the clock distribution system.

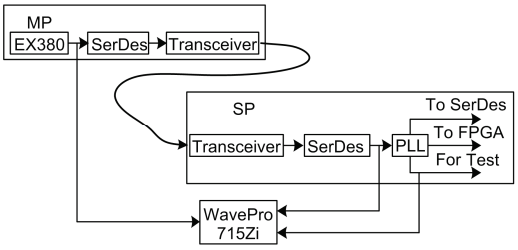

Fig.5 Diagram of system test on clock distribution.

4 Conclusions

A clock distribution system of the distributed architecture for LHAASO WCDAs was designed. An evaluation system of two modules was developed to test the performance of the clock distribution system. The jitter of the recovered clock is below 17 ps RMS, and DS92LV16 has a fixed phase between transmission clock and recovered clock, thus reaching a good performance in LHAASO WCDAs.

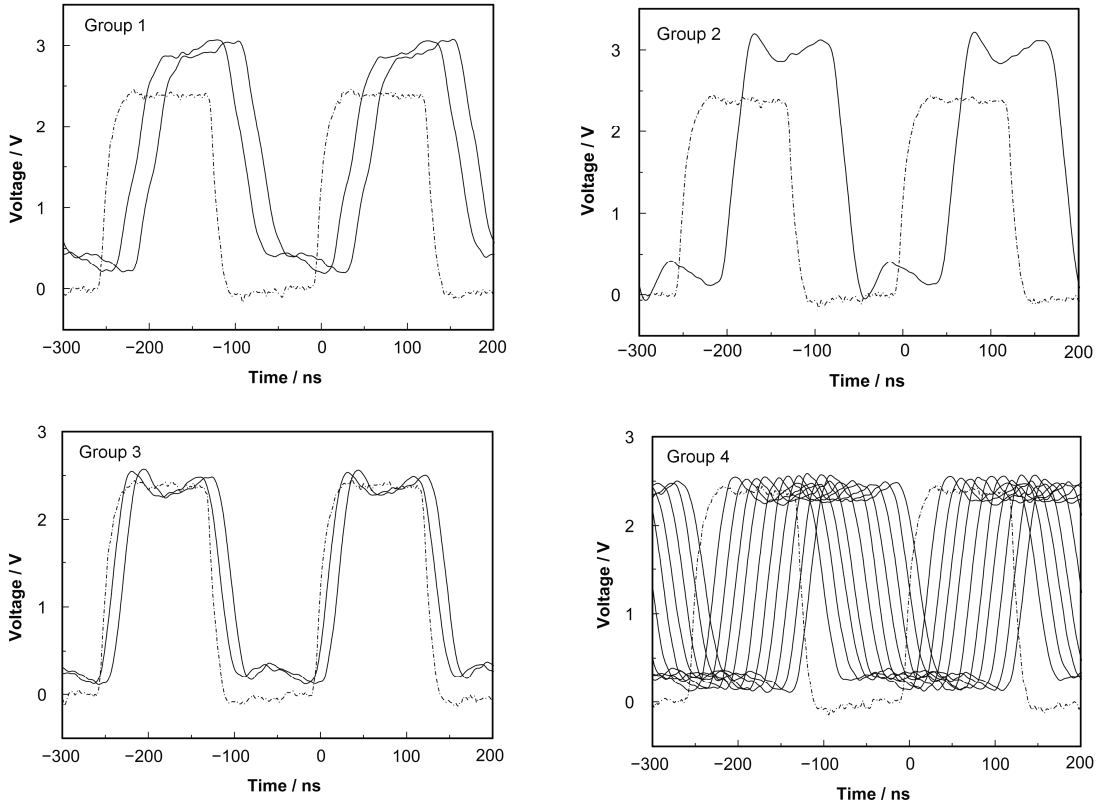

Fig.6 Different phases of recovered clock (solid lines) in Groups 1, 2, 3 and 4. The dotted lines are of the transmission clock.

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