A Microvertex Detector for B-Physics at the SSC

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1 Introduction

1.1 B-Physics at the SSC

The physics of bottom quark decays provides stringent tests of the standard model through the rich structure of CP-violating decays that are expected. CP-violation would show up as an asymmetry in the decay rates of a B-particle and its anti-particle,

$$A = \frac{\Gamma(B \to f) - \Gamma(\overline{B} \to \overline{f})}{\Gamma(B \to f) + \Gamma(\overline{B} \to \overline{f})},$$

where f is the final state. Asymmetries have been predicted[1][2] for a number of decay modes within the framework of the standard model by using the available measurements of the CKM mixing angles, the mixing parameter x_d=.73, and plausible values for those standard model parameters not yet well measured.

For the benchmark case of $B_d \to \pi^+\pi^-$, A is estimated to lie in the range .05 to .3 and the branching fraction for this mode is estimated to be 5×10^{-5}. To measure such an asymmetry at the 5σ level would require between $6 \times 10^6/\epsilon$ and $2 \times 10^8/\epsilon$ produced $b\bar{b}$ events, where ϵ is the efficiency for reconstructing the B decay and tagging it as B or $\bar{B}$. For an overall acceptance of 1% including tagging the accompanying b, about 10^{10} produced b's are required. At the SSC, for a luminosity of 2×10^{32} $cm^{-2}sec^{-1}$, 10^{12} $b\bar{b}$ pairs per year will be produced, a rate which easily meets the requirement. The fraction of the interactions that will produce $b\bar{b}$ pairs is 0.5%.

B_s decays may be even more favorable than B_d decays for CP-violation measurements because the large value (~15) expected for the mixing parameter x_s gives rise to measurably different time development of the B versus $\overline{B}$ decays.

To measure these decays will require a new type of colliding beam detector[3,4] with a large acceptance for small p_t particles and with excellent tracking, vertexing, and particle identification in this range. A crucial element of the experiment is a micro-vertex system capable of distinguishing the long-lived charm and bottom decays from prompt particle production and measuring the time development of the decay asymmetry.

Important physics other than B-decays will be accessible to an experiment equipped with micro-vertex detection capability. Higgs particles decaying into $b\bar{b}$ quark pairs will have a clean signature through the reconstruction of nearly back-to-back, high p_t b-particles. Another physics area will be opened up by the unprecedented number of charmed particles ($> 10^8$) that can be reconstructed with a B-physics detector. The dependence of the charm cross section on x_f will reveal the gluon structure function at small momentum fraction - an unexplored regime of QCD. In addition

studies of rare D decays and a sensistive search for non-standard CP-violation in D-decays will be possible.

1.2 Vertex Detector Requirements

The micro-vertex detector must meet a number of challenging design requirements. Foremost is the need for space point measurement with an r.m.s. resolution of about 5 μm in each coordinate (x and y) of the measurement plane. The amount of material in the planes must be such that this resolution is not significantly degraded by multiple scattering error when tracks of typical transverse momentum 1 Gev/c are projected to their vertex of origin. These fundamental requirements can be met by a hodoscope system of silicon strip and pixel detectors built on substrates with thickness in the range 200 to 300 μm.

The silicon wafers will be arranged in a mosaic structure surrounding the beam pipe. A preliminary geometrical design of this system is shown in figures 1 and 2. The inner layers will consist of pixel detectors, while the outer layers will have strip detectors.

Radiation doses will be at least 1 Mrad per year just outside the beam pipe. Both the detection diodes and readout electronics must tolerate this. For radiation doses greater than about 1 Mrad, pixel detectors are required which have a smaller detection diode area (typically 100 μm $\times$ 100 μm) than strip detectors (typically 50 μm $\times$ 5 cm). In addition, the relatively higher track density at smaller radius requires the pattern recognition capability of a pixel device.

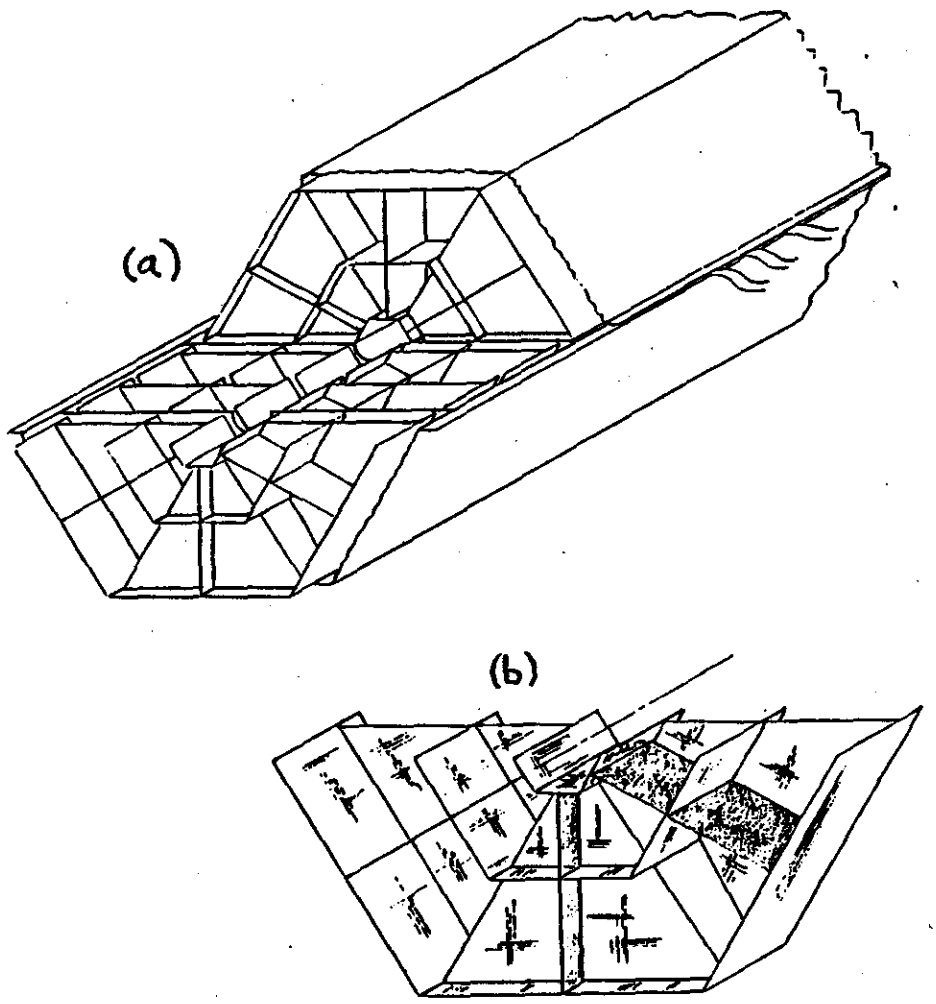
The interaction rate will be in the range of 10 to 100 MHz for accelerator luminosity in the range 10^{32} to 10^{33} $cm^{-2}sec^{-1}$. The vertex system must be able to buffer hit information at this rate and store it for a few μsec until a trigger decision is made.

Because of the compact nature of the vertex detector, the heat dissipation must be limited to a few watts per cm^2. The mechanical structure must accommodate this heat load while still maintaining the alignment at the few micron level and minimizing the amount of structural material. Electromagnetic shielding of the detectors, electronics, and cables must be adequate to maintain overall noise levels of less than 600 electrons.

To address the above problems we propose a program emphasizing the development of three key items:

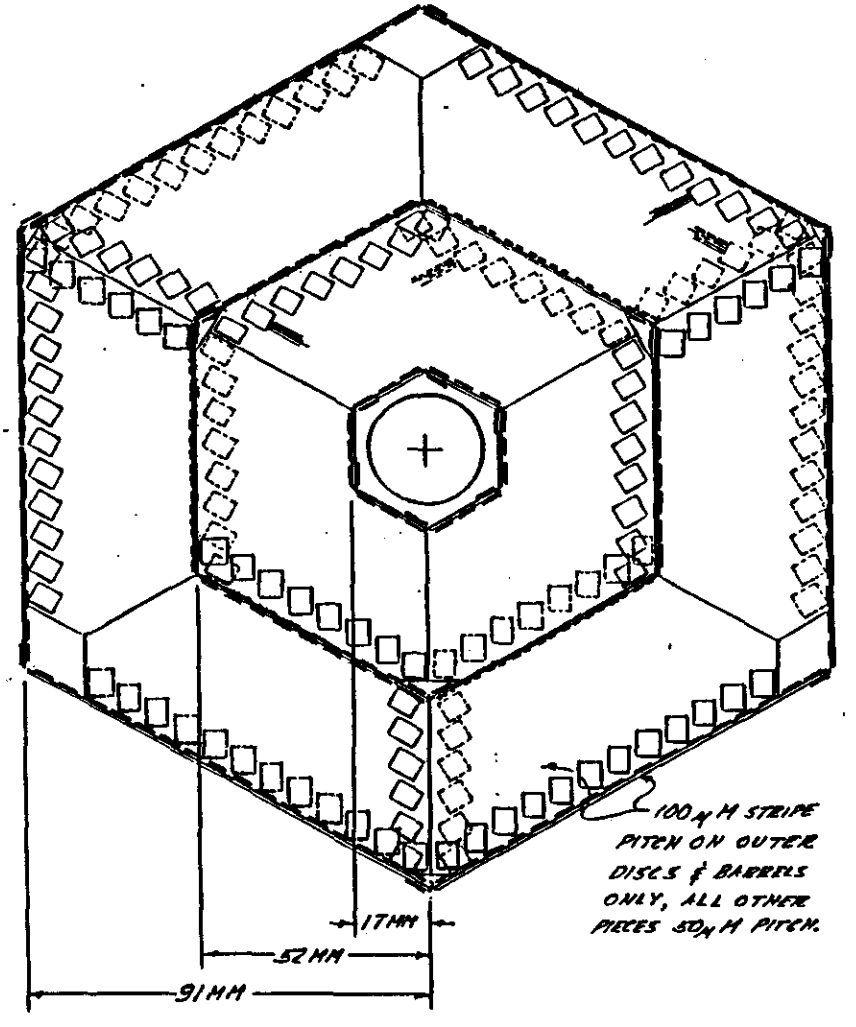
- a high rate, high resolution pixel device,
- a high rate, high resolution silicon strip readout chip, and
- a prototype system utilizing existing silicon strip technology.

Figure 1:



(a) Arrangement of silicon wafers for micro-vertex detection of B-decays at the SSC. In this preliminary design, wafers are oriented both perpendicular and parallel to the beam. The outer barrel radius is about 10 cm. (b) Detail of a single module. Drawings courtesy Carl Lindenmeyer, Fermilab.

Figure 2:



Detail of a microstrip wafer assembly oriented perpendicular to the beam. Readout chips are located on both sides of the wafers. Drawing courtesy Carl Lindenmeyer, Fermilab.

These projects are discussed in detail below.

2 Silicon Strip Readout Electronics - Oak Ridge National Lab

2.1 Overview

The BVX/S Chip is an ASIC (application specific integrated circuit) for readout of a silicon strip vertex detector at the SSC.

The main difference between the Fermilab BVX and the SSC version, dubbed the BVX/S is that BVX/S must operate faster than the BVX (50 ns vs. 400 ns) and that the BVXS must tolerate more radiation (> 1Mrad vs. > 0.1 Mrad).

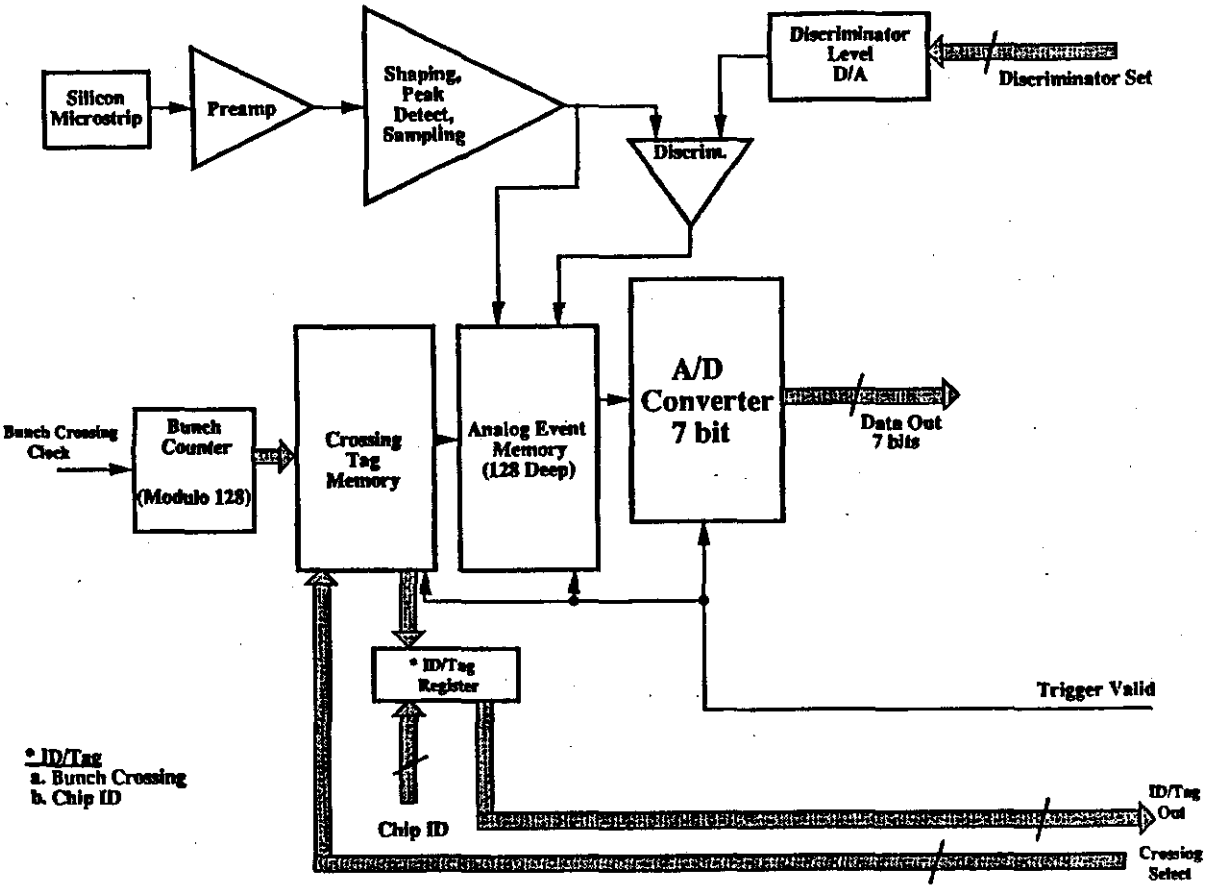
The overall specifications of the BVX/S chip are:

- amplifier pulse dwell time of 50 ns
- power consumption goal of 3 mW/channel
- noise $\leq$ 600 electrons, rms
- trigger delay of 2 μsec with 16 ns steps (4 μsec with 32 ns steps)
- 7 bit ADC readout with sparsification
- suppression of strip clusters with n > 5
- 50 micron pitch of input pads
- radiation damage tolerance to at least 1 Mrad (goal: 5 Mrad)
- 128 channels per chip

2.2 Scope

Since prior work has already been done in this area, our approach is to build as much as possible on this work. The SVX chip is probably the most highly developed readout chip presently available, therefore, we plan to investigate enhancing its functionality by incorporating additional key innovations such as analog storage in each channel and perhaps on-chip A/D conversion. The proposed chip, illustrated in Figure 3, will be designed in such a way to facilitate bonding directly to microstrip detectors with a contact pitch of 50 microns.

Figure 3:



Channel Architecture.

Although the goal is to implement 128 readout channels on one chip, it seems unlikely that this many channels of enhanced functionality electronics can be put onto one substrate. At this time we plan to make the analog storage 128 deep. We plan to investigate different filter topologies to be used on the analog front end to improve the signal to noise ratio over what has been done previously. The present goal for power dissipation is to require no more than 3mW per channel. We set this as a goal only since there are some sincere doubts as to whether this can be met with the massive amount of desired analog memory. Most of the readout chips up to this point have been fabricated using processes that are not inherently radiation hardened. Although the ultimate goal of this work is to develop a radiation hardened CMOS readout chip, the concept of the chip will be proven first using a non radiation hardened CMOS process. The CMOS processes offered through the MOSIS service will be used for the non radiation hardened prototyping. Because of density and speed advantages, either the 1.2 micron or the 1.6 micron process will be used. The primary reason for proceeding this way is because of the fabrication cost associated with a radiation hardened process. After the concept has been proven, it will be mapped into a radiation hardened CMOS process during the third year. Efforts are already underway to identify an appropriate process. Outlined below is a more detailed account of the work to be performed in each of the three years.

2.3 PHASE I (YEAR1)

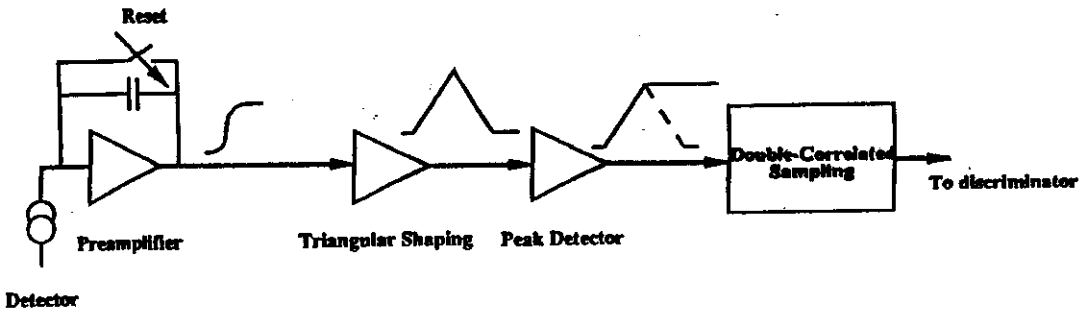
2.3.1 Charge Sensitive Preamplifier

Investigations will be performed to determine the best choice for a front end topology. It is felt at this time that a full MOSFET front end will be sufficient. At least one other possibility is that a bipolar or BiCMOS preamplifier may be necessary not for noise, but for bandwidth since there have been some concerns voiced about the run-to-run performance consistency of the commercially available CMOS processes. We intend to build upon, as much as possible, prior work performed on charge sensitive preamplifier development. A desired noise performance target is 600 electrons rms at approximately 50 nanoseconds pulse dwell time. One goal of this chip is to be able to interface to both polarities of input signals thereby using both sides of the microstrip detector. We will need some ability to be able to not only drive both polarities, but also to input the correct polarity into the subsequent shaping and storage stages. One approach that will be investigated is to pin program the polarity to which specific chips will be subjected.

2.3.2 Baseline Restoration-Shaping-Discrimination

The primary usefulness of double correlated sampling is that the technique removes very low frequency variations in the signal being processed and removes noise at integer multiples of the sampling frequency. Examination of the noise spectral

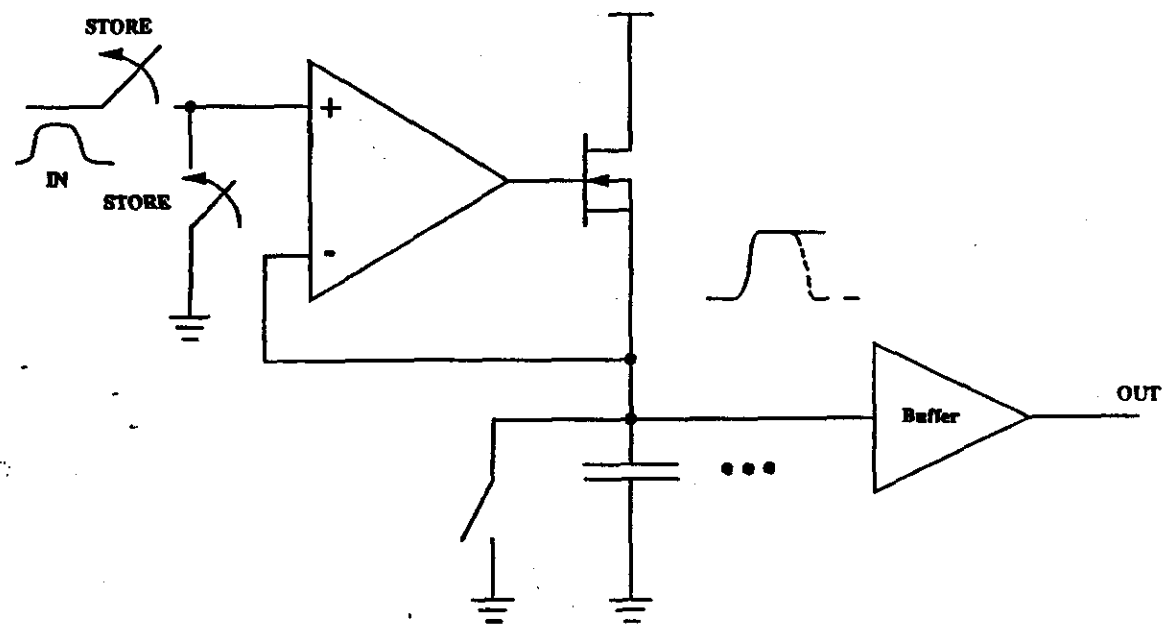
Figure 4:



Vertex detector front-end and signal processing electronics.

weighting function W(ft) = 1-cos(2pft) reveals that as an undamped periodic function in the frequency domain, there is no bandwidth limitation for white noise. Some 'integration' can be performed by multiple sampling, but the most effective method of actual signal-to-noise improvement appears to be pre-filtering before the sampler. In vertex detectors, the short shaping-time constants dictated by the high system clock rate force signal processing operation well into the frequencies where series noise (front end and second stage preamplifier noise) is dominant. Because, to a first order, we are dealing with only one noise spectral density (assuming 1/f noise is negligible in a good analog process at high frequencies), some modification of the weighting function exhibited by a simple integration is in order. In particular, a weighting function whose time derivative is minimized is most appropriate since this will minimize the series noise contribution. It has been known that, for time-invariant filters, a symmetrical triangle is the optimum step response for a filter that will be used for processing signals in the presence of primarily series noise. This assumes also that the charge-collection time for a given detector and preamplifier risetime is much shorter than the signal processing time. We will investigate the design and fabrication of a triangular filter that will act as a prefilter for a double correlated sampler. Specifically, the development will focus on a single active delay line-integrate triangle generator to be followed by a peak-detecting track-and-hold. The track-and- hold output will be the input to the correlated sampler as shown in Figure 4. Amplitude discrimination will be needed for determining the channels that have interesting information. This discriminator will be set by an on-chip D/A converter that will be accessible to the data bus during calibration. A 'hit' on the discriminator will be stored with the bunch crossing tag for ease in sparsification of data.

Figure 5:



Analog Storage Cell.

2.3.3 Analog Storage

Analog storage that will retain a faithful representation of the input signal will be needed to buffer the acquired data prior to A/D conversion. Other requirements are that the storage elements be compact and highly arrayable since each channel will need to have at least 128 storage elements. This will allow approximately 2 microseconds worth of analog data to be stored at an 16 nanosecond interaction rate. In this case, the first level trigger delay will be 2 microseconds or less. It may be possible, after closer investigation of our chip real estate budget, for us to add more analog storage and lengthen the trigger delay to something on the order of 5 microseconds or less. One topology that we have been investigating is shown in Figure 5. Each element of analog data will have to be tagged with a digital word that represents the beam crossing number and the channel number. The digital tag will have to remain linked to the analog data as long as the analog data is held.

It is anticipated that several topologies for the charge-sensitive preamp, shaping circuitry, and analog storage cell will be prototyped using the MOSIS service before

an the optimum is found. All of these functional modules will be tested thoroughly and refined as necessary. In addition the specific work mentioned above, the high-level floorplan for the chip will be developed.

2.4 PHASE II (YEAR 2)

2.4.1 A/D Topologies

Previous readout chips have not incorporated integral A/D converters. Decisions must be made as to how many converters to try to put on a single chip. Its probably not feasible to put a converter per channel in the final chip. Some decision will therefore need to be made relating to the segmentation of the data conversion and readout paths. This determination will need to be made early in the project but in parallel with the development of the data collection channels since ultimately the design restrictions will be those of speed and available chip area. The present resolution target for this converter is 7 bits for adequate charge interpolation between channels. This number may be able to be reduced to 5 bits, but our present estimate will remain conservative. Investigations of an different architectures for the analog/digital converter will be performed Different algorithms for A/D conversion will be studied with a tradeoff being made between speed and power requirements.

2.4.2 Sparsification

Sparsification will be done in the analog portion of the chip. Each channel will have its own discriminator level that will be preset by loading the discriminator level D/A converter during system calibration. Any event that crosses this level will be stored and tagged. If all events are desired, the discriminator need only be set to the lowest possible level. The analog memory will contain only those events that exceed the preset level. The bunch crossing tag memory will be synchronized to the analog memory. When a given bunch crossing is desired, the memory will be read out in a random access manner. In addition, we intend to incorporate some level of nearest neighbor suppression in order to reduce the number of multiple hit occurrences. We believe that if a minimum of 5 adjacent strips are hit, these should all be ignored and not stored.

Work in the second year will build upon the accomplishments of the first year. In general, the functional blocks developed in the first year will be molded into the overall chip architecture. Low level details and issues associated with the chip's functionality and architecture will be addressed, for example, sparsification (specifically discussed above) , real estate tradeoffs, logic to determine how many adjacent strips have been hit, crossing and ID tag generator, interface to a data collection chip, etc. It is anticipated that several prototype chips will be fabricated during this phase. We plan to have a functional non radiation hardened CMOS readout

chip fabricated by the end of the second year.

2.5 PHASE III (YEAR 3)

Work in the third year will be devoted entirely to mapping the proof of concept design developed in year 1 and 2 into an appropriate radiation hardened process. We have already been laying the groundwork for finding an appropriate process. Contact has been made with both AT&T and Harris Semiconductor. A non-disclosure agreement was signed with AT&T and the details of their radiation hardened CMOS process (design rules, process techniques, etc.) are being studied. An agreement with Harris is being pursued that would allow us to beta site some of their new design software in return for access to their fabrication lines. The first phase of this agreement will involve a dielectrically isolated bipolar process that probably will not be appropriate for this project. We will be discussing the possibility with Harris of doing a similar arrangement perhaps using their radiation hardened CMOS line. The plan is to have a functional radiation hardened version of the readout chip at the end of this year.

3 Pixel Detectors

3.1 Bump-bonded Device

It is the primary goal of this collaboration to design the best vertex detector possible for the SSC. Both bump-bonded and integrated pixel devices hold great promise for high resolution vertex detection. We expect to carry out tests of pixel detectors in parallel with the microstrip tests. By combining resources of microstrip and pixel groups we believe that cost savings can be achieved. We plan to test existing pixel detectors in a stand alone mode in the MTEST beam and expect to incorporate pixels into the vertex detector design for the system test. Funding has been requested for the extra costs involved in testing of hybrid (bump-bonded) pixel devices in a separate subsystems proposal which includes groups from SLAC, UCD, UC Berkeley Space Sciences Laboratory, and Hughes Aircraft Corporation. The pixel detector tests are described in detail in the pixel subsystem proposal.

3.2 Integrated Device - Hawaii, Stanford CIS

Work is underway, in a collaboration between the Center for Integrated Systems of Stanford University and the University of Hawaii, on the development of a pixel detector with integrated electronics[5]. The collaboration had its origin in the CIS-UH-CERN development of the Microplex chip, the first VLSI readout for silicon

microstrip detectors, which started in the summer of 1982 and was completed successfully in 1984[6]. At that time UCSC joined the group and work started on the first microstrip vertex detector for colliding beam use (now complete and waiting for installation in the Mark II at SLC in October[7].

Plans for a pixel device were started in 1985, and an initial specific design was proposed in 1987 and funded in 1988 under the SSC generic research and development program[8]. Unlike the Microplex chip, which used a standard nMOS process, this device, with detectors and transistors on the same silicon substrate, requires the development of a new set of fabrication steps. James Plummer, a professor of electrical engineering at Stanford and one of his students, W. Snoeys, have now joined the project. Detailed simulations have been completed, a process test chip (one with specialized structures to test the fabrication steps) has been designed, masks have been made, and the first process test wafers are now being fabricated.

We would like to increase the rate of progress by adding a second student. In addition to the fabrication steps, which must be determined before detailed circuit designs are completed, much work will be required in taking the known techniques for radiation hardness and combining them with the steps for high purity silicon. The basic pixel structure will be optimized for the requirements of the B-physics vertex detector. Detailed circuit design and layout for the on-chip readout including time tagging and information storage during the trigger delay must be completed..

As a point of interest relevant to other detector systems we note that the pixel structure may also be optimized for use as a photon detector. The same set of fabrication steps, with the addition of a transparent, high resistivity layer such as tin oxide, can be used to make a photodiode with nanosecond rise time and capacity one or more orders of magnitude lower than that of PIN diodes. Detailed simulation calculations are now underway.

Funds in this year's contract and expected for next year's should be adequate for W. Snoeys' support, and, if silicon and related costs do not rise significantly, for somewhat more than half of a second student's support ($87K per year including lab charges and technician help where necessary). A group of this size would also be adequate for the preliminary design and simulation calculation for these additional uses. It would need to be increased in size if they were to be undertaken and completed in time for an SSC detector.

We propose here the addition of two graduate students so that a prototype device suitable for B-physics can be fabricated in two years. One student would have primary responsibility for the layout of the circuitry specialized for this application. The other student would concentrate on the fabrication technology for radiation hardness. Depending on the support for graduate students available to the Hawaii-Stanford group from sources outside this proposal, funds under this proposal may be used alternatively for engineering manpower devoted to the radiation hard fabrication.

4 System Testing

4.1 Motivation and Goals

There is as yet no operational experience with full micro-vertex detection in a colliding beam experiment. For e^+e^- experiments this situation will soon change. The ALEPH and DELPHI experiments at LEP and the MARKII experiment at SLC have silicon microstrip vertex detectors either completed or nearly so. Indeed, the MARKII experiment has a three detector, 512 channel (per detector) telescope just outside the beam pipe which has performed satisfactorily in measuring tracks from Z^0 decays. The SLD experiment at SLC will operate a CCD vertex detector in about a year's time. These experiments will provide valuable experience for the SSC. However, there are many key differences between vertex detection at a Z^0 machine and at the SSC. The differences in interaction rates, event multiplicities, and the angular distribution of tracks are dramatic. The CDF experiment at Fermilab will operate a barrel geometry silicon microstrip vertex detector for the first time in 1991. The interaction rate will approach 1 MHz and the event multiplicity will be nearly (about 2/3 of) that at the SSC. The CDF vertex detector will clearly provide relevant experience for the SSC. However, for B-physics there are a number of crucial aspects of vertex detection that will not be addressed by CDF. These aspects include three-dimensional vertexing and tracking over a large range in rapidity. We intend to investigate these and other aspects in detail with a modest-scale prototype of an SSC vertex detector and operate it in colliding beam and/or test beam modes. We will use commercially available double-sided silicon microstrip detectors and readout chips. A detailed plan is presented below.

4.2 Silicon Microstrip Detectors and Micro-mechanical Mounting - Yale

4.2.1 Description

The use of double-sided silicon microstrip detectors provides three-dimensional vertexing capability with a minimum of detector planes. The Oklahoma and Yale groups are developing experience with these devices under existing SSC generic R&D projects. (See the appendix for a description of these programs.) For the system test proposed here, a substantially larger number of wafers will be required.

In the preliminary design shown in Figures 1 and 2 there are 5 different shapes of silicon strip detector. There are 38 wafers per central module and 95K channels. Each central module contains 3 barrels and 2 disks. There are 84 24-channel cables per module. In addition to the central modules, there are forward modules containing 17664 channels partitioned among 6 wafers. We will limit the total channel count in our prototype to 64K by instrumenting only a portion of a barrel section

and parts of at least three disks. The total detector wafer count for the test will be 64, including spares.

The Yale group will supply the double-sided silicon strip detectors and assemble them in an appropriate geometry. We will wire bond the readout chips to the detectors and the cables to the readout chips.

The geometrical layout will be optimized for B-physics using a GEANT based Monte Carlo. A.J. Slaughter has extensive experience with this software and has taken a leading role in simulation studies for BCD. We will use existing computer resources at Yale and Fermilab for this work.

The detailed mechanical design and drawings for the strip detectors will be made using an existing CAD/CAM system at Yale. W. Emmet, mechanical engineer for the Yale HEP group, is expert in using this system.

The silicon detectors will be procured from industry with funds requested under this proposal. We are currently evaluating a double-sided AC-coupled strip detector from Messerschmidt Bolkow Boehm (Munich) and a single sided AC-coupled detector from the Center for Industrial Research (Olso). On the basis of our experience with those detectors and from the experience of our Oklahoma collaborators with DC-coupled doubled sided devices from Micron Semiconductor (U.K.), we will critically evaluate proposals from these and other manufacturers, eg., Hamamatsu. We will also pursue contacts with U.S. companies, although there are none currently involved in strip detector manufacture.

After procurement, we will make I-V measurements of the detectors and test individual strips for punch through of the capacitor. We will use an existing microprobe station (now under procurement) but will require the addition of a specialized probe card to make rapid measurements of a large number of strips.

Wire bonding will be done with an existing machine (also now under procurement) but will require some modifications for semi-automatic operation.

A prototype cable for connection to the readout chips has been made by Carl Lindenmeyer at Fermilab. We will base our cable design on tests of this prototype. Cable manufacture will be subcontracted to industry.

4.2.2 Schedule

In the first year we will specify and procure detectors. Because of the lead time necessary to fabricate masks and manufacture the detectors it is important to establish a contract for commercial production early in the funding cycle.

In the second and subsequent years we will assemble prototype detector structures and use them in the test beam at Fermilab as part of experiment E784 which is

an R and D program for the Bottom Collider Detector. Fermilab is reviewing the possibility of tests in the C0 collision region. If approved, we will also test prototype devices there. We are also exploring the possibility of tests using the CERN $S\overline{P}S$ collider.

4.3 VLSI Readout Chips and Driving Electronics - Albany, Oklahoma

4.3.1 Introduction: Generic SSC R&D

The University of Oklahoma and Oak Ridge National Laboratory are collaborating on a generic Detector R&D project to "Investigate Radiation Hardened Device Technologies for use with Silicon Strip Detectors at the SSC". The project includes the following three tasks:

Task 1: Theoretical studies of electronic device technologies for use at the SSC. (E. J. Kennedy and A. Wu; ORNL and University of Tennessee)

Studies of device technologies have been started using the SPICE simulation program and related VLSI software tools assembled by the Instrument and Controls Division of ORNL. Of particular interest are radiation hardened processes which have been developed by industry. Initial contact has been made with the group which developed the radiation hardened (10 Mrad) CMOS process at AT&T. Copies of the proprietary design rules were obtained under a non-disclosure agreement between AT&T, OU, and ORNL. We expect to obtain post and pre-radiation SPICE files soon which will allow quantitative evaluation of the process for analog applications. Similar arrangements are also being negotiated with Harris Semiconductor Corporation.

Task 2: Experimental evaluation of MOSIS processes for application to radiation hardened readout circuits for solid state tracking detectors at the SSC. (G. Alley; ORNL)

Evaluation of MOSIS processes for application to low noise, radiation insensitive JFET, bipolar, and CMOS devices has been started. We have submitted for fabrication several device structures using the MOSIS p-well CMOS process. Structures submitted include differential pair MOSFET's, differential pair JFET's, substrate bipolar transistors, and MOSFET's using a variety of geometries. These chips have been received and have been irradiated using a cobalt 60 gamma source at UTK. Similar device structures using an n-well process will be fabricated later in the summer. Similar GaAs device structures have also been submitted for fabrication this fall.

Task 3: Radiation testing and evaluation of fabricated devices with solid state tracking detectors. (P. Skubic, G. Kalbfleisch; OU)

Solid state microstrip detectors with two-sided readout will be interfaced to readout devices and will be tested for radiation hardness with neutrons, gammas, and charged particles. This work will be done at the UCD Cyclotron facility (protons and neutrons), at Fermilab in the MTEST beam line (high energy charged particles), and at UTK and/or Hughes Aircraft Corporation (gammas). These tests are described in more detail in a separate subsystems proposal on hybrid pixel detectors.

In order to gain experience and establish procedures in radiation testing, we irradiated a Micron Semiconductor, Inc. double-sided (1mm pitch with orthogonal strips) detector with the cobalt 60 source at the UTK Department of Chemistry. The detector was irradiated without bias voltage with a dose in the range 2-4 Mrad. Studies of the signal to noise ratio (and leakage currents) were performed before and after irradiation as a function of time. No change was observed within the sensitivity of the measurements (+- 15%). We have further tested this detector by irradiating it with bias voltage on with the cobalt 60 source while monitoring the leakage current at the same time. Post irradiation evaluation is now in progress.

The work proposed here can be considered a natural continuation of this generic R&D project. Additional funds for the generic project have been requested for the period October 1, 1989 to September 30, 1990 to finish the work now in progress in a timely fashion. If supplemental operating funds are obtained during the first half of this period, the work proposed here by the ORNL group could begin early in 1990.

4.3.2 VLSI Readout Chips

We are requesting funds in the first year budget for 64,000 channels of VLSI readout. The choice of which readout chip to use in the system tests will be based on the results of the MTEST beam tests which will be completed approximately half way through the first year of the project. The cost of the VLSI readout chips is based on the present price of the CAMEX chip which is $70 per 128 channels (each chip has 64 channels). More information will be available after the first production run of the SVX-D chips is complete, which should occur before the end of 1989. If the yield is high and if the present SVX-D is chosen for the system tests without modification, some reduction in cost may be possible. In order for the system tests to be started during the second year of the project, it is necessary that the readout chips be ordered before the end of the first year since long lead times are required for delivery and testing.

4.3.3 Driving Electronics

The driving electronics for the readout chips will be developed by the Oklahoma group in collaboration with The State University of New York at Albany. We will build on our experience in constructing the CAMAC sequencer and ADC modules

which are used to read out the SVX chip. We have constructed two sets of these modules and are testing them now. The CDF experiment will use a FASTBUS version of this system to readout the CDF vertex detector during the next colliding beam run at Fermilab. If this system is available on schedule, it would satisfy our requirements for the system test at C0. We are therefore requesting funds in this proposal to purchase electronics for reading out 64,000 channels based on the preliminary design for CDF. This would require one FASTBUS sequencer module which would control four buffer modules, each of which controls a RABBIT crate with eight ADC modules. Sixteen SVX chips would then be read out by each ADC module. We are requesting funds in the first year for one sequencer, one buffer module and RABBIT crate, and two ADC modules which can be used for testing and software development as soon as they are available. The balance of thirty ADC modules, three buffer modules and RABBIT crates can then be purchased with second year funds.

At the end of the MTEST beam run during the first year of the project, we will decide which readout chip and detector type to use in the C0 system test. At that time, if the SVX chip is chosen and data sparsification works according to design, an option exists to use an expanded version of the CAMAC readout system. Five sets of existing sequencer and ADC modules could be used in parallel to read out sparsified data at 9600 bytes/event at a rate of 50 events/second which is the estimated interaction rate for a C0 test run. (This assumes a factor of 100 less luminosity at C0 than at B0 and that we instrument only 10% of the bunch length.) This option would require construction of a factor of 8 multiplexing module for each set of SRS-SDA modules to allow addressing and readout of all the SVX chips in the complete vertex detector subsystem. The cost of the CAMAC option would be less than that for the FASTBUS readout based on preliminary cost estimates for that system.

Software and testing responsibilities will be divided between the Oklahoma and Albany groups. A set of CAMAC readout modules will be supplied to Albany by OU at cost so both groups will have compatible systems. If the FASTBUS system is used in the C0 test, it will be necessary for Albany to obtain a FASTBUS crate and segment manager. (OU has these items already.) Funds for this will then be requested in the second year Albany budget.

4.3.4 Schedule

1 to 6 months: Complete MTEST data run comparison of SVX and CAMEX readouts and double-sided microstrip detectors.

6-12 months: Choose readout chip and detector for C0 system tests. Place orders for readout chips and driving electronics.

13-18 months: Bench testing of driving electronics and readout chips at home in-

stitutions and develop software.

19-24 months: Construct and assemble hardware at system test beam site (C0?). Initial testing of combined subsystem and data acquisition computer hardware.

4.4 Data Acquisition and Macro-mechanical Mounting - Iowa

4.4.1 Overview

(E. McCliment)

I am currently involved in two phases of the Fermilab fixed-target test of elements of the proposed BCD detector: the design and construction of a test stand, and development of the online data acquisition (DAQ) system. Because the central vertex detector is to be a principal element of the BCD detector for the SSC, I propose to continue this work to develop the mechanical mountings and hardware for a practical 4-pi vertex detector for the SSC, and to develop DAQ hardware and software for the detector readout. This work will be carried out in collaboration with the university efforts at Hawaii, Oklahoma, Stanford, State University of New York at Albany, Hawaii, and Yale, and with Oak Ridge National Laboratory.

4.4.2 Macro-Mechanical Mounting

Elements of the BCD detector will be tested in a test beam at Fermilab during the latter part of the next fixed target running period. The test stand has been designed for this purpose by ERM and C. Lindenmeyer. The test stand provides maximum flexibility to investigate various schemes of assembly and testing of the components of a 4-pi silicon vertex detector within a fixed-target environment. The rotatable planes allow one to simulate the effects of particles passing through silicon microstrip detectors at large angles away from the normal to the detector surfaces as happens in a colliding beam environment. The snap-in Pyrex glass planes are easily removable and can be rotated through 90 deg so that other subassemblies such as a preassembled configuration of silicon strip detectors (SSD's) can be mounted on the test stand. The thermal jacket will allow temperature studies to be done on the SSD system. Fabrication of the components for this test stand is now underway in the U of I Physics and Astronomy shop. The assembly and testing of the stand will be done at U of I before it is brought to the Mtest area at Fermilab.

It is proposed to continue and extend this work to actual mechanical mounting systems for the SSC BCD 4-pi silicon vertex detector system. Studies of mechanical, thermal, and electrical properties of the mounting initiated at Fermilab by H. Jostlein must be continued to ensure mechanical stability to within a few microns, dissipation of approximately 1 kW of heat generated by the readout chips, temperature stability within 1 deg C, proper rf shielding of the detector elements,

and reasonable cabling configurations. The shop facilities in the U of I Physics and Astronomy Dept. are well suited to this project. It is envisioned, for example, that magnesium will be the material of choice for the mounting to keep the mass as low as possible. The U of I shop has the facilities and expertise to work with this material, having done this on several projects in the past. We also have available an engineering staff and full CAD system to aid in the mechanical and electrical design. (The presence of this infrastructure is the result of a large space science effort.)

4.4.3 Data Acquisition Hardware

Last summer at Fermilab I participated (along with Fermilab staff physicist L. Stutte and Yale graduate student S. Utku) in an effort to put together an online data acquisition system at Fermilab for the fixed- target test of the BCD detector elements. We succeeded in reading out a Lecroy Fast Encoding Readout ADC (FERA Lecroy 4300B), its driver (Lecroy 4301), and memory module (Lecroy 4302), which will be used by P. Karchin to process data from CAMEX SSD integrated readout chips in the fixed-target test alluded to above. This was done first with the simple CAMAC diagnostic program DDL, and then incorporated into the VAX-ONLINE data acquisition software that will be used in the fixed-target test. The Iowa group is also committed to supplying an SSD system to measure the beam position in (fixed-target) experiment E781 at Fermilab (A Segmented Large X Detector to study charmed baryon production and decay.) This system will make use of a Berkeley readout system including SVX integrated readout chips plus the SRS pattern generator/chip controller and SDA data collection modules. The silicon detectors are currently on order from Hamamatsu and the readout chips from Berkeley. I mention this because it means I will have experience with SSD systems that have LSI chip readouts. The Berkeley system is a serial readout system that requires approximately 1 μs per channel, all the data moves through a single flash ADC on the data collection board, and this board has only about 2000 words of memory. If every strip were hit this would mean that one SDA module would be needed to service every 2000 strips and would require 2 ms to read out. With data sparsification the readout speed increases by an order of magnitude, but with 10^6 strips in the complete vertex detector 50 SDA modules need to be read out. The situation is somewhat better with the Lecroy FERA ADC's which have 16 channels per module. However, the data rate here is 4.8 μs per channel and essentially the same memory size, so there is overall only a factor of 4 improvement. Either scheme is thus adequate for low data rates. To handle much higher data rates at the SSC will require significant improvements in data acquisition. To produce a more SSC-worthy DAQ I propose first to adapt the Berkeley pattern generator/chip controller and data-collection modules to a FASTBUS-based data collection system and to evaluate their performance, first in bench tests then in a beam test, most likely the "C0" test at Fermilab (1992.) This will require effort in both hardware and software. The work on the hardware will be done with the assistance of an electronic

engineer staff in the U of I physics department and the electronics assembly shop. Secondly, I propose to introduce parallelism into the data acquisition by means of an ACP farm to process the data from each of the memory units in parallel.

4.4.4 Data Acquisition Software

The VAXONLINE software developed for use by CDF at Fermilab provides a general framework for online data acquisition. VAXONLINE is organized into "producers" that communicate directly with the hardware (both CAMAC and FASTBUS versions are available), a data pool where data from various parts of the experiment are collected, and "consumers" to process the data and store it on tape. As alluded to above some preliminary work has been done on a "producer" for BCD. A producer was written to read out the Lecroy FERA ADC system, which will be used in the fixed- target and C0 collider test runs at Fermilab. A producer for a FASTBUS version of the data collection module needs to be written and tested. Also, a full consumer has yet to be written. At present only the barest skeleton of a consumer exists for the fixed-target test, namely one that histograms the hit channels. I propose to write a producer and consumer to handle data from the FASTBUS version of the Berkeley modules and the FERA system. I also intend to write pattern recognition software to reconstruct space points from the hits in the SSD's. And I propose to write the software for the parallel data processing on the ACP farm alluded to above.

4.4.5 Schedule and Support

I believe the work on both the hardware and software can be accomplished within carried a two-year period with the aid of one Iowa graduate student and the technical support personnel at the University of Iowa. I ask for the following manpower support:

Salary and benefits for one 1/2-time graduate student; Travel for myself and the student; Six months shop time; Two months electrical engineering time; and Two months mechanical engineering/computer aided design.

Note:The University has contributed to the BCD effort by bearing the full manpower cost for machining the components of the fixed-target test stand.

I also ask for the following hardware on a 50% matching basis with the University of Iowa:

A Vax 3200 work station; A fastbus crate and segment manager.

I believe these requests to be necessary to accomplish the proposed development of the macro-mechanical mounting of the vertex detector, and development of the proposed DAQ system.

5 Budget

5.1 State University of New York at Albany

At Albany, we have a CAMAC test setup, based on the LeCroy3500 Data Acquisition System, which uses the Intel8085 8-bit microprocessor and $8\frac{1}{2}$ floppy drives. The system has limited memory and can record data only at a few kilohertz. Further, the available software is very limited. In fact, the system is a major bottleneck in our setup. We would like to update to a PC-based system but also desire portability so that we can carry the setup to different accelerator laboratories for testing purposes.

We need to set up a small electronic shop with printed circuit fabrication facility.

The details of the equipment budget we request follows.

First Year Budget

Equipment

Data Acquisition	
Laptop PC-386 system with VGA, $5\frac{1}{4}$ and $3\frac{1}{2}$ disk drives,	
40 MB Hard disk drive, Mouse, Modem	\$3,500
PC-to-CAMAC Interface. Kinetics Corp. 3922 Crate	2,500
Controller and 2926 IBM PC Interface Card	
PC CAMAC driver software	250
Total	\$6,250
CAMAC Instrumentation	
LeCroy 8013A Benchtop 13 slot CAMAC Power Bin	2,450
ADC/TDC Calibration Module. Phillips Scientific 7120	2,250
Total	\$4,700
NIM Instrumentation	
High Power NIM bin and power supply. LeCroy 1403	2,830
Quad two-fold logic unit. LeCroy 622	995
Triple 4-fold logic unit. LeCroy 465	1,195
Two-channel four-fold logic majority unit. LeCroy 365AL	1,045
Digital Readout Visual Scaler (BNC)	1,500
NIM pocket pulser	65
Total	\$7,630
Electronic Shop	
PCB software	1,500
Board etching machine	1,500
Total	\$3,000
Miscellaneous	
Limo cables, connectors, etc.	2,000
Oscilloscope	
LeCroy 9400 Fast waveform digitizing scope	8,900
EQUIPMENT TOTAL	\$32,480

Travel

Travel to Collaborators	
6 trips x $1,000 each	$6,000
Instrumentation Conferences	
1 x $1,000 each	1,000
TRAVEL TOTAL	$7,000

Salaries

Graduate Students	
Full time students	12,000
2 Summer students	5,000
Total	$17,000

TOTAL DIRECT COSTS

Equipment + Travel + Salaries	$56,480

TOTAL INDIRECT COSTS

(Travel + Salaries)× .521	$12,504

TOTAL BUDGET FIRST YEAR $68,984

Second Year Budget

Equipment	
Fastbus Data Acquisition System	$40,000
Travel	
Same as first year	7,000
Salaries	
Same as first year	17,000
Total Direct Costs	$64,000
Total Indirect Costs	$12,504
TOTAL BUDGET SECOND YEAR	$76,504

5.2 University of Hawaii

Cost Per Year for First and Second Years

2 graduate student salaries	$30,000
lab costs	24,000
supplies - wafers, etc.	20,000
computer time	10,000
engineering consulting time with CIS staff	10,000
technician time	40,000
SUBTOTAL	$134,000
OVERHEAD (@30%)	$40,000
TOTAL COST	$174,000

5.3 University of Iowa

1 June 1990 through May 1991

A-II(a) - REIMBURSABLE OF COST-SHARING PORTION

Salaries and Wages	
Scientific Discipline Personnel	
Principal Investigator, E. R. McCliment,	
Professor - no salary support	$0
Graduate Research Assistant, 50% time for 2 summers	
months at $1,233/mo., and 50% time for AY 1990 - 91	
at $1,289/mo.	14,066
Support Personnel	
Electrical Engineer, $3,400/mo. for 2 months	6,800
Mechanical Engineer, $4,400/mo. for 4 months	17,600
Machinist, $2570/mo. for 6.0 months	15,420
Secretary, $2070/mo. for 0.5 months	1,035
SALARIES AND WAGES SUBTOTAL	$54,921
Permanent Equipment	
Computer Equipment: VAX3200	15,000
Laboratory Equipment:	7,500
1 fastbus crate + programmable segment manager	
PERMANENT EQUIPMENT SUBTOTAL	$22,500
Expendable Supplies and Materials	
Magnesium and other machining materials	2,000
Electronic components and miscellaneous	
expendable supplies and materials	500
Computer	500
EXPENDABLE SUPPLIES SUBTOTAL	$3,000

Publications	
(No publications charge)	$0
Travel	
Collaboration meetings at the SSC Dallas, TX, 4 trips/yr, 2 days/trip; air fare at $620/trips, subsistence at $107/day, and car rental $50/day.	3,738
Collaboration meetings at FNAL, 4 trips for 2 days each; air fare $218/trip, and subsistence at $113/day.	1,776
TRAVEL SUBTOTAL	$5,512
Other Direct Costs	
Staff Benefits: retirement, FICA and insurance; 25% of Professional Salaries ($24,401), and 28% of general service staff salaries ($16,455).	11,439
Xerographic, photographic, and other technical services, telephone usage	1,186
CAD/CAM usage, 100 hours at $20/hr	2,000
OTHER DIRECT COSTS SUBTOTAL	$14,625
Total Direct Costs	100,558
Indirect Costs	
39.0% of modified total direct costs (MTDC) for on-campus research activities ($78,058)	30,042
TOTAL COST	$131,000

It is requested that the Department of Energy provide 100% of the A-II(a) portion of $131,000.

A-II(b) - ITEMS EXCLUDED FROM COST-SHARING TO BE FURNISHED BY THE UNIVERSITY OF IOWA

Computer equipment (50% of total cost)	$15,000
Laboratory equipment (50% of total cost)	7,500
Total	**$22,500**

A-II(c) - UNIVERSITY CONTRIBUTION OF PRINCIPAL INVESTIGATOR

Principal Investigator, E. R. McCliment, 5% of time during the academic year.
(* 50% of the permanent equipment will be paid by the University of Iowa)

1 June 1991 through 31 May 1992

A-II(a) - REIMBURSABLE OR COST-SHARING PORTION

Salaries and Wages	
Scientific Discipline Personnel	
Principal Investigator, E.R. McCliment,	
Professor - no salary support -	$0
Graduate Research Assistant, 50% time	
for 9 month academic year and 2 summer	
months at $1,289/mo., for AY 1990-91 at	
$1,367/mo. for AY 1990	14,878
Support Personnel	
Machinist, $2,776/mo. for 6.0 months	16,656
Secretary, $2,236/mo. for 0.5 months	1,118
SALARIES AND WAGES SUBTOTAL	$32,652
Permanent Equipment	
(No equipment)	$0
Expendable Supplies and Materials	
Magnesium, and other machining materials	2,000
Miscellaneous expendable supplies and	
materials	500
Computer software	500
EXPENDABLE SUPPLIES SUBTOTAL	$3,000
Publications	
Journal page charges, Phy Rev. D.	500

Travel	
Collaboration meetings at FNAL, 4 trips for 2 days each; air fare at $229/trip and subsistence at $119/day	1,868
Collaboration meetings, SSD, Dallas, TX, 4 trips/yr, 2 days/trip; air fare at $651/trip, subsistence at $112/day	3,500
TRAVEL SUBTOTAL	$5,368
Other Direct Cost	
Staff Benefits: retirement, FICA and insurance; and 28% of general service staff salaries ($17,774)	4,977
DEC Microcomputer maintenance	3,000
Xerographic, photographic, and other technical services, telephone usage, etc.	863
OTHER DIRECT COSTS SUBTOTAL	$8,840
Total Direct Costs	50,360
Indirect Costs	
39.0% of modified total direct costs (MTDC) for on-campus activities ($50,360)	19,640
TOTAL COST	$70,000

It is requested that the Department of Energy provide 100% of the A-II(a) portion of $70,000

A-II(b) - ITEMS EXCLUDED FORM COST-SHARING TO BE FURNISHED BY THE UNIVERSITY OF IOWA

None $0

A-II(c) - UNIVERSITY CONTRIBUTION OF PRINCIPAL INVESTIGATOR

Principal Investigator, E. R. McCliment, 5%
of time during the academic year.

5.4 Oak Ridge National Laboratory

Budget

First Year

Labor (2 man-yrs. @ $80.2K/yr.)	$160,400
ASIC Fab. (4 "Tiny Chips" 2u, 2 ea. 4600X6800 1.2u)	25,000
Material	10,000
Miscellaneous	0
Subtotal	$195,400
Indirect	78,160
Total	$273,560

Second Year

Labor (2 man-yrs. @ $84.2K/yr.)	$168,400
ASIC Fab. (4 "Tiny Chips" 2u, 2 ea. 7900x9200 1.2u)	70,000
Material	10,000
Miscellaneous	0
Subtotal	$248,400
Indirect	$99,360
Total	$347,760

Third Year

Labor (2 man-yrs. @ $88.4K/yr.)	$176,800
ASIC Fab. (Rad. Hard Fab. Run)	125,000
Material	20,000
Misc. (Rad. Testing)	1,500
Subtotal	$323,300
Indirect	$129,320
Total	$452,620

5.5 University of Oklahoma

FIRST YEAR OU BUDGET

April 1, 1990 to March 31, 1991

Operating Expenses	
Travel (12 trips to Fermilab @ $500 per trip)	$6,000
Graduate Student Salary	12,000
Undergraduate Student Salary	4,500
Permanent Equipment	
LeCroy qvt NIM module	4,000
1 ea. FASTBUS sequencer module	10,000
1 ea. RABBIT crate buffer module	1,000
2 ea. RABBIT crate ADC modules	4,000
1 ea. RABBIT crate	1,000
64K channels of SVX-D or CAMEX microstrip detector readout circuits @ $70 per 128 channels	35,000
Total Direct Costs	$77,500
Indirect Costs	
26% MTDC as set by DHHS on 2/10/89	$5,850
TOTAL COSTS Year 1	$83,350

SECOND YEAR OU BUDGET

April 1, 1991 to March 31, 1992

Operating Expenses	
Travel (12 trips to Fermilab @ $500 per trip)	$6,000
Graduate Student Salary	12,000
Undergraduate Student Salary	4,500
Permanent Equipment	
3 ea. RABBIT crate buffer modules	3,000
30 ea. RABBIT crate ADC modules	60,000
3 ea. RABBIT crates	3,000
Total Direct Costs	$88,500
Indirect Costs	
26% MTDC as set by DHHS on 2/10/89	$5,850
TOTAL COSTS Year 2	$94,350

5.6 Stanford University - Center for Integrated Systems

Costs will be reimbursed through the University of Hawaii.

5.7 Yale University

First Year Budget

It is assumed that 6 months of post-doctoral research physicist time will be funded from the generic SSC R&D program and so it is not included here. Another six months will be funded from other HEP funds.

32 double sided AC-coupled silicon microstrip detectors including mask design	$68,000
probe card and spare to assist in testing	3,000
modifications for semi-automatic bonding	5,000
cables for connection of readout chips to driving electronics	5,000
3 months mech. engineering time	30,000
student technician - 6 months	9,000
12 months - graduate student	9,000
travel to manufacturers	5,000
TOTAL	$134,000

Second Year Budget

Note that the 6-months of research physicist time is now included as part of the subsystem effort. The other 6 months will continue to be paid from HEP funds.

32 double sided AC-coupled silicon microstrip detectors	$32,000
6 months post-doctoral research physicist	30,000
student technician - 6 months	9,000
12 months - graduate student	9,000
TOTAL	$80,000

6 Appendix on Generic SSC R&D

6.1 University of Oklahoma

The University of Oklahoma group has ordered 10 double-sided microstrip detectors from Micron Semiconductor, Inc. These detectors, which were purchased from University matching funds, will be delivered this fall and will be tested at Fermilab during the next fixed target run in the MTEST beam line. We have also ordered SVX-D readout chips to be used in the Fermilab tests from the next production run in collaboration with UC Berkeley and Carnegie Mellon University. The readout chips will be wire bonded to the detectors and will be readout with UC Berkeley designed CAMAC sequencer (SRS) and flash ADC (SDA) modules which are presently under construction at OU. The purpose of these tests is to measure position resolution of high energy particle tracks as a function of incident angle. The performance of various types of microstrip detectors and readout circuits (including SVX and CAMEX chips) will be compared during stand alone tests by the OU and Yale groups. At the end of the tests, the best combination of detector and readout chip will be chosen for a larger scale system test of an actual SSC design for a vertex detector based on a 2.54 cm. diameter beam pipe.

6.2 Yale University

6.2.1 Silicon Detectors and Readout Electronics

Vertex detector R&D has already begun at Yale under the generic SSC program to evaluate VLSI readout electronics for silicon strip detectors[11].

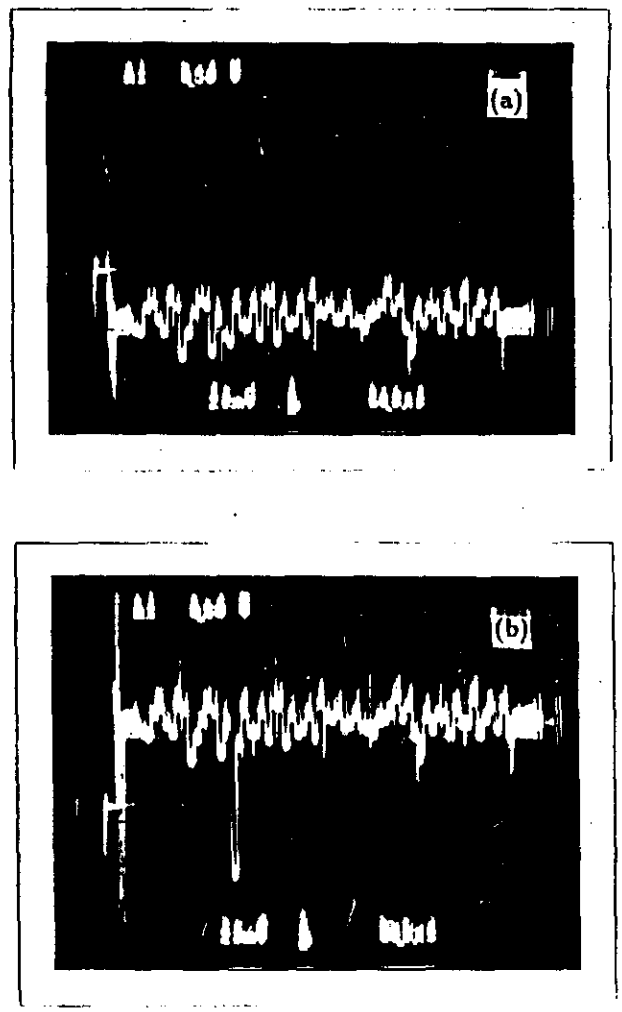
A flexible test station has been set up at Yale to operate silicon strip readout chips at a variety of speeds. P. Karchin, W. Ross, and E. Wolin have been working on these bench tests. We can now inject test signals into the analog inputs of the CAMEX silion strip readout chip and see the response of the analog output on an oscilloscope as shown in Figure 6.

We have begun measurements of microstrip detectors procured from the Center for Industrial Research in Oslo and from Messerschmidt Bolkow Boehm in Munich. With our continuing studies at Yale, we are developing the practical expertise necessary to mount an experiment with these devices.

As part of Fermilab experiment E784, prototype silicon detectors will be operated in a test beam during the fixed target run in 1990. A. J. Slaughter and S. Utku, a Yale graduate student, have been preparing a computer interface and readout at Fermilab that can be used with various microplex chips.

The electrical engineering department at Fermilab is developing a readout chip for

Figure 6:



Waveform from the analog output of the CAMEX silicon strip readout chip using the test stand at Yale. No input charge is applied in (a) while a test pulse simulating a minimum ionising particle in the microstrip detector is applied to all channels in (b). The 64 channels are interrogated sequentially to produce the waveform shown. Channels 0, 15, 48, and 63 show more noise than the others because these channels have a 12 pF capacitor connected to their input to simulate the capacitive load of the microstrip detector.

silicon strip detectors that will include an analog time delay circuit, a feature that is required at both Fermilab and the SSC. P. Karchin is the liason physicist from E784 for the development of this chip and has worked closely with Fermilab on its design. Tests of the existing chips are an important input to the design of the new Fermilab chip.

6.2.2 Mechanical Assembly

In June, 1989 we proposed a generic SSC research program to develop new methods of assembling multi-element microvertex detectors. That program is essential to develop the techniques for the system test. The generic program will develop the methods of mechanical assembly necessary to achieve the requirements for gluing, wire bonding, electrical shielding, precision alignment, and thermal cooling. The reader is referred to the generic proposal[12] for a detailed discussion.

Under the generic proposal, funding is requested for the key equipment to do this work: a wedge bonding machine and a microprobe station. J. Sinnott, mechanical technician with the Yale HEP group, is coordinating the purchase of this equipment. Also requested under the generic proposal is 50% of the salary of a post-doctoral physicist. Funding for the other 50% is requested from the high energy physics research branch of the DOE, including funds under the OJI program. We are planning to start this position on May 1, 1990.

7 Environmental Statement

We do not present an environmental assessment of our research program for the following reasons.

1. We are not producing any equipment item which falls into the category of major equipment as defined in the "Guidance for Preparation of Environmental Assessment."

2. The potential environmental impact of our research program derives from the use of the high energy beams used in our experiments. The environmental aspects of the high energy accelerator which produce these beams are presumably covered in the assessments provided by the National Laboratories that operate the accelerator and manage the research program with them.

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