Development of the Readout System for CTA Using the DRS4 Waveform Digitizing Chip

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Abstract: We have developed a prototype of the photomultiplier tube (PMT) readout system for the next generation VHE gamma-ray observatory, the Cherenkov Telescope Array (CTA). Several thousand PMTs along with their readout systems are arranged on the focal plane of each telescope, with one readout system per 7-PMT cluster. The signal from a PMT detecting Cherenkov light from an air shower is amplified, and the waveform is then digitized at a sampling rate of the order of GHz using an analog memory ASIC developed at Paul Scherrer Institute (PSI), called the Domino Ring Sampler (DRS4). The sampler has 1,024 capacitors per channel and the ability to cascade channels for increased depth. After a trigger is generated in the system, the charges stored in the capacitors are digitized by an external slow sampling ADC and then transmitted via Gigabit Ethernet. An onboard FPGA controls the DRS4, trigger threshold, and Ethernet transfer. In addition, the control and monitoring of the Cockcroft–Walton circuit that provides high voltage for the 7-PMT cluster are done by the same FPGA. Using a prototype named *Dragon* we successfully obtained a pulse shape of a PMT signal at a sampling rate of 2 GS/s and a single photoelectron spectrum.

Keywords: Imaging Atmospheric Cherenkov Telescope, Gamma-rays, Electronics.

1 Introduction

A ground-based imaging atmospheric Cherenkov telescope (IACT) measures Cherenkov light from an extended air shower (EAS) generated by the interaction between very high energy (VHE) gamma rays and the upper atmosphere. Night sky background (NSB) also enters a pixel photon sensor of the focal plane of the IACT with a rate of the order of 10–100 MHz, depending on the mirror size and the pixel size. In some region of the Galactic plane, the NSB can reach on average up to 400 MHz. The NSB therefore becomes noise that affects the sensitivity and the energy threshold. Given this NSB pollution, and the fact that the duration of Cherenkov light from EAS is a few nanoseconds, a fast digitization speed of the readout system coupled to a fast photosensor like a photomultiplier tube (PMT) is beneficial to increase the pixels' signal-to-noise ratio. In addition, this system should be compact and have low cost and low power consumption because each IACT possesses several thousand photon sensor pixels and the readout system attached to the sensors is in a camera container located at the focal position. Furthermore, a wide dynamic range of

more than 8–10 bits is required to resolve a single photoelectron and have a wider energy range.

A commercial flash analog-to-digital converter (ADC) satisfies the requirement of a wide dynamic range. However, it is costly and consumes relatively high power of a few watts per channel. On the other hand, an analog memory application specific integrated circuit (ASIC), that consists of several hundred to several thousand switched capacitor arrays (SCA) per channel, can sample a signal at the order of GHz, with a wide dynamic range and lower power consumption. Several types of analog memory ASICs have been developed for applications in particle physics and cosmic ray physics. With respect to IACTs, a modified version of ARS0 [1], Swift Analog Memory (SAM) [2], and Domino Ring Sampler (DRS) [3] chips are used in the H.E.S.S.-I, H.E.S.S.-II, and MAGIC experiments, respectively.

Cherenkov Telescope Array (CTA) [4] is the next generation VHE gamma-ray observatory, which improves the sensitivity by a factor of 10 in the range 100 GeV–10 TeV and an extension to energies well below 100 GeV and above 100 TeV. CTA consists of telescopes having mirrors with size 20–30 m, 10–12 m, 3.5–7 m, and ~50 m^2, which are called large size telescope (LST), medium size telescope (MST), small size telescope (SST), and Schwarzschild-Couder telescope (SCT), respectively. Several types of readout systems are developed for CTA with different analog memories for the requirements of LST, MST, SST, and SCT (CTA-US). At the same time, there has been progress in the development of photon sensors such as PMT and a Geiger-mode avalanche photodiode (or silicon photomultiplier) for CTA. At this time, the primary candidate is a PMT.

Using the analog memory DRS version 4 (hereafter DRS4), we have so far developed two versions of prototypes for the PMT readout system for CTA, named *Dragon*. Using the first version of the prototype, we demonstrated that the waveform of a PMT signal can be well digitized with the DRS4 chip. The second version of the prototype was developed based on the first version, with improvements made to the sampling depth of DRS4 and a trigger. In this paper, we report the design and performance of the second version of the prototype.

2 Design of Readout System

2.1 Overview

Several thousand PMTs and their readout systems are arranged on the focal plane of each telescope, with one readout system per 7-PMT cluster. We have developed a prototype of the PMT readout system. Figures 1 and 2 show a photograph and block diagram of the prototype, respectively. The prototype consists of a 7-PMT cluster, a slow control board and a DRS4 readout board. The total size is 14 cm × 60 cm. The 7-PMT cluster and the slow control board are described in detail in reference [5]. In this paper, a brief description is provided.

Our 7-PMT cluster consists of seven head-on type PMTs with a super-bialkali photocathode and 8-stage dynodes (Hamamatsu Photonics, R11920-100 with a diameter of 38 mm), a Cockcroft–Walton (CW) circuit for high voltage supply to the PMTs (designed by Hamamatsu Photonics), and a preamplifier board. A signal from the PMT is amplified by the preamplifier (Mini-circuits LEE-39+), and fed to the DRS4 readout board.

On the DRS4 readout board the preamplified signal is divided into three lines: a high gain channel, a low gain channel, and a trigger channel. The high and low gain channels are connected to DRS4 chips. The signal is sampled at a rate of the order of GHz and the waveform is stored in a SCA in DRS4. When a trigger is generated in the trigger circuit, the voltages stored in the capacitor array are sequentially output and then digitized by an external slow sampling (~30 MHz) ADC. The digitized data is sent to a field programmable gate array (FPGA) and then transmitted to a gigabit ethernet transceiver and a backplane via a data input/output (I/O) connector. The FPGA controls a static random access memory (SRAM) that stores large amounts of data before transmission and a digital-to-analog convertor (DAC) used for thresholding in the trigger circuit.

The slow control board is equipped with a generator for generating test pulses that are fed to the preamplifier, a temperature and humidity sensor with I^2C interface, a DAC for setting the voltage of the CW high voltage circuit, and an ADC for monitoring both the CW circuit and the DC anode current. These devices on the slow control board are controlled by a complex programmable logic device (CPLD). Since the CPLD communicates with the FPGA on the DRS4 readout board, the data to and from the CPLD is sent via the Ethernet.

The power supply to the DRS4 readout board and the slow control board is ±3.3V and +5V. The total power consumption is ~2W per channel.

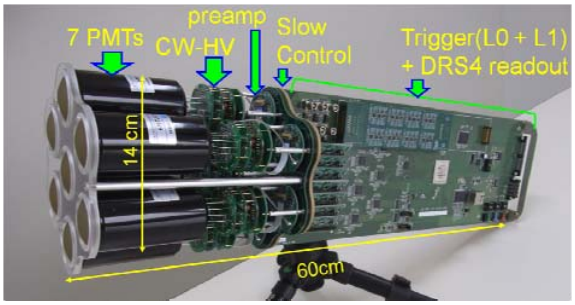

Figure 1. Photograph of the 7-PMT cluster and readout system (ver. 2).

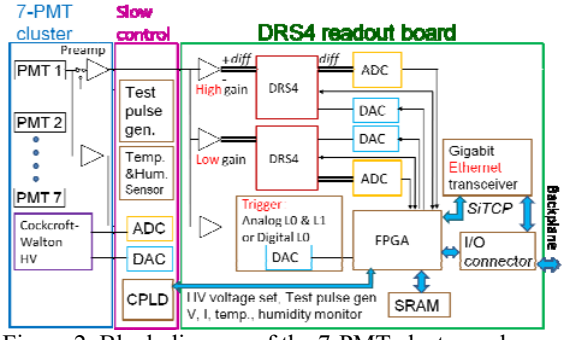

Figure 2. Block diagram of the 7-PMT cluster and readout system (ver. 2).

2.2 DRS4 Readout Board

Figure 3 shows a photograph of the DRS4 readout board with a size of 14 cm × 41.5 cm. The slow control board attached to the 7-PMT cluster is connected to the DRS4 readout board from the right side via two card-edge connectors. The DRS4 board has eight DRS4 chips, ADCs for digitizing a signal stored in the capacitor array in DRS4 at a sampling frequency of 25 MHz, a DAC to control the DRS4, a FPGA (Xilinx Virtex-4), a 18Mbit SRAM, a Gigabit Ethernet transceiver, and a data I/O connector to the backplane. In addition, seven pieces of main amplifier mezzanines, analog level 0 (L0) and 1 (L1) trigger mezzanines, and a digital level 0 (L0) trigger mezzanine are mounted on the DRS4 board. Details of these parts are described in the following subsections.

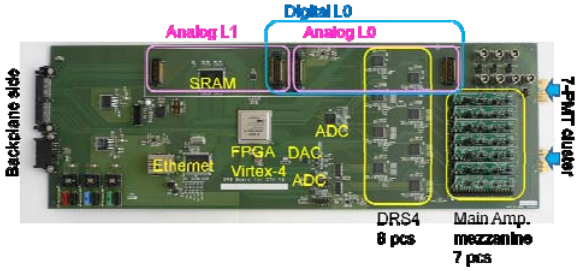

Figure 3. Photograph of the DRS4 readout board (ver. 2).

2.3 Main Amplifier

Figure 4 shows a photograph of the main amplifier mezzanine with a size of 1.8 cm × 5 cm. One part of the mezzanine receives a signal from one PMT. The block diagram is shown in Fig. 5, and is designed to have a bandwidth greater than 350 MHz, lower power consumption, and a dynamic range of 0.2–3000 photoelectrons for LST. A preamplified signal from a PMT with a typical gain of 4×10^4 is fed to the main amplifier mezzanine. The signal is amplified using two differential amplifiers to meet the requirement for bandwidth and power consumption. For a high gain channel, it is amplified by a gain of 9 using Analog Devices, ADA4927. For a trigger, it is amplified by a gain of 4 using Analog Devices, ADA4927 and ADA4950. For a low gain channel, the preamplified signal is attenuated by 1/4 and then buffered with a differential amplifier using Analog Devices, ADA4950.

Figure 4. Photograph of the main amplifier mezzanine.

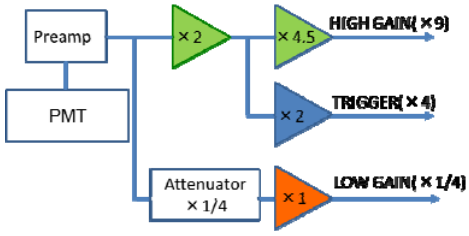

Figure 5. Block diagram of the main amplifier mezzanine.

2.4 Trigger

Figure 6 shows a photograph of a 4.1 cm × 16.5 cm digital L0 trigger mezzanine mounted on the DRS4 readout board. Its block diagram is shown in Fig. 7. A differential signal from the trigger channel of the main amplifier mezzanine (Figure 5) is fed to the digital trigger mezzanine through the DRS4 readout board. The signal is amplified with Analog Devices, ADA4187, and then fed to a comparator (Analog Devices, ADCMP604). A low voltage differential signaling (LVDS) output from the comparator is sent to the FPGA on the DRS4 readout board. This FPGA controls a DAC (Linear Technology, LTC2634) for thresholding of the comparator.

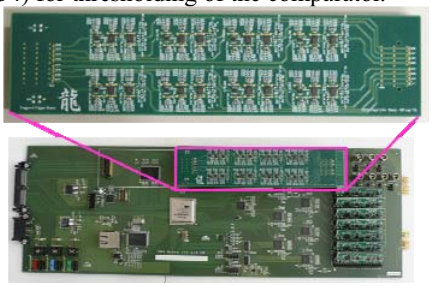

Figure 6. Photograph of the digital trigger mezzanine.

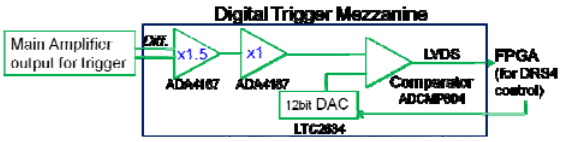

Figure 7. Block diagram of digital trigger mezzanine.

In the current phase of the CTA project, two methods of trigger generation are being developed: the digital trigger and the analog trigger. In the first version of our readout system, only the digital trigger mezzanine can be mounted. However, in the second version, the analog trigger mezzanines with level 0 or 1 can also be mounted as shown in Fig. 3. Performance evaluation of the DRS4 readout board with the analog trigger mezzanines is not yet complete. Therefore, in this paper, we report the performance of the readout system with the digital trigger mezzanine. The generated trigger is distributed via the backplane to FPGAs on backplanes of surrounding PMT clusters to generate a L1 trigger by coincidence of L0 triggers.

2.5 DRS4 chip

The DRS chip is being developed at the Paul Scherrer Institute (PSI), Switzerland, for the MEG experiment [3]. Four versions of the DRS chip have been designed so far by improving the functionality and performance in each version. The second version, DRS2, is used in the MAGIC-II experiment [6], and will be replaced with the current version, DRS4. The DRS4 chip includes nine differential input channels at a sampling speed of 700 MS/s–5 GS/s, with a bandwidth of 950 MHz, and a low noise of 0.35 mV after offset correction. The analog waveform is stored in 1,024 sampling capacitors per channel and the waveform can be read out after sampling via a shift register that is clocked at a maximum of 33 MHz for digitization using an external ADC. A write signal is generated

for the sampling capacitors by a chain of inverters in the chip, and is stabilized by a phase locked loop (PLL). The power consumption of the DRS4 chip is 17.5 mW per channel at 2 GS/s sampling rate. The chip is fabricated using the 0.25 μm CMOS technology and is available in a 76-pin QFN package with a size of 9 mm × 9 mm.

It is possible to cascade two or more channels to obtain deeper sampling depth. In the first version of our readout system, the DRS4 chip was not cascaded. In the second version, four channels were cascaded, leading to a sampling depth of 4,096 for each PMT signal, which corresponds to a depth of 4 μs at 1 GS/s sampling rate. It enables continuous sampling without waiting the decision of trigger coincidence between multiple telescopes when a trigger of the local telescope is generated.

2.6 Self Calibration Function for DRS4

In the second version of the readout board, we implemented a self-calibration function for controlling the gain, offset, and timing of the SCA in the DRS4 chip. With respect to the gain and offset calibrations, the reference voltage is generated by a DAC and then fed to the DRS4 chip. With respect to the timing, a clock generated by the FPGA is fed to the DRS4 chip. After calibration, the systematic timing jitter for a given chip is below 40 ps.

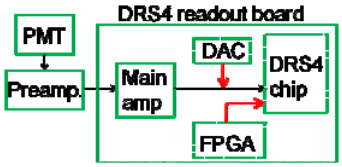

Figure 8. Self-calibration function for the DRS4 chip.

2.7 FPGA-based Gigabit Ethernet (SiTCP)

As described in section 2.1, the digitized waveform data and the monitor/control data are transmitted via Ethernet with only two devices: FPGA and Gigabit Ethernet transceiver (PHY). This simple composition is available on a hardware-based TCP processor, *SiTCP* [7]. The circuit size of SiTCP in the FPGA is ~3000 slices, which is enough small to allow implementation with user circuits on a single FPGA. In addition, the SiTCP has an advantage in that the throughputs in both directions can simultaneously reach the theoretical upper limits of Gigabit Ethernet.

3 Performance of Readout System

We have measured the performance of the DRS4 readout system (ver. 2) attached to a PMT. The preliminary results are shown here. Figure 9 shows a pulse shape of the high gain channel of the PMT signal with a gain of 2.4 × 10^5, which was measured with an LED and the DRS4 readout system at a sampling rate of 2 GS/s. The PMT signal having a width of 5 ns and a height corresponding to 7 photoelectrons was successfully digitized. Figure 10 shows a single photoelectron spectrum of the high gain channel of the PMT signal with a gain of 5 × 10^4, which was measured with an LED and the DRS4 readout system at a sampling rate of 2 GS/s. In the figure, a single photoelectron peak is clearly seen. The measurement of other performance parameters is ongoing.

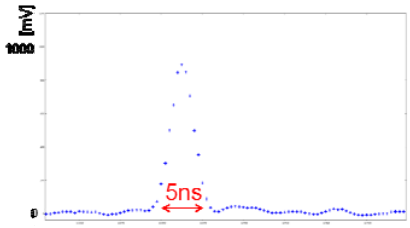

Figure 9. Pulse shape of the PMT signal measured with the DRS4 readout system at a sampling rate of 2 GS/s.

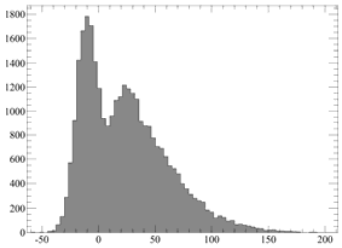

Figure 10. Single photoelectron spectrum of the PMT signal measured with the DRS4 readout system. The horizontal axis is in units of mV × ns.

4 Conclusion

We have developed a prototype 7-PMT cluster readout system for the next generation VHE gamma ray observatory, CTA. In the readout system named *Dragon*, a PMT signal is amplified, and its waveform is then digitized at a sampling rate of the order of GHz using an analog memory ASIC DRS4 that has 1,024 capacitors per channel. In the second prototype, four channels of the DRS4 chip are cascaded to obtain a sampling depth of 4,096. After a trigger is generated, the charges stored in the capacitors are digitized by an external slow sampling ADC and then transmitted via Gigabit Ethernet using the FPGA-based processor SiTCP. Using the prototype system attached to a PMT with a Cockcroft–Walton circuit, we successfully obtained a pulse shape of the signal of the PMT detecting an LED light at a sampling rate of 2 GS/s, and also a single photoelectron spectrum. Evaluation of the readout system's performance is ongoing, and a prototype with several PMT clusters and their readout boards will be constructed as the next step for the development of a full telescope camera.

Acknowledgement

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http://www.cta-observatory.org/?q=node/22

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