SLAC-TN-72-16
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November 1972

INSTRUCTION MANUAL
SPEAR P.W.C. CONTROLLER/INTERFACE (135-161)

I. Introduction

The SPEAR Proportional Wire Chamber (P.W.C.) Controller/Interface is an interface box between the P.W.C. electronics and the Sigma 5 computer. The system block diagram is shown in Figure 1.

The 320 wires from the P.W.C. feed into 40 8-channel chamber boards which upon arrival of the LOAD signal, load the data into the 8-bit parallel-in-serial-out shift registers. This data is then shifted out in serial to the controller's 32-bit serial-in-parallel-out shift register (32 bits at a time), under command from the computer. At the end of the data string is a fixed data word (programmable by switches inside the controller/interface box), which serves as a verification of proper operation. Through this box, the computer can also generate a system TEST PULSE which induces a small signal in all chamber wires, as a means of checking the P.W.C. electronics. To help system checkout, the controller/interface box can be switched to local control mode, under which the user can do most of the checking without the computer.

II. Description of Operation

The schematic of the SPEAR P.W.C. Controller/Interface is shown in Figure 2. There are basically two modes of operation: the computer control mode and the local control mode.

Computer Control Mode

Under this mode (switch in COMPUTER control position), the system works as follows:

a. A master trigger (NIM) from the machine initiates a properly timed load pulse (adjustable by the MT trimmer). This signal is sent along coax lines to the Chamber Amplifiers (135-137-03), where data on the wires is loaded into the parallel-in, serial-out registers. The load signal also loads the dummy registers in the controller with a pre-selected code. If no event trigger is received, the system continues to cycle, over-writing the old data each time.

b. When the fast logic (not part of this unit) decides an event has occured, it sends out an event trigger. This initiates a master inhibit, (timing adjustable by the ET trimmer), which stops further load pulses and after approximately 75 μsec delay, to allow time for high voltage noises to settle, initiates a fast clock (approximately 5 MHz). The clock shifts the first data word into a serial-in, parallel-out shift register in the controller.

c. During the shift process, the HLDR' goes low which tells the computer that no reading is allowed at this time. As soon as the shift is complete, HLDR' goes high and the computer can start its read cycle. The computer gives a low on the RE' line during the read cycle. After completion of the read cycle, RE' goes high again. This re-starts the fast clock and the cycle repeats for the second word, and so on for the third and fourth.

d. Just before the last read (computer keeps track of the count and the special code word at the end serves as sufficient verification) the RESET line goes high. Therefore the RESET.RE' condition signifies the completion of the whole event cycle. After approximately 20 μsec, to allow sufficient time for computer to finish its read cycle, the system resets itself and is ready to load data again.

e. The computer can initiate an automatic test by sending SE' low and RESET high. This initiates a test pulse which is sent to the 320 wires at the chamber. At the same time a load pulse and event trigger condition are produced. This enables the computer to read the data as before, hence provides a means of checking the electronics.

Local Control

When switch is in the LOCAL position there are two operating conditions, selectable through another switch, the LOCAL MANUAL/ LOCAL AUTO switch.

A. Manual

a. The TEST EVENT TRIG accepts a NIM pulse and generates a LOAD signal without any delay (in the computer mode, there is a delay). It also inhibits the next event until all shifts are completed or until the RESET button is pushed.

b. The SHIFT 32 button gives 32 shift counts from the clock every time it is pushed.

c. The LOAD button loads data (in this case, normally "0's") into all registers, except the dummy register, which will be loaded with the code word.

d. The COUNTER STATUS lights indicate the status of the shift count.

e. The RESET button resets the counter and removes the inhibit on the TEST EVENT TRIG and the system is ready for another test event.

B. Automatic

In the automatic mode the TEST EVENT TRIG in A.a. loads the registers, stops further loads and shifts all the registers (i.e., 352 bits). A switch is provided to exclude the code word (i.e., shift only 320 bits). When the shifts are complete, the load inhibit will be removed.

III. Controls, Displays, Input/Output Jacks

The following is a summary of controls, displays, input/ output jacks:

A. COMPUTER/LOCAL switch:

Selects either computer mode operation or local mode operation.

B. LOCAL AUTO/LOCAL MANUAL switch:

Selects either local manual or local automatic operations. It can be left at either state when A is in computer mode operation.

C. COUNT 352/COUNT 320 switch:
Includes (COUNT 352) or excludes (COUNT 320) the 32 bit data code word; only to be used when A is in LOCAL and B is in LOCAL AUTO.

D. LOAD pushbutton:
Generates a LOAD signal with each punch; only to be used when A is in LOCAL and B is in LOCAL MANUAL.

E. SHIFT 32 pushbutton:
Generates 32 shift clock signals with every push; only to be used when A is LOCAL and B is LOCAL MANUAL.

F. RESET button:
Resets controller/interface for a new cycle of operation under LOCAL mode.

G. TEST PULSE button:
Generates a test pulse to P.W.C. wires and associated load signal.

H. 4-bit COUNTER STATUS lights:
Indicates the number of 32-bit words shifted.

I. 32-bit word lights:
Indicates the contents of the 32-bit word that was last shifted into the controller/interface box and is ready for computer read.

J. +5V, -5V power status lights:
Lights when +5V, -5V power is on.

K. Input/Output jacks:

a. EVENT TRIG - accepts NIM signal (~25 nsec)from fast logic which signals an event has occured.

b. MASTER TRIG - accepts NIM signal (~25 nsec) from SPEAR, normally 780 nsec apart.

c. SHIFT OUT - sends shift clock (TTL logic level) to I/O card and chamber data boards.

d. SHIFT IN - receives shift clock (TTL logic level) from I/O card (for timing match).

e. DATA IN - receives serial data (TTL logic level) from I/O card and chamber electronics.

f. LOAD - sends load signal (TTL logic) to I/O card and chamber electronics.

g. TEST EVENT TRIG - to be used only in local test mode; receives NIM signal.

h. TEST PULSE - sends system TEST PULSE (variable amplitude) to P.W.C.; amplitude adjustable by TP trimmer.

i. EVENT OUT - TTL output to scaler counter for monitoring actual number of test event trigger inputs.

j. DATA - TTL level signal to scaler counter for monitoring serial data output.

k. DATA CODE - serial output (TTL level) from 32-bit dummy code register; to be connected to end of data chain.

l. 50-pin connector - communication between computer and controller/interface, where pins

1 - 32 - contains the 32-bit data
33 - 0 or ground
34 - power on/off status to computer
35 - computer/local status to computer
42 - HLDR' : 0 - shifting in progress
1 - no shift
46 - SE' (sense enable)
47 - RE' (read enable)
48 - Reset

IV. Signal Timing

Figure 3 shows the timing of the various signals involved.

V. Test Procedure

A. Local Manual Test

1. Connect cables to P.W.C. electronics, i.e., DATA CODE, SHIFT IN, SHIFT OUT, DATA IN and LOAD.
2. Switch positions in LOCAL, LOCAL MANUAL.
3. Connect DATA jack output to scaler counter, reset counter.
4. Push RESET.
5. Push TEST PULSE.
6. Push SHIFT 32.
7. Observe BØ through B31 lights: all should be "on".
8. Repeat 6 and 7 ten more times; on the nineth time, BØ through B31 should match the pre-selected code. BØ through B31 should be "off" at the end of the tenth time.
9. Observe scaler counter display; should read 320 + number of 1's in the pre-selected code word.
10. Push RESET, LOAD.
11. Repeat 6 through 8, except on 7 all lights should be "off".
12. Observe scaler counter display - reading should equal number of 1's in the pre-selected code word.

B. Local Automatic Test

1. Do A.1.
2. Connect trigger generator to TEST EVENT TRIG jack; leave trigger generator at manual.
3. Switch positions in LOCAL, LOCAL AUTO, COUNT 352.
4. Push RESET; reset scaler counter.
5. Push manual (trigger generator) once.
6. Observe COUNTER STATUS lights; should read 11.
7. Observe scaler counter reading; should be equal to number of 1's in pre-selected code word.
8. Switch to COUNT 320 position.
9. Repeat 5 through 7. COUNTER STATUS should read 10; scaler counter should read 0.

10. Optional test:
    a. set trigger generator to automatic
    b. connect EVENT OUT to another scaler counter
    c. reset and observe various readings.

C. Computer Control Test

1. Switch position in COMPUTER

2. Have computer generate command signals, read data and verify.

VI Acknowledgements

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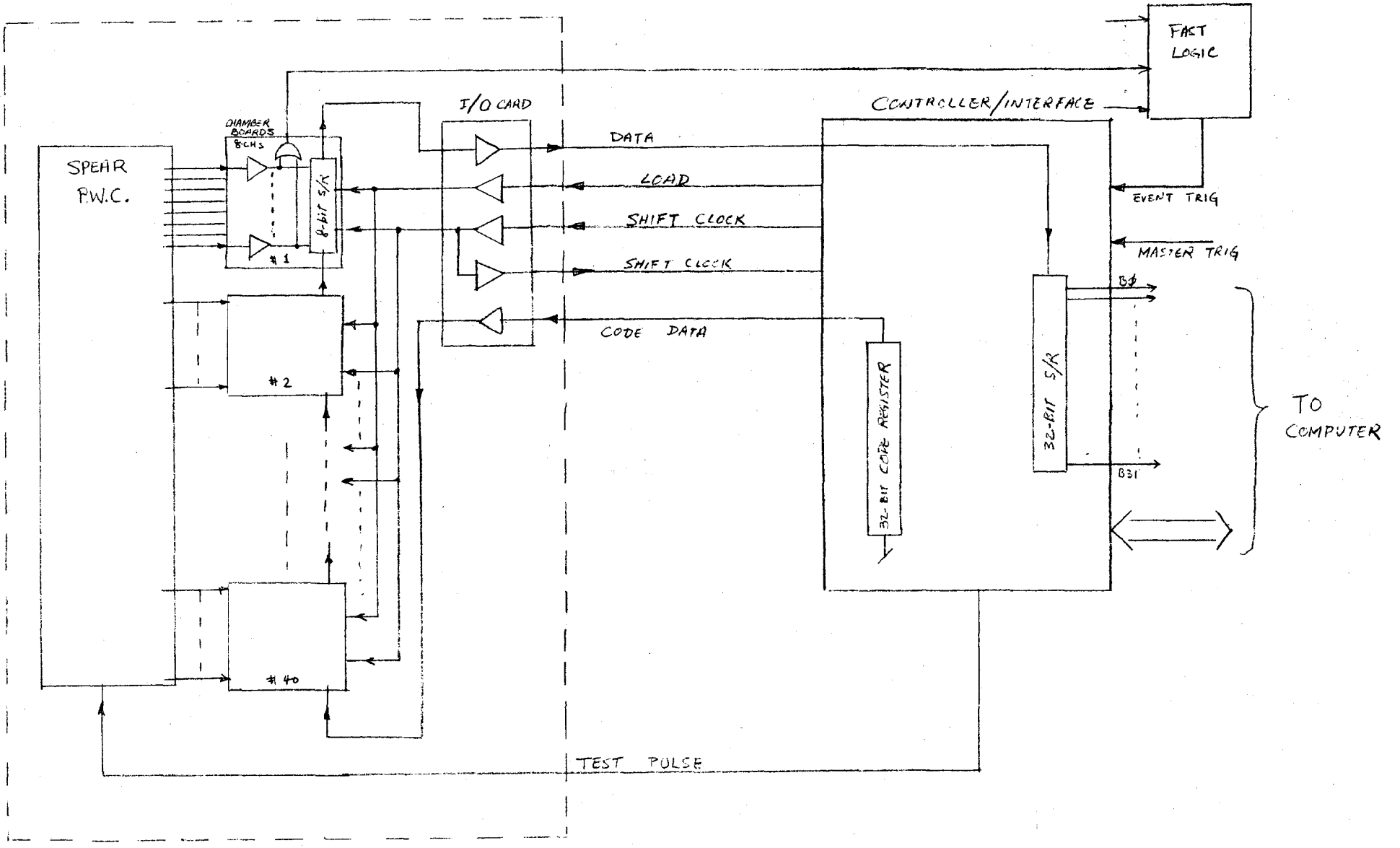

FIG. 1 SYSTEM BLOCK DIAGRAM

AC 11/6/92

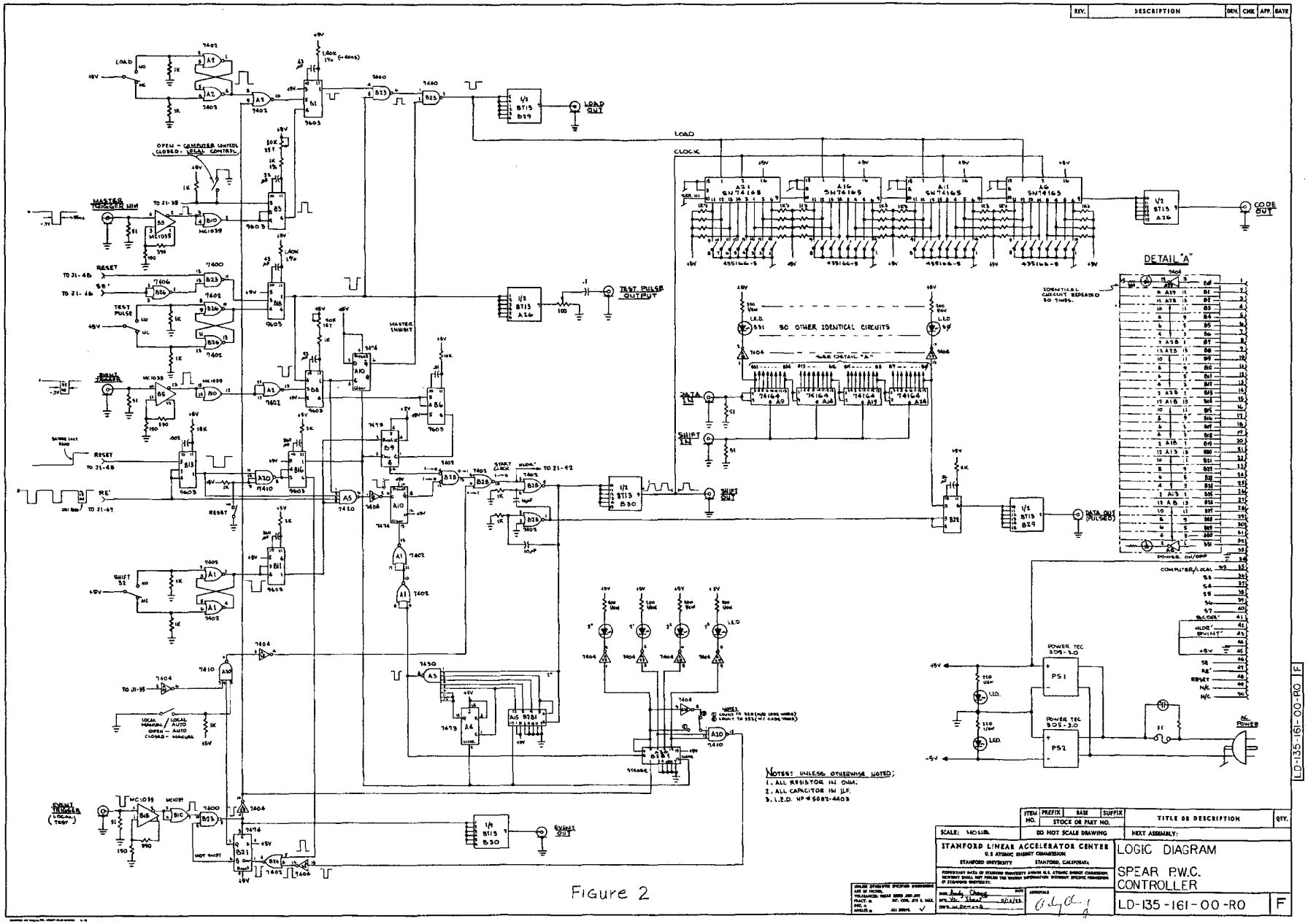

Figure 2

REV.	DESCRIPTION	DRN.	CHK.	APP.	DATE

ITEM NO.	PREFIX	BASE	SUFFIX	STOCK OR PART NO.	TITLE OR DESCRIPTION	QTY.

SCALE: NONE DO NOT SCALE DRAWING NEXT ASSEMBLY:

STANFORD LINEAR ACCELERATOR CENTER
U.S. ATOMIC ENERGY COMMISSION
STANFORD UNIVERSITY STANFORD, CALIFORNIA

LOGIC DIAGRAM
SPEAR P.W.C. CONTROLLER

LD-135-161-00-R0 F

LD-135-161-00-R0 F

FIGURE 3 TIMING DIAGRAM

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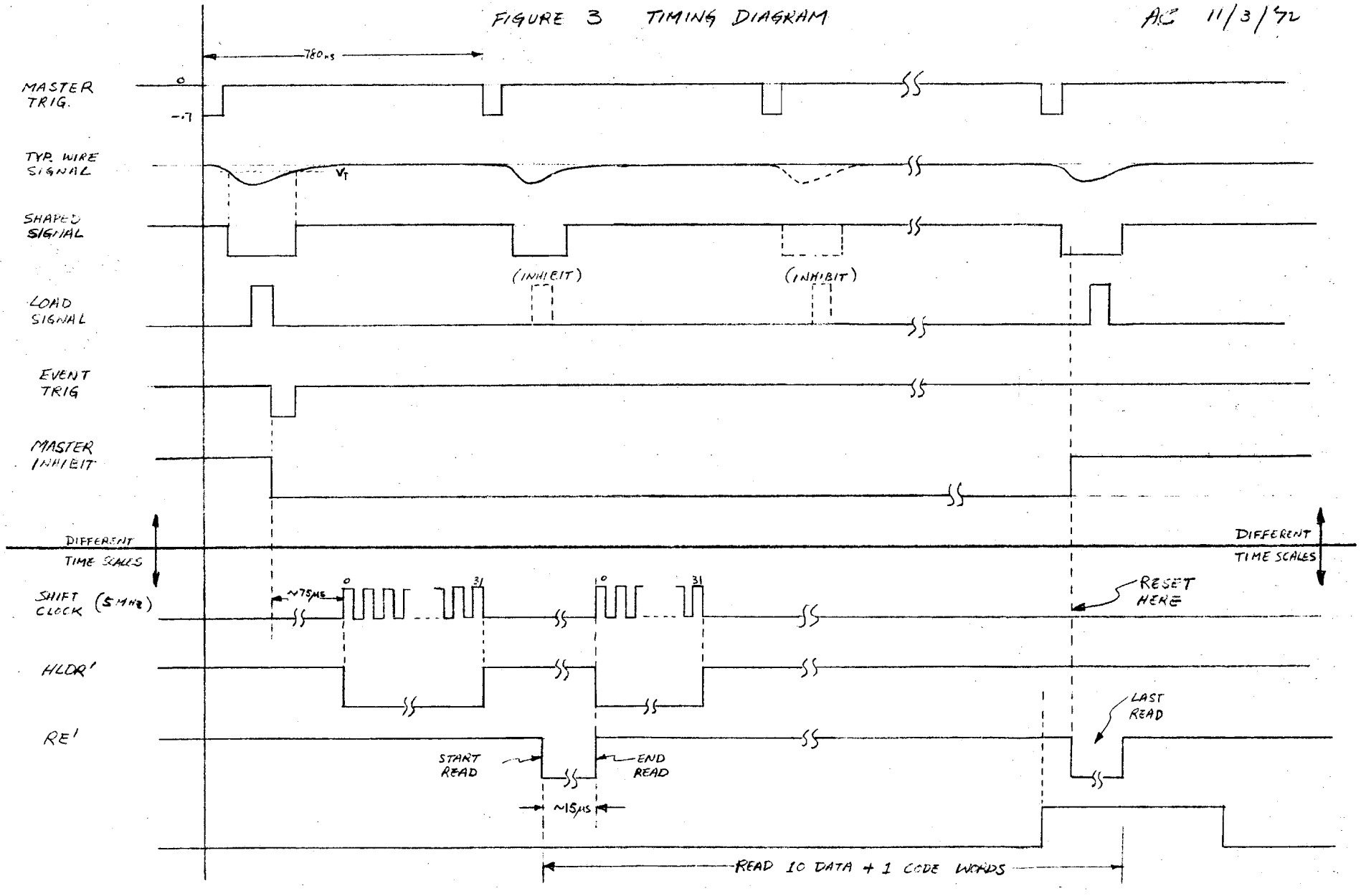
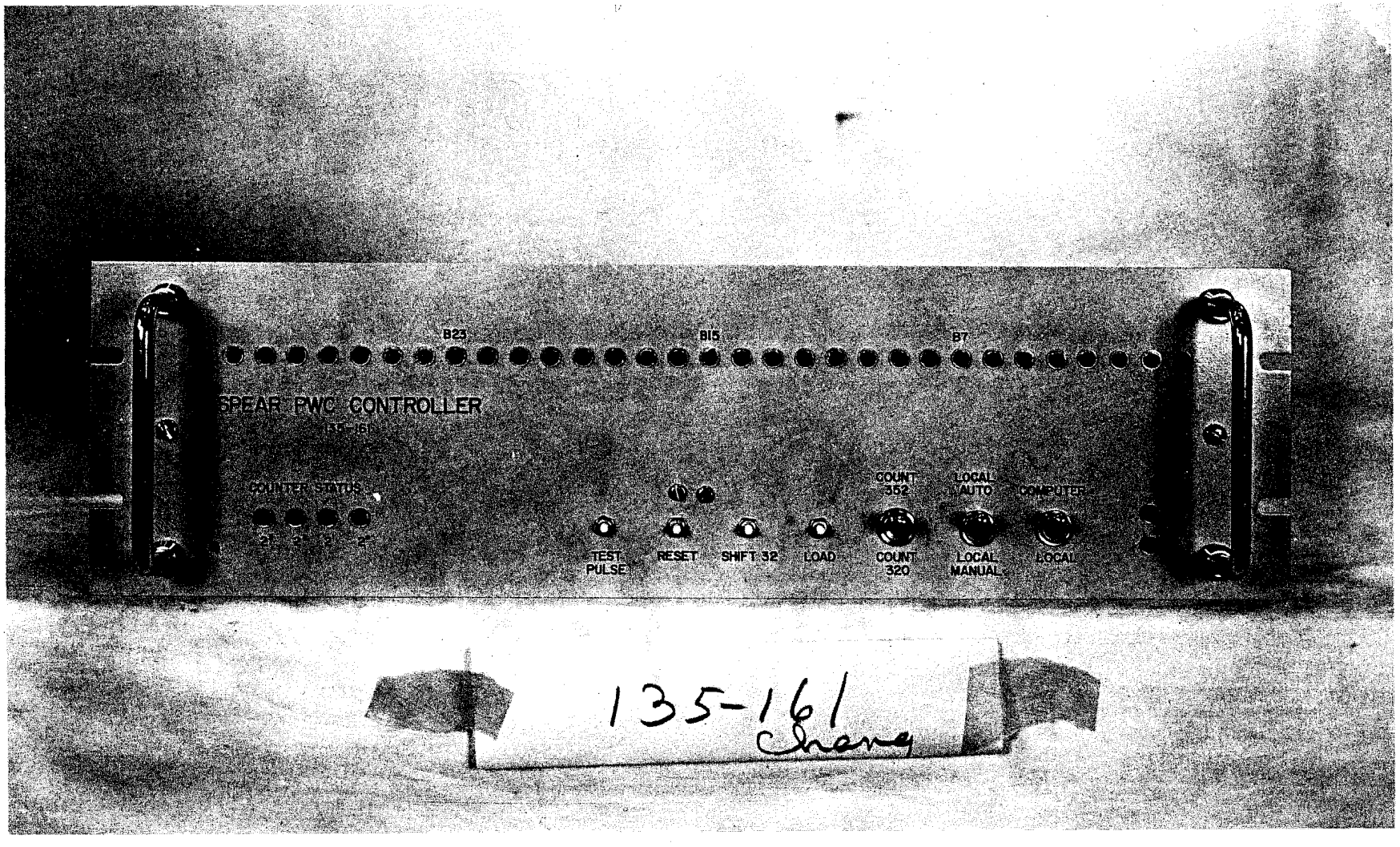
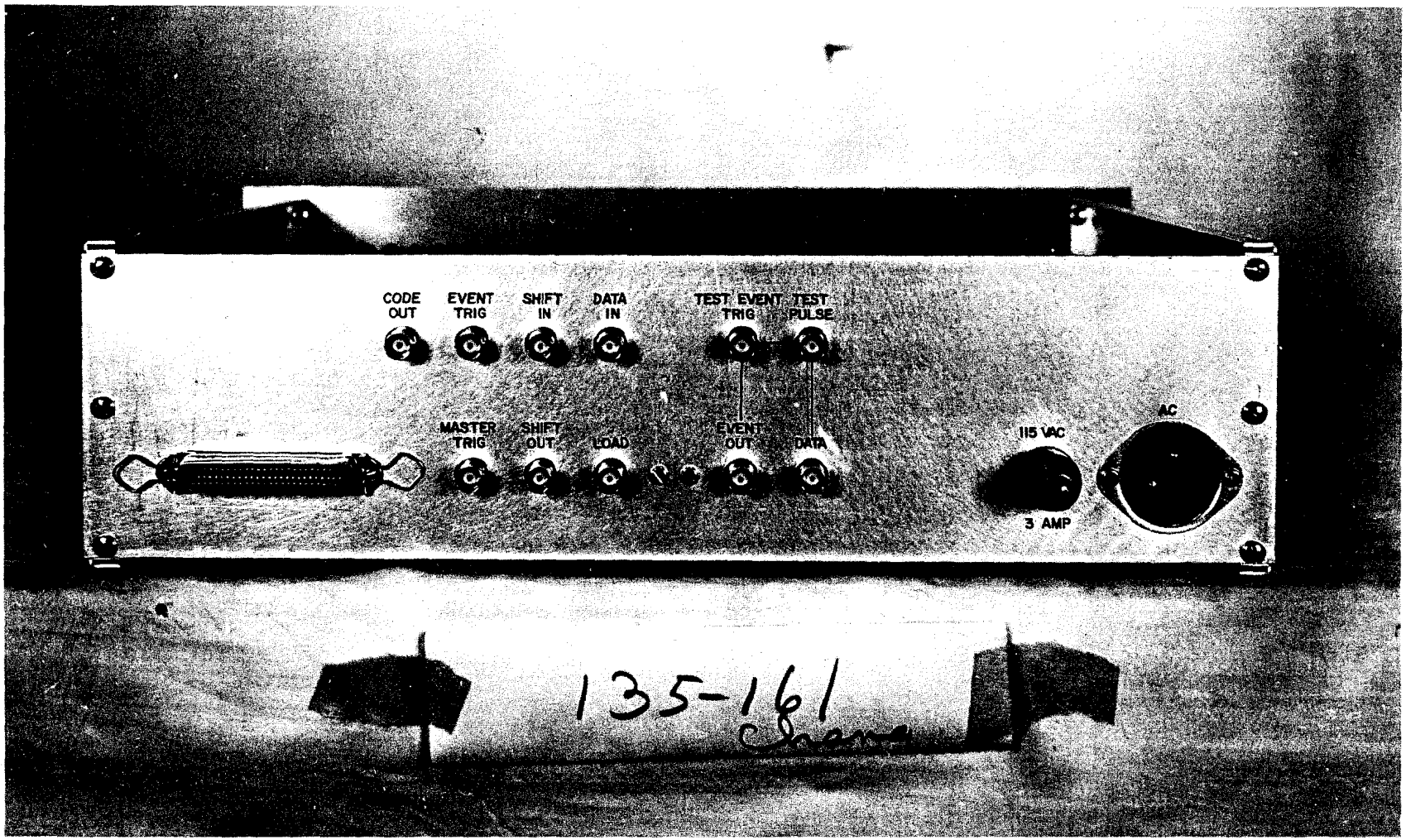



B23
B15
B7
SPEAR PWC CONTROLLER
135-161
COUNTER STATUS
2¹ 2² 2³ 2⁴
TEST PULSE
RESET
SHIFT 32
LOAD
COUNT 352
COUNT 320
LOCAL AUTO
LOCAL MANUAL
COMPUTER
LOCAL
135-161
Shaw


CODE OUT
EVENT TRIG
SHIFT IN
DATA IN
TEST EVENT TRIG
TEST PULSE
MASTER TRIG
SHIFT OUT
LOAD
EVENT OUT
DATA
115 VAC
3 AMP
AC
135-161