UNIVERSIDAD
POLITECNICA
DE VALENCIA

Novel Front-end Electronics for Time Projection Chamber Detectors

Eduardo José García García

Under the direction of Dr. Raúl Esteve Bosch

Universidad Politécnica de Valencia

June 2012

“Novel Front-end Electronics for Time Projection Chamber Detectors”

Este trabajo ha sido realizado en la Organización Europea para la Investigación Nuclear (CERN) y forma parte del proyecto de investigación Europeo para futuros aceleradores lineales (EUDET).

En física de partículas existen diferentes categorías de detectores de partículas. El diseño presentado esta centrado en un tipo particular de detector de trayectoria de partículas denominado TPC (Time Projection Chamber) que proporciona una imagen en tres dimensiones de las partículas eléctricamente cargadas que atraviesan su volumen gaseoso.

La tesis incluye un estudio de los objetivos para futuros detectores, resumiendo los parámetros que un sistema de adquisición de datos debe cumplir en esos casos. Además, estos requisitos son comparados con los actuales sistemas de lectura utilizados en diferentes detectores TPC. Se concluye que ninguno de los sistemas cumple las restrictivas condiciones. Algunos de los principales objetivos para futuros detectores TPC son un altísimo nivel de integración, incremento del número de canales, electrónica más rápida y muy baja potencia.

El principal inconveniente del estado del arte de los sistemas anteriores es la utilización de varios circuitos integrados en la cadena de adquisición. Este hecho hace imposible alcanzar el altísimo nivel de integración requerido para futuros detectores. Además, un aumento del número de canales y frecuencia de muestreo haría incrementar hasta valores no permitidos la potencia utilizada. Y en consecuencia, incrementar la refrigeración necesaria (en caso de ser posible).

Una de las novedades presentadas es la integración de toda la cadena de adquisición (filtros analógicos de entrada, conversor analógico-digital (ADC) y procesado de señal digital) en un único circuito integrado en tecnología de 130nm. Este chip es el primero que realiza esta altísima integración para detectores TPC.

Por otro lado, se presenta un análisis detallado de los filtros de procesado de señal. Los objetivos más importantes es la reducción de potencia de procesado y la mejora de ruido digital introducido.

Por último, se muestra el prototipo de 16 canales. Los resultados obtenidos con este circuito integrado han sido muy satisfactorios. El éxito de la integración ha sido cuantificado por medidas como el crosstalk del 0.3% y por la no existencia de ruido del circuito digital en el muestreo del ADC. Además, la potencia del circuito digital ha sido reducida al 28% respecto a su predecesor. Por último, una de las técnicas de reducción de potencia mas eficaces pare este tipo de detectores (power pulsing) ha sido demostrada con éxito. Reduciendo la potencia de 47.25mW/canal a 1.76mW/canal con un periodo de funcionamiento del 0.5%.

Dentro de las líneas futuras de investigación se encuentra el diseño de un circuito integrado de 64 canales basado en la topología demostrada en esta tesis.

“Novel Front-end Electronics for Time Projection Chamber Detectors”

This work has been carried out in the European Organization for Nuclear Research (CERN) and it was supported by the European Union as part of the research and development towards the European detector the (EUDET) project, specifically for the International Linear Collider (ILC).

In particle physics there are several different categories of particle detectors. The presented design is focused on a particular kind of tracking detector called Time Projection Chamber (TPC). The TPC provides a three dimensional image of electrically charged particles crossing a gaseous volume.

The thesis includes a study of the requirements for future TPC detectors summarizing the parameters that the front-end readout electronics must fulfill. In addition, these requirements are compared with respect to the readouts used in existing TPC detectors. It is concluded that none of the existing front-end readout designs fulfill the stringent requirements. The main requirements for future TPC detectors are high integration, an increased number of channels, faster electronics and very low power.

The principal disadvantage of existing readout systems is the utilization of several integrated circuits in the acquisition chain. Those systems cannot achieve the high integration needed for future detectors. In addition, the increase in the number of channels and sampling rate planned for future detectors would increase the power consumption in the existing systems above the acceptable values. In consequence, it would also increase the loading on the necessary cooling systems.

This thesis presents the integration of the whole acquisition chain (analog front-end filters, analog-to-digital converter (ADC) and digital signal processing) into a single integrated circuit in 130nm CMOS technology. This chip is the first that contains such a high integration level for TPC applications.

Another area of importance which has been researched is the detailed analysis of the digital processing filters, and these results are presented here. The most important objectives are the reduction of power consumption in the digital processing blocks and reduction of digital noise.

Finally, this thesis shows the 16-channel prototype which has provided very satisfactory test results. The integration success has been quantified by measuring the crosstalk (0.3 %) and the absence of digital noise in the ADC sampling. In addition, the digital power consumption has been reduced to 28 % of the preceding design. Moreover, the concept of one of the most important power reduction techniques, power pulsing, has been proven. The power has been reduced from 47.25mW/channel to 1.76mW/channel with a duty cycle of 0.5 %.

Future investigation lines will focus on the design of a 64-channel integrated circuit based on the topology proven in this thesis.

“Novel Front-end Electronics for Time Projection Chamber Detectors”

Aquest treball ha estat realitzat en l'Organització Europea per a la Investigació Nuclear (CERN) i forma part del projecte d'investigació Europeu per a futurs acceleradors lineals (EUDET).

En física de partícules existeixen diferents categories de detectors de partícules. El disseny presentat està centrat en un tipus particular de detector de trajectòria de partícules denominat TPC (Time Projection Chamber) que proporciona una imatge en tres dimensions de les partícules elèctricament carregades que travessen el seu volum gasós.

La tesi inclou un estudi dels objectius per a futurs detectors, resumint els paràmetres que un sistema d'adquisició de dades ha de complir en aquests casos. A més, aquests requisits són comparats amb els actuals sistemes de lectura utilitzats en diferents detectors TPC. Es conclou que cap dels sistemes compleix les restrictives condicions. Alguns dels principals objectius per a futurs detectors TPC són un altíssim nivell d'integració, increment del nombre de canals, electrònica més ràpida i molt baixa potència.

El principal inconvenient de l'estat de l'art dels sistemes anteriors és la utilització de diversos circuits integrats en la cadena d'adquisició. Aquest fet fa impossible aconseguir l'altíssim nivell d'integració requerit per a futurs detectors. A més, un augment del nombre de canals i freqüència de mostreig faria incrementar fins a valors no permesos la potència utilitzada. I en conseqüència, incrementar la refrigeració necessària (en cas de ser possible).

Una de les novetats presentades és la integració de tota la cadena d'adquisició (filtres analògics d'entrada, convertidor analògic-digital (ADC) i processament de senyal digital) en un únic circuit integrat en tecnologia de 130nm. Aquest xip és el primer que realitza aquesta altíssima integració per a detectors TPC.

D'altra banda, es presenta una anàlisi detallada dels filtres de processament de senyal. Els objectius més importants són la reducció de potència de processament i la millora de soroll digital introduït.

Finalment, es mostra el prototip de 16 canals. Els resultats obtinguts amb aquest circuit integrat han estat molt satisfactoris. L'èxit de la integració ha estat quantificat per mesures com el crosstalk del 0.3% i per la no existència de soroll del circuit digital en el mostreig de l’ADC. A més, la potència del circuit digital ha estat reduïda al 28% respecte al seu predecessor. Finalment, una de les tècniques de reducció de potència més eficaç per a aquest tipus de detectors (power pulsing) ha estat demostrada amb èxit. Reduint la potència de 47.25mW/canal a 1.76mW/canal amb un període de funcionament del 0.5%.

Dins de les línies futures d'investigació es troba el disseny d'un circuit integrat de 64 canals basat en la topologia demostrada en aquesta tesi.

Contents

Table of Figures

List of Tables

Preface

Introduction

The work presented in this thesis was carried out at PH-ESE-MIC group at the European Organization for Nuclear Research (CERN) ([CERN]) in Geneva, Switzerland. This research project has been supported by a Marie Curie Early Stage Research Training Fellowship of the European Community's Sixth Framework Programme under contract number (MEST-CT-2005-0200216 – Elacco).

CERN is the world's largest particle physics centre. Founded in 1954, the laboratory has become the foremost international collaboration in its field, exploring what matter is made of, and what forces hold it together. Matter does not decay into elementary particles under normal conditions in nature, and as such, energetic collisions of particles are needed to create them. These collisions are carried out in particle accelerators, which are the basic instruments in high energy physics (HEP). Once the elementary particles are created, the detectors task is to observe those elementary particles. There are many different kind of detectors, nevertheless this thesis is focused on only one type: Time Projection Chambers (TPCs).

A TPC is a particle detector that provides a 3-D picture of charged particles traversing its gaseous sensitive volume ([KNOLL]). This detector is commonly used in HEP for the 3-D reconstruction of the trajectories of charged particles, the measurement of their momenta and their identification through their ionization energy loss (dE/dx).

A TPC at a typical collider experiment comprises of a cylindrical volume surrounding the interaction point which is itself immersed in a large solenoid magnet. Electrically charged particles traversing the gas will leave behind the memory of their passage in the form of a long trace of ionized gas. The cylinder walls (called field cages) and central electrode of the TPC comprise a high voltage distribution chain. This allows the moving of the ionization trace at

constant velocity to either of the two end plates. The end plates are equipped with readout chambers which provide amplification of the electrical signal. These amplified signals are read by the readout electronics. The data coming from the readout electronics is then processed off-line providing a precise measurement of the location in the x and y coordinate; the z coordinate corresponds to the time hits are sampled on the readout pads.

TPCs have been used to study collisions in many experiments and have been at the heart of many important discoveries in the last 30 years. The first TPC was developed for the PEP Experiment ([PELLEG]) in the early 70's. Later on, in the 80's, large TPCs have been successfully employed at CERN in the main LEP Experiments (ALEPH and DELPHI). In the 90's the NA49 Experiment ([NA49]) proved that TPCs could also be successfully employed for tracking the many thousands of particle produced in the collisions of heavy-ions. Currently, the biggest TPC built is working at ALICE experiment ([ALICETPC]) in the Large Hadron Collider (LHC) ([LHC]).

In general HEP experiments require a large number of detector channels working at high frequencies. For instance, the ALICE TPC detector has more than 1/2 million channels working with a clock frequency of 10 MHz ([ALICETPC]). Moreover, future TPC designs aim at very high spatial resolution, requiring pad sizes of the order of a few square millimeters. In particular, the designs intended for the International Linear Collider (ILC) TPC ([ILC]), will have up to 1 million channels and will operate with frequencies up to 40 MHz. Besides leading to an increasing data rate, it has severe implications on cost (number of channels) real-estate and power consumption/cooling. As a result, higher density, higher number of channels, faster electronics, lower mass and lower power consumption will be required.

The main drawback of the current generation of TPC readout electronics is that the sensitive analog amplifier and filters are still kept separate from the ADC circuits and the high-speed digital processing. However this will not be possible if the aim is to reach such high integration density. A new achievement for HEP applications is a full integration of sensitive analog designs with high-speed digital processing. Furthermore there are key parameters to optimize such as flexibility, low power consumption and digital noise. All those requirements are fundamental to a promising front-end electronics solution for future TPCs.

The S-ALTRO is the novel front-end electronics introduced in this thesis which fulfill all the requirements mentioned. Implemented in an ASIC it embeds multi-purpose charge-amplifiers, analog-to-digital converters, digital signal processors and interface. Besides, it includes an improvement in power consumption, noise and flexibility with respect to its precedent front-end electronics.

Finally, an S-ALTRO prototype has been implemented with a simplified architecture to test the main concepts of full integration, low power consumption, low digital noise and filter flexibility.

Objectives

1.- Study of the state-of-the-art in TPC Front-End electronics.

Future TPCs present new challenges in the field of front-end electronics for HEP Experiments and requirements include - higher density, larger number of channels, faster electronics, lower mass and power consumption. A study of the requirements of future TPC detectors is needed to define the specifications of the corresponding readout electronics.

Moreover, a detailed review of the readout electronics of several TPCs built in the past is essential to actually verify that the requirements for future TPCs really demand new development with innovative solutions. Their different architectures and applications make it complicated to conduct a simple comparison between them. However, a study of the main features is presented. In many cases the advantages and disadvantages are dependent on the application.

The studies of future TPCs requirements and front-end electronics are the base for the novel front-end definition, the S-ALTRO.

2.- Definition of the novel front-end block diagram, S-ALTRO.

Once the future TPCs requirements and the state-of-the-art are clarified, the block diagram of the S-ALTRO chip is defined.

The S-ALTRO chip is a multi-purpose charge-amplifying, digitizing, processing and read-out chip. It is designed for TPCs, but in principal it is suitable for any application that needs to sample charge signals with a 10-bit dynamics and up to 40 MHz frequency. One S-ALTRO consists of 64 complete signal acquisition lines (channels) that are run in parallel.

The acquisition pipelines of all 64 S-ALTRO channels are identical. They comprise of several functional blocks that can be arranged in different ways to serve a wide range of applications. Each arrangement corresponds to a different acquisition mode.

This ASIC fulfills the requirements of very high integration, flexibility, low power consumption and good signal to noise ratio.

3.- Optimization/Investigation of the algorithms for low power consumption and low digital noise introduced.

As explained in the introduction, the power consumption and the digital noise introduced are the key parameters to optimize.

There are many design parameters that can be used to optimize the power consumption in a design at different levels: Architecture level, (Micro-)Architecture level and circuit level. The (Micro-)Architecture level defines the IC solution, being the custom design (Application-Specific Integrated Circuit, ASIC) the only suitable solution for this application. Finally, the efforts are focused on the optimization at the architecture level and the circuit level. The

architecture level tries to find optimum processing algorithms and techniques of power distribution, while the circuit level studies the effects in the design of the V_{DD} reduction.

The digital filters introduce noise into the system. There is always a trade-off between hardware resources and noise optimization. Detailed signal to noise analysis are performed in the filters.

4.- Mixed signal ASIC prototype implementation.

A prototype chip is implemented to demonstrate the main concepts of the S-ALTRO chip, for instance the integration of the analog sensitive amplifiers, ADCs and digital signal processing in a single ASIC. Moreover, the optimized digital filters are also included in the processing chain.

The S-ALTRO prototype is implemented in IBM 130nm technology.

5.- Measurements and analysis.

A test board is designed to characterize the main features of the S-ALTRO prototype. The tests are divided in three steps to isolate potential problems in the integration:

- Analog front-end + ADC + Digital interface: functional test of the analog front-end and the ADC (DSP bypassed).
- DSP: functional test of the DSP stand alone (no analog power).
- Full chain: functional test, feasibility of the integration, detailed power consumption analysis and power pulsing technique.

Thesis structure

The first chapter presents the future TPCs requirements. The chapter starts with a short introduction to the necessity of accelerators and detectors for the study of elementary particles. Later, a summary of detectors is presented focusing on the TPCs. This is followed by an introduction to TPC readout chambers, which are one crucial component to be taken into account for the design of front-end electronics. Finally, the future TPCs requirements are summarized and some conclusions are extracted.

The second chapter illustrates the different TPC readout electronics available in the market or in development/study. The differences among architectures and applications make complicated a simple comparison. However, a summary considering few basic categories of all of them is presented at the end of this chapter. This comparison concludes that a novel front-end electronics is needed and a basic description is provided.

The third chapter introduces the S-ALTRO architecture overview and the functionality of all its blocks: programmable charge sensitive shaping amplifier, analog-to-digital converter, ring buffer, multi-event buffer, baseline correction 1, digital shaper, baseline correction 2, 3D zero suppression, internal data formatter and interface.

The fourth chapter presents different optimizations of the baseline correction 1, digital shaper and baseline correction 2 filters introduced in chapter 3. These optimizations are in terms of power consumption, digital noise introduced and flexibility. The results are compared with its precedent front-end electronics (the ALTRO chip). In particular, this chapter presents an extensive study of different architectures for the digital shaper, which is one of the most important filters in the design due to its power consumption and area.

The fifth chapter describes the prototype implemented. The block diagram is slightly different to the one presented in chapter 3 in order to reduce the cost, the implementation time and testing time. Nevertheless, the main objectives are fulfilled. This chapter also describes the digital design layout flow and the S-ALTRO prototype integration.

The sixth chapter presents the prototype test board and the testing procedure. Moreover, the tests prove the functionality of the full prototype and the feasibility of the integration. Finally, this chapter details the power consumption per block and proves the power pulsing technique.

Finally, the seventh chapter summarizes the most important achievements and conclusions of this thesis. In addition, it describes the future steps to complete the implementation of the S-ALTRO chip.

Acknowledgments

In the first place I want to thank Raúl Esteve and Luciano Musa, without them it would never have been possible to present this work. They have supported me from the first moment, and that cannot be overlooked.

The S-ALTRO project started in 2005 with the design of its first block by Gerd Trampitsch. However, I started on this project in September 2007. At that time, Hugo França-Santos had been working in the ADC block for the last two years and was about to start the ADC layout. At the same time than me, Christian Patauner joined to the S-ALTRO team to work on a data compression block, which posteriori was moved to an external FPGA. Around the first quarter of 2008, Paul Aspell joined the project as implementation project leader. Later, in July 2008 Massimiliano de Gaspari joined to the team to work, initially, on the integration and technology convergergency of the different blocks and, afterward, on the test board design and test measurements. In addition, other people collaborated at different phases of the project, for instance Magnus Mager and Attiq Rehman helped in the specification phase and Sandro Bonaccini assisted me with the use of the Cadence digital design tools.

I would like to thank all of them for the amazing experience. Special thanks to Massimiliano de Gaspari , the person with whom I was collaborating the most, and with which I shared many different moments over the course of the project: stressful, relaxed, worrying, humorous...

I want to thank to Marie Curie program for giving me the extraordinary opportunity to be part of this project and for supporting me in my academic formation over those 33 months. Equally,

I cannot forget the help of Taylan Akdogan, from Boğaziçi University, and Lucie Linssen for her support in the last 6 months of the project giving me the possibility of continuing at CERN.

Thanks to my friends from all around the world, colleagues from CERN, colleagues from Agilent, volleyball team mates, for all the good times shared along the way. I consider those moments as an essential contribution to the work presented in this thesis. Special thanks to John Hefferman and Paul Harwood for their help.

Finally, but no less importantly I would like to thank my family and my girlfriend. They were always there, with good advice, supporting me at all times and encouraging me to continue all along the way. I feel very lucky to have you all around me.

Chapter 1 Introduction

1.1 Introduction to High Energy Physics

Everything in the tangible world is built of matter. Particle physics is the part of physics which focuses on the study of the basic elements of mater, and the interactions between those elements. These elementary particles do not occur under normal circumstances in nature, and as such, energetic collisions of particles are needed to create them. This task is done in the particle accelerators, which are the basic instrument in high energy physics (HEP). Once the elementary particles are created, the instruments in charge of observing those elementary particles are the detectors (explained in the next section).

A particle accelerator uses electric fields to push ions or charged subatomic particles to near the speed of light and magnetic fields to contain/drive them through the accelerator. The main objective of an accelerator is to provide particle collisions at the points where the detectors are placed. This gives the physicists the opportunity to study the behavior of the elementary particles and their interactions. There are two basic types of accelerators:

- Linear accelerators: the particles are accelerated in a straight line with a target of interest at one end. Alternatively, they can be used to provide an initial low energy bunch of particles with the objective of being injected into circular accelerators.

- Circular accelerators: the particles move in a circle until they reach sufficient energy to collide. Magnetic fields are used to bend the particles. The most important advantage of circular accelerators over linear accelerators is that the ring topology allows continuous acceleration.

Nowadays, the particle physics community is recording the data of the biggest accelerator in the world, Large Hadron Collider (LHC) ([LHC]) and setting the features of the future International

Linear Collider (ILC) ([ILC]) and Compact Linear Collider (CLIC) ([CLIC]), which will complement the LHC having more precise measurements of the properties of the newly found particles.

1.2 Particle detectors

A particle detector detects, tracks, and/or identifies high-energy particles. Detectors designed for modern accelerators are huge, both in size and in cost. There are different kinds of detectors, but many of them have some similarities in the basic functions ([SPIELER]), see Figure 1.1.

The sensor converts the energy deposited/induced by a particle (or photon) to an electrical signal. The signal charge can be quite small, therefore it must be amplified. Usually, the preamplifier is configured as an integrator, which converts the narrow current pulse from the sensor into a step impulse with a long decay time. In HEP detectors the primary function of the pulse shaper is to improve the signal to noise ratio. However, the pulse shape should be compatible with the digitizer. Analog-to-digital conversion translates continuously varying amplitude to discrete steps, which correspond to a unique output bit pattern. Finally, the digital information is ready for subsequent storage and analysis.

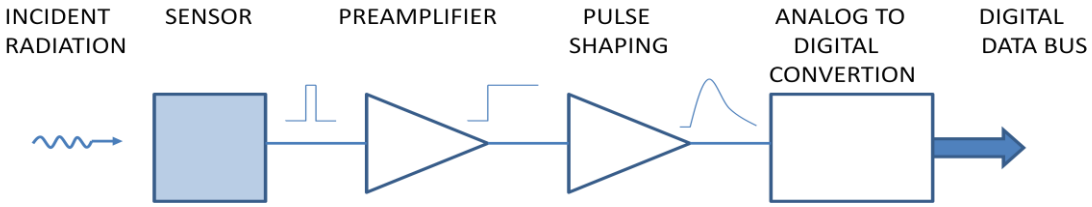


Figure 1.1 Basic detector functions

The detectors are structured in different layers, which are focused on a particular task. The location of the detectors layers depends on the purposes, capabilities and life time of the particles. This collection of detectors is often called “experiment” and is designed by a collaboration of different research centers. Figure 1.2 shows the different layers in a typical detector and the life time of some particles.

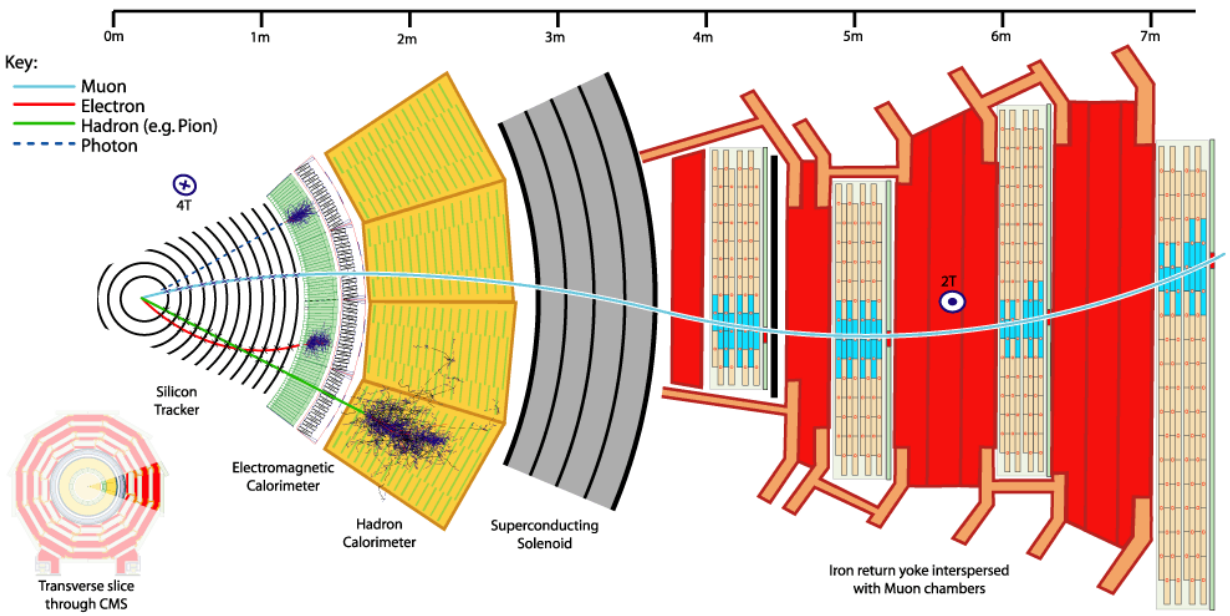


Figure 1.2 Layers in a typical detector

There are three important categories of sub-detector, for more details ([KNOLL]):

- **Tracking devices**: reconstruct the tracks of electrically charged particles through the trails they leave by ionizing matter. These devices are immersed in a large magnet field, which curves trajectory of the particles. The measure of that curvature is used to calculate the momenta of the particles. In current tracking systems the electrical signal produced in the detectors are recorded as computer data and off-line analysis are performed to reconstruct the tracks recorded.

  The main techniques use to build tracking detectors are:

  - gaseous chamber, where the ionizing matter is a gas and the ions and electrons are collected on electrodes. A representative example is the TPC detector explained in detail in the next section.

  - semiconductor detectors, where the particle creates electrons and holes as it passes through a reverse-biased semiconductor. The devices are subdivided into strips or pixels.

- **Calorimeters:** measure the energy of the particles by stopping or absorbing them and measuring the amount of energy released. There are two main types of calorimeters: electromagnetic (ECAL) and hadronic (HCAL). Different materials are used depending on which type of particle they are stopping. Calorimeters provide the main way to identify neutral particles such as photons or neutrons revealed by the energy they leave in the calorimeters.

- **Particle identification detectors:** identify the type of particle using one of the various techniques. Some examples are:

    - Cherenkov radiation: charge particles traversing a medium above certain velocity emit photons at a specific angle that depends on the velocity.

    - Energy loss dE/dx: a charged particle loses energy in matter by ionization at a rate determined in part by its velocity. The energy loss per unit distance is typically called dE/dx.

    - Time of flight: determines the charged particle velocity by measuring the time required to travel from the interaction point to the time of flight detector, or between two detectors.

  Combining the momentum measurement from the tracking devices and the particle velocity from one of these methods, the mass of the particle can be determinate. Consequently, the mass can be used to identify the particle.

1.3 TPC working principle

A TPC is a particle detector that provides a 3-D picture of charged particles traversing its gaseous sensitive volume. This detector is commonly used in HEP for the 3-D reconstruction of the trajectory of charged particles, the measurement of their momenta and their identification through their ionization energy loss (dE/dx).

A TPC at a typical collider experiment comprises a cylindrical volume surrounding the interaction point and immersed in a large solenoid magnet, see Figure 1.3. Electrically charged particles traversing the gas will leave behind the memory of their passage in the form of a long trace of ionized gas. The cylinder walls, called field cages, and central electrode of the TPC comprise a high voltage distribution chain. This allows moving the ionization trace at constant velocity to either of the two end plates. The end plates are equipped with readout chambers (explained in detail in the next section), which provide an amplification of the electrical signal. These amplified signals are read by the front-end electronics. The chapter 2 explains in detail several front-end electronics. Finally, the data coming from the front-end electronics is processed off-line providing a precise measurement of the location in the x and y coordinate; the z coordinate correspond to the time hits are sampled on the readout pads.

The most desired attributes in a TPC are momentum resolution, dE/dx resolution and two-track resolution.

- Momentum resolution: The momentum of a track can be determined by fitting through the points along the track. The radius of the curvature and the emission angles of the track at the interaction point are used to calculate the momentum.

- dE/dx resolution: The charge deposited in the clusters is used to obtain dE/dx information over the length of the track, which combined with the momentum measurement allows the identification of the particle
- Two-track resolution: The minimum separation of pairs neighbor tracks determinate the accuracy of the detector in high track density environments.

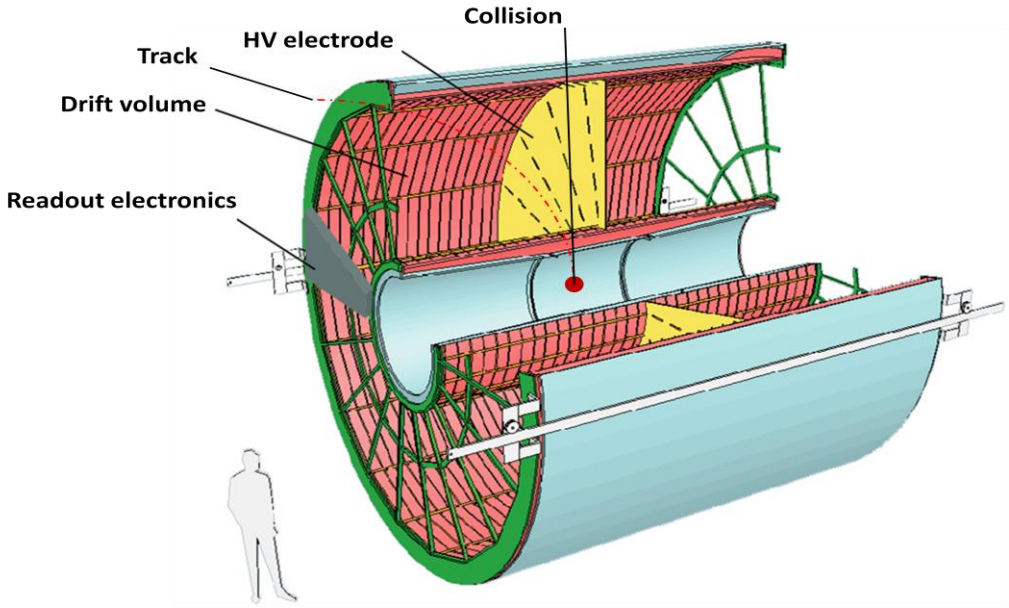


Figure 1.3 TPC structure

A summary of the parameters to be considered in a TPC could be: magnetic field, drift volume, electric drift field, drift velocity, maximum drift time, readout chambers, gain, pad size, number of channels, dynamic range, beam pulse duration, beam repetition rate, occupancy, material budget and trigger. The section 1.5.3 will present the values for these parameters in one current and some future TPC detectors.

1.3.1 Readout chambers

The HEP community is continually investigating different methods for obtaining large, stable and proportional gains in gaseous detectors.

The invention of the Multi-Wire Proportional Chamber (MWPC) in 1960 by Georges Charpark was a big step in the readout chamber evolution. However, more recently two different approaches seem promising for the future gaseous detectors. These are MicroMEsh GAseous Structure (MICROMEGAS) invented in 1995 by Yannis Giomataris and Georges Charpark; and Gas Electron Multiplier (GEM) invented in 1997 by Fabio Sauli.

This section explains the different concepts of readout chambers.

- **MWPC:**

The MWPC consists of a pad plane and three wire planes (see Figure 1.4).

Drifting electrons originating from the primary ionization by themselves do not induce a sufficiently large signal in the readout pads. The necessary signal amplification is provided by avalanche creation in the vicinity of the anode wires. As shown in the Figure 1.4, the induced charge from the avalanche is shared over several adjacent pads (2-3).

The outermost wire plane is the gating grid. This grid is a shutter to control the entry of electrons from the TPC drift volume into the readout chambers and it also blocks positive ions produced in the readout chamber. Therefore, positive ions are kept from entering the drift volume, where would distort the drift field. The positive ions are too slow to escape during the open period and get captured during the closed period. The switching of the potential of the gating grid from closed to open mode is controlled by the experiment trigger(s).

The two disadvantages of the MWPC are:

- Long peaking time (ballistic deficit): limit the rate capability of the detector. A compromise between pulse-width and charge measurement accuracy is necessary.

- Slow mobility of the ions (1/t tails): the ions mobility is several orders of magnitude lower than the electrons. Consequently, the current signal induced in the pads is characterized by a fast rise time (few ps) due to the electrons and a slow decay (few μs) due to the ions. This perturbs subsequent pulses.

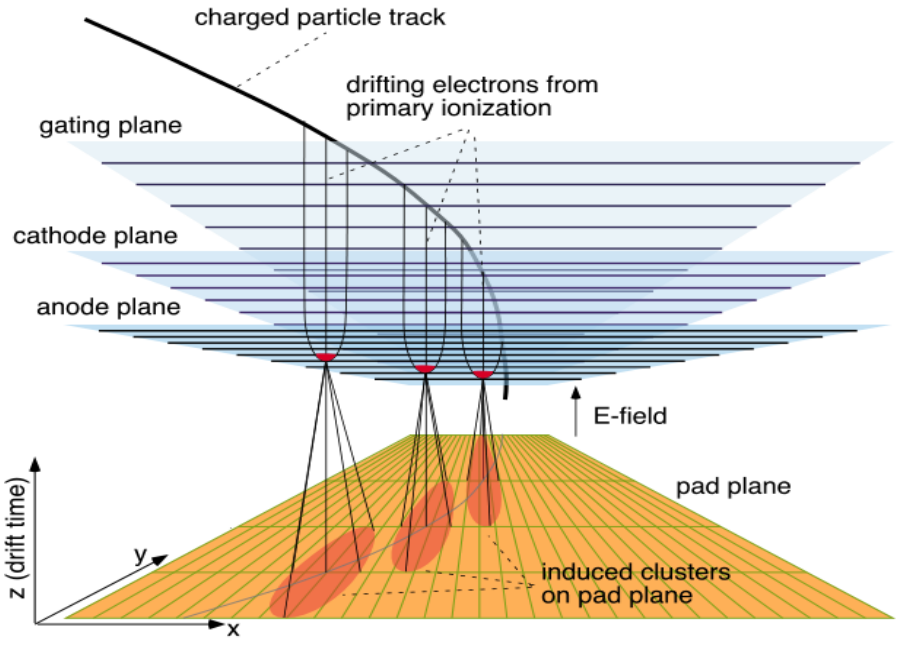


Figure 1.4 The gating grid (cathode and anode wires are in the readout chambers)

- **MICROMEGAS** ([GIOMAT])**:**

In this readout chamber the gas volume is separated by thin micromesh in two regions, one where the conversion and drift of the ionization electrons occurs and one, 50-100 μm thick, where the amplification takes place (see Figure 1.5).

In the amplification region, a very high field (40 to 70 kV/cm) is created by applying a voltage of few hundred volts between the mesh and the anode plane, which collects the charge of the avalanche. The anode can be segmented into strips or pads. The authors have demonstrated very high gain and rate capabilities using gaps in the range of 50 to 100 μm (realized by stretching a thin metal micro-mesh electrode parallel to a read-out plane). This result comes from the special properties of electron avalanches in very high electric fields.

The advantages of MICROMEGAS follow from the smallness of the amplification gap and the particular configuration of the electric field on the two sides of the mesh, itself depending on the mesh pitch. The small size of the gap and, consequently, of the avalanche creates an electron signal of few nanoseconds and an ion signal of usually less than 50-100 ns, for most of the gas mixtures. Starting from the avalanche concentrated in the last few microns of the gap, the ions flow back to the mesh in the almost uniform amplification field. This avoids the ballistic deficit and the 1/t tails present in the wire chambers.

The major practical inconvenience lies in the necessity of stretching and maintaining parallel meshes with very good accuracy. The presence of strong electrostatic forces adds to the problem, particularly for large sizes. However, MICROMEGAS has reached the statute of a mature technology.

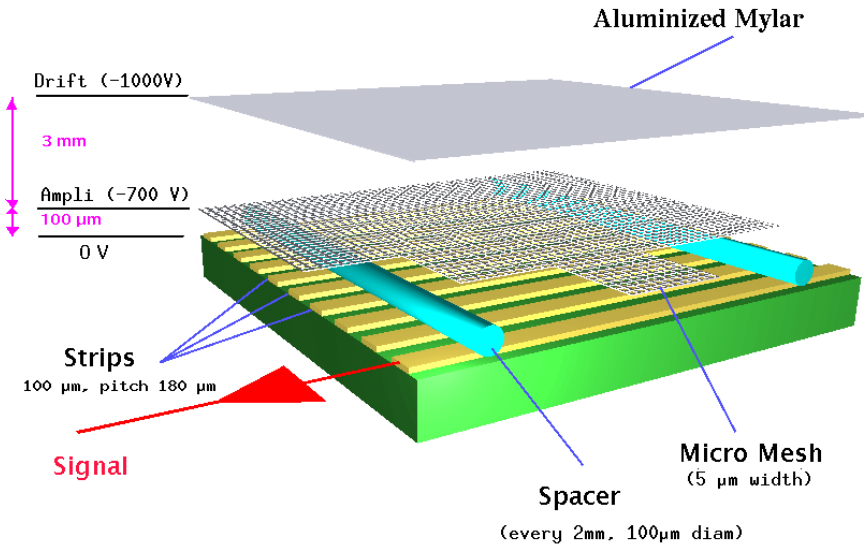


Figure 1.5 MICROMEGAS scheme

- **GEM** ([SAULI]):

GEM seems a promising solution due to his simplicity and high field advantages. The basic element of the GEM detector is a thin sheet of plastic coated with metal on both sides and chemically pierced by a regular array of holes a fraction of a millimeter across and apart (see Figure 1.6).

Applying a voltage, about 500 V on 50 microns across the GEM conducting layers, the resulting high electric field in the holes makes an avalanche of ions and electrons pairs (see Figure 1.7). Finally, the electrons are collected by a suitable device, such as a micro-strip gas chamber ([OED]).

Compared with the traditional MWPC, the new generation of TPCs based on GEM detector has much higher track resolution and very low ion feedback. The traditional MWPC is commonly implemented with a gating grid to provide lower ion feedback. The fact that GEM detectors do not need a gating grid, which requires an appropriate trigger signal for opening, makes them suitable for implementing continuously sensitive detectors.

Several groups are currently investigating GEM solutions, looking at different configurations, geometries, operating conditions, gas filling, etc. A lot of progress has been achieved, especially regarding the suppression of the ion feedback.

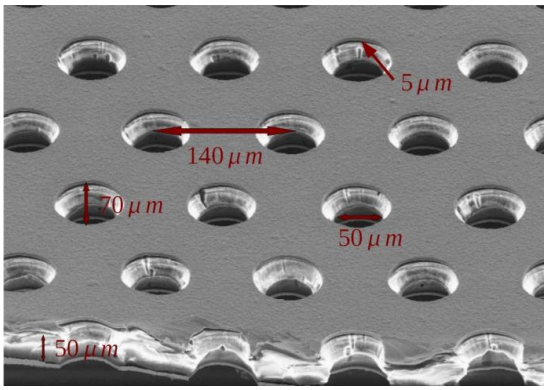


Figure 1.6 GEM arrays of sub-millimeter holes

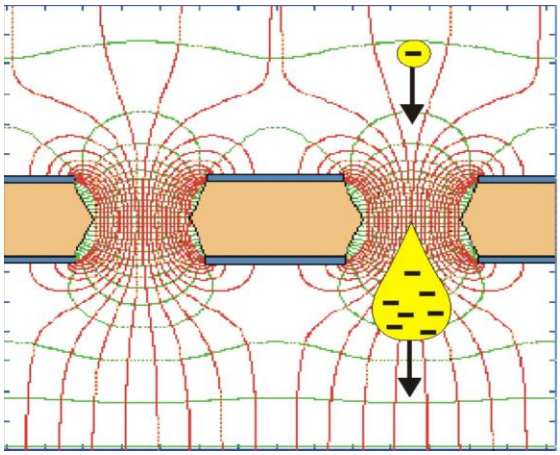


Figure 1.7 Field regions and avalanche of the GEM device

1.4 Future TPCs requirements

TPCs are being considered as main tracking detector in three main new accelerators facilities: the International Linear Collider (ILC), the Compact Linear Collider (CLIC) and the Facility for Antiproton and Ion Research (FAIR).

There are many similarities between the ILC ([ILC]) and the CLIC ([CLIC]). At the moment, they even share part of their R&D. Finally, only one of these accelerators will be built in the future.

On the contrary, FAIR has proposed a novel concept. A TPC with GEM readout chambers and continuously sensitive TPC has been proposed for the inner tracker of PANDA (FAIR detector).

1.4.1 Design parameters

TABLE 1-1 summarizes the main requirements for future TPCs with respect to the ALICE TPC ([ALICETPC]). The ALICE TPC can be considered as the readout electronics state-of-the-art due to its comparable requirements and its successful performance.

TABLE 1-1 TPC design parameters

	ILC [1]	CLIC [1]	FAIR (PANDA)	LHC (ALICE)
Drift volume (m^3)	40		0.7	90
Drift field (V/cm)	200		400	400
Magnetic field (T)	3.5		2	0.5
Drift velocity (cm/μs)	5 – 10		2.7	2.6
Max drift time (μs)	46		56	92
Longitude cluster width (ns)	100 – 400		60 - ?	124 – 400
Readout chamber	GEM, MICROMEGAS		GEM	MWPC
Gain (avalanche region)	~ 10^3		~ 2-5 x 10^3	~ 10^4
Pad size (mm^2)	1 x 5		2 x 2	4 x 7.5
Number of channels	1 x 10^6		0.8 x 10^5	5.7 x 10^5
Dynamic range	8-10 bits		8 bits	10 bits
Sampling rate	40-10 MHz [2]		100MHz	10MHz
Beam pulse duration (ns)	10^6	156 – 177	continuous	continuous
Beam repetition rate (Hz)	5	50	-	-
Trigger/event rate (Hz)	5	50	20M	1k
Occupancy	< 0.2 %	< 0.2 %	2% - 8%	< 10%
Trigger	beam pulse		none	event (collision)

[1] Design parameter with standard electronics. A new concept (CMOS Pixel readout) is under development.

[2] R&D phase required 40MHz sampling rate. However, the cluster size shows that it can run at 10MHz in standard operation.

1.5 Conclusions

TPCs for future experiments aim at very high spatial resolution requiring pad sizes of the order of few square millimeters (see TABLE 1-1). Therefore, the number of channels per area will increase significantly with respect to the ALICE TPC. Moreover, the R&D phase requires higher sampling. Both factors lead to a major increase in the power consumption. There are two approaches to meet this requirement:

- Implement low power techniques in the readout chip. This is valid for any of the TPCs presented in the last section.

- Use power pulsing technique. As shown in TABLE 1-1, the ILC TPC will have a beam repetition rate of 5Hz and beam pulse duration of 1ms. This corresponds to a beam duty cycle of 0.5%. Therefore, the power pulsing is an efficient technique to achieve very low power consumptions. This technique can reduce even more the power consumption in the CLIC TPC. Unfortunately power pulsing cannot be applied to PANDA due to its continuous acquisition.

Moreover, other important design criteria are the noise introduced by the electronics, which will contribute to the detector spatial resolution, the physical size of the circuit and the versatility to cover a broad range of applications.

In conclusion, these requirements call for highly integrated low-power front-end electronics and represent a significant challenge in the design of a novel front-end electronics.

Chapter 2 TPC Front-end Electronics State-of-the-art

2.1 Introduction

This chapter reviews several TPC readout electronics and proves that none of the current or in development front-end electronics meet the requirements presented in chapter 1. The readout electronics are compared in terms of integration, channels per chip, events rate, power consumption, data reduction, radiation hardness and technology.

The status of the readout electronics can vary from 'Installed', 'Prototyped' or 'In study'. TABLE 2.1 shows the list of readouts reviewed.

TABLE 2-1 TPC readout electronics and status

Front-End electronics	TPC	Status
Cold JFET preamp + FPGA	MicroBooNE	Installed
AFTER + FPGA	T2K	Installed
TimePix	ILC/CLIC	In study
ASDQ + TDC + FPGA	ILC/CLIC	In study
PASA + ALTRO	ALICE	Installed
S-ALTRO	ILC/CLIC, PANDA	Prototyped

Finally, a first outline of a possible front-end solution is presented. The novel front-end electronics for TPC detectors is an evolution of the ALICE TPC front-end electronics. Although it inherits its main features, higher integration, lower power consumption, larger flexibility and further functionality are included. This architecture meets all the requirements presented in the first chapter.

2.2 Readout Electronics

The purpose of the readout electronics is to acquire the detector data from the readout chambers, do the first signal processing and transfer it outside the detector. The readout electronics can be very different depending on the application, although some common issues exist to take into account as: signal-to-noise ratio, power consumption, integration, data volume and radiation hardness.

- Signal-to-noise ratio: one of the first blocks in any front-end electronics is the pulse shaper, which has as primary function the improvement of the signal to noise ratio. The ideal pulse shape for signal-to-noise ratio is the cusp which is unfeasible with analog electronics. However a trade-off between signal-to-noise ratio and feasibility is the semi-Gaussian function widely used in HEP frontend electronics.

- Power consumption: HEP experiments have huge amount of channels working with frequencies of tenth of Mhz. Power dissipation is an important property of a design that affects feasibility, cost and reliability. On top of that, power consumption is close related with the front-end integration capabilities and cooling systems requirements.

- Integration: the increase of number of channels per area for future detectors makes highly integrated front-end electronics more and more necessary.

- Data volume: the enormous amount of data generated in the detectors requires on-line data compression before shipping the data off detector. The most popular technique in HEP is the zero suppression, although Huffman coding and dynamic decimation are other very interesting techniques.

- Radiation hardness: the radiation environment is different for each experiment, depending on the collisions system (e-e, p-p, N-N), energy, and interaction rate. This has to be simulated carefully for each experiment and for the location of the different detectors.

2.2.1 MicroBooNE Readout Electronics

The Micro Booster Neutron Experiment (MicroBooNE) is located at Fermilab, USA. This experiment will build and operate a large, approximately 100-ton, liquid Argon Time Projection Chamber (LArTPC) ([LArTPC]). The present LArTPC has 2.5m drift at 500V/cm with three readout wire planes: 2 induction planes and 1 collection plane. The number of channels is approximately 10,000.

Figure 2.1 shows the block diagram of the MicroBooNE TPC readout electronics. In this detector the electrical signals in the readout chambers are pre-amplified based on “cold” JFET preamplifiers. These JFET preamplifiers are placed inside the cryostat where the cold temperature (≈120K) of the gas allow the amplifiers to operate with a signal-to-noise that is a factor of 3 better than at room temperature.

The signals coming from the JFET amplifiers are driven through cold twisted pair cables to a distance between 2.5-3.5 meters. At that point, an intermediate amplifier line drives the signals through approximately 20-30 meters of room temperature shielded twisted pair cables. Finally, it is place the TPC readout board which contains 12 bits multichannel ADC digitizing individually at 16MHz and a FPGA carrying out all the digital signal processing.

Two techniques of data reduction are implemented in the FPGA: lossless data reduction (Huffman coding) and lossy data reduction (Dynamic decimation).

It is important to emphasize that this readout can be used only when the readout board plan to be installed far from the detector. This is not the case for the future TPCs.

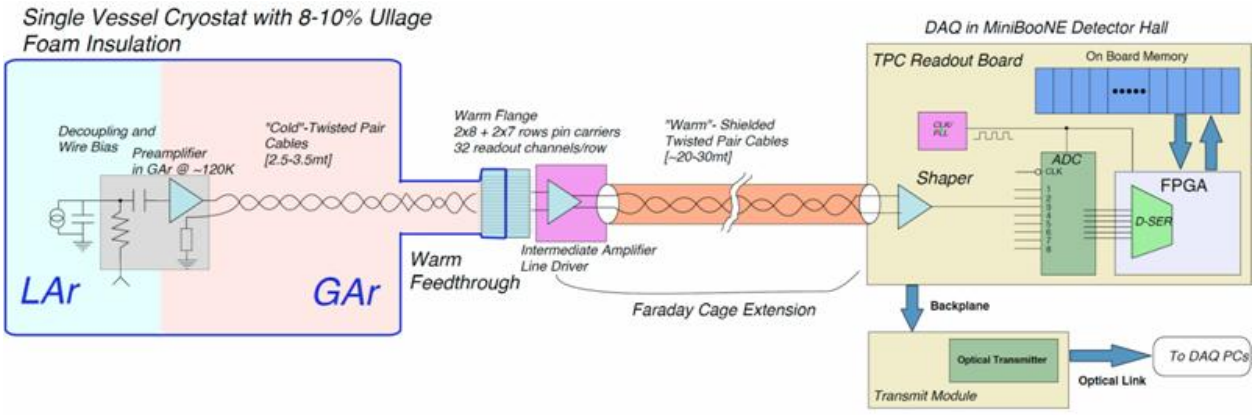


Figure 2.1 MicroBooNE readout electronics

2.2.2 AFTER Readout ASIC

The AFTER readout chip ([BARON]) was developed to read the data coming from the T2K (Tokai-to-Kamioka) ([TK2]) TPCs. The T2K experiment is dedicated to the study of neutrino oscillations. An intense neutrino beam from the J-PARC (Japan Proton Accelerator Research Complex) facility in Tokai is sent 295 km across Japan, where a detector (ND280) includes three large TPCs. These detectors use MICROMEGAS technology with anode plane readout pixilated into about 125,000 pads. One special feature of this detector is the low event rate.

The AFTER is a readout chip of 72 channels, where each channel includes a low noise charge preamplifier (CSA), a pole zero compensation stage, a second order Sallen-Key low pass filter and a 511-cell Switched Capacitor Array (SCA). See Figure 2.2.

This chip offers flexibility in order to accommodate its response to a few kinds of detectors and gas mixtures. For instance, the sampling frequency can go up to 50 MHz, the shaping time can be configured with 16 values from 100ns to 2µs, the gain can be configured with 4 gains from 120 fC to 600 fC and/or it has the possibility of processing both signal polarities depending on the choice of few external components.

This ASIC features a very low power consumption (<0.8mW/ch). Owing to the low event rates the 72 shaped signals are stored in analog memories and then digitized by a common external ADC. This allows achieving a very low power figure at the price of readout speed.

The AFTER is the central component of the front-end board and it is fabricated in 0.35µm CMOS technology. Unfortunately, this front-end board can only be used when the event rates are very low (~ 0.3Hz), which is not the case of the future TPCs.

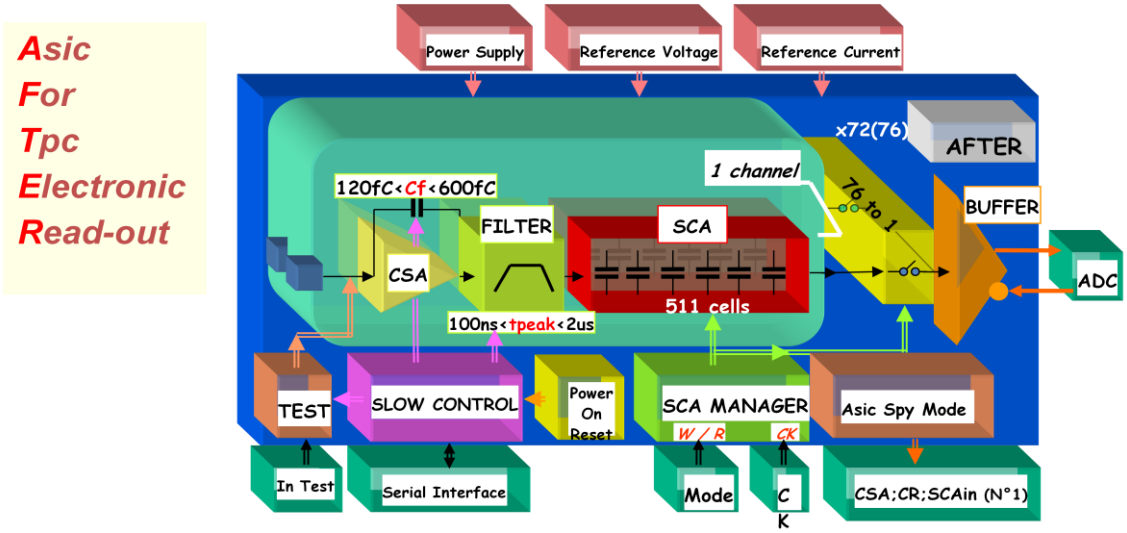


Figure 2.2 AFTER readout electronics

2.2.3 TimePix Readout ASIC

TimePix is another approach for future TPCs. This system is based on CMOS pixel detector combined with a gas gain grid ([LLOP07]). TimePix is an evolution from the Medipix2 ([LLOP02]) and provides information on the arrival time of the electron, Time-Over-Threshold (TOT) and/or event counting for each pixel. Unfortunately this chip cannot distinguish between different tracks arriving to the same pixel at different timing inside the time window.

Figure 2.3 shows the pixel cell schematic. The pixel is divided in two large blocks: analog side formed by the preamplifier, the discriminator (with polarity control pin) and 4-bit threshold adjustment, and the digital side formed by the Timepix Synchronization Logic (TSL), the 14-bit shift register, the overflow control logic, the Ref_Clk pixel buffer (up to 100 MHz) and an 8-bit Pixel Configuration Register (PCR). Each pixel can be independently configured in one of four different modes:

- Masked mode: pixel is off.
- Counting mode: 1-count for each signal over threshold.
- TOT mode: the counter is incremented continuously as long as the signal is above threshold.
- Arrival time mode: the counter is incremented continuously from the time the first hit arrives until the end of the shutter.

TimePix has been designed using 0.25µm CMOS technology, with a pixel cell of 55x55 μm^2 and the static power consumption of ~13.5µW. Measurements have shown an electronic pixel noise of ~100e^- rms, for a minimum detectable charge of 650e^-.

The impossibility of distinguishing tracks arriving to the same pixel at different timing makes this readout system useless for the future TPCs. Some redesign is being carried out to solve this issue. On the other hand, TimePix is being widely used to characterize readout chambers as MICROMEGAS or GEM.

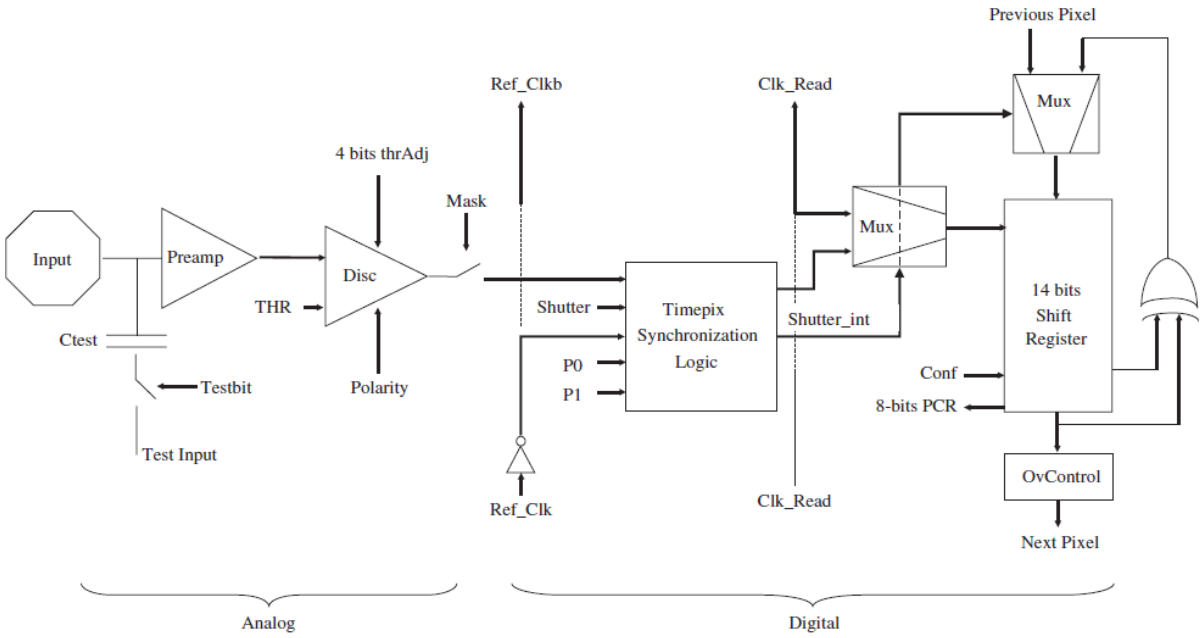


Figure 2.3 TimePix pixel cell schematic

2.2.4 Time-to-Digit Converters (TDCs) based readout electronics

The front-end electronics based on Time-to-Digital Converters (TDCs) measure the charge of the signal from the TPC with the help of a charge-to-time converter (QTC). QTCs represent the charge of the input signal as a digital pulse, where the digital pulse duration is proportional to the charge in the analog input signal, see Figure 2.4.

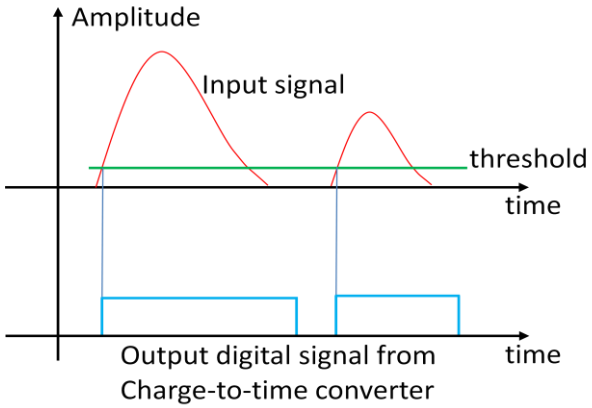


Figure 2.4 Measurement of a charge signal with a QTC

The arrival time of the analog signal is obtained from the moment of time when the analog input crosses the threshold. Therefore, the information on charge and arrival time of the input signal are encoded in the QTC output. Afterward, the signal from the QTC is digitized with a TDC.

The main advantage of this system is that only two values need to be recorded: the arrival time of the signal and the output pulse duration of the charge-to-time converter. This reduces enormously the data volume.

Figure 2.5 shows an example of TPC readout electronics based on TDCs ([KAUKHER]).

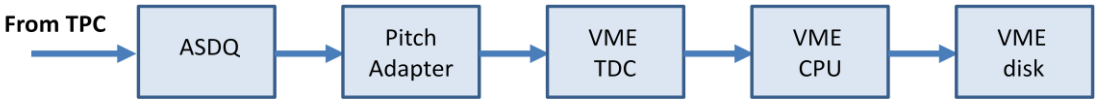


Figure 2.5 TPC data acquisition system based on TDC

This system is based on the Amplifier-Shaper-Discriminator-dE/dx (ASDQ) ([BOKHARI]). Figure 2.6 shows the block diagram of the ASDQ channel which contains a low noise preamplifier, ion tail compensation, multi-pole shaper, baseline restorer and dE/dx discriminator. The ASDQ provides eight channels of full analog signal processing between the readout chamber and the TDC, was implemented on a monolithic 5.4 mm x 3.9 mm silicon substrate using an analog bipolar process (radiation tolerant) and its power consumption is ~ 40 mW/ch.

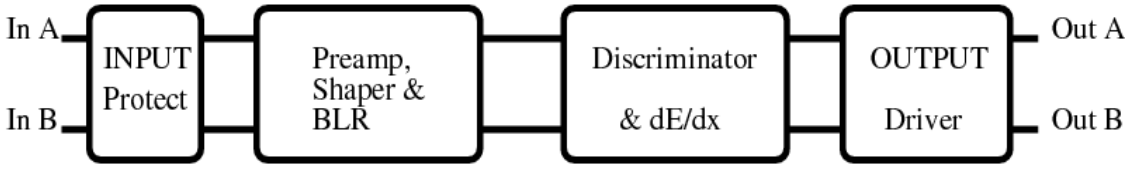


Figure 2.6 ASDQ channel

The output signals from the ASDQs, see Figure 2.5, are transmitted via 20 cm long flat flexible cables to a cable pitch adapter. The function of the pitch adapter is to connect fine-pitch flexible

cable to twisted pair cables, which are connected to a commercial VME TDCs based on four 32-channel TDC chips ([CHRIST]). This ASIC was fabricated in 0.25µm CMOS technology and the power consumption is ~ 10mW/ch.

Finally, the front-end electronics board designed for Large TPC Prototypes uses 4 ASDQ chips. The area occupied by the board is 4.4 mm x 30 mm, which allows working with pad sizes of ~1 mm x 4 mm. Therefore, the boards can be connected directly to a GEM module minimizing the path between the TPC pads and readout electronics, which reduces the pick-up noise. However, the power consumption of this system is larger than 50mW/ch and power pulsing techniques were never studied. This design is part of the R&D phase to understand better the behavior of such systems for large TPCs. Although its current low integration and high power consumption make this specific system inadequate for future TPCs.

2.2.5 PASA + ALTRO Readout electronics

The PASA + ALTRO chips form the readout electronics of the ALICE TPC ([ALICETPC]). A single readout channel is comprised of three basic units: a charge sensitive preamplifier/shaper, an Analog-to-Digital Converter (ADC) and a digital signal processing chain with a multi-event memory, see Figure 2.7.

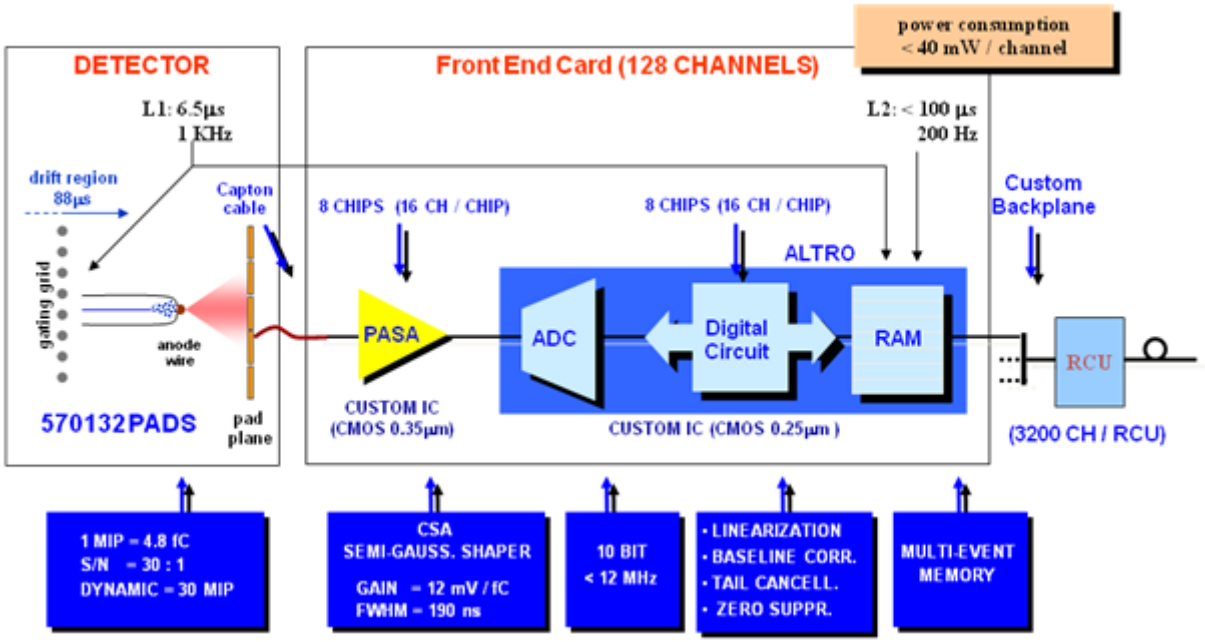


Figure 2.7 Basic components of the TPC front-end electronics.

The charge induced on the TPC pads is amplified and integrated by a low input-impedance amplifier, which is based on a Charge-Sensitive Amplifier followed by a semi-Gaussian pulse shaper of the second order. These analog functions are achieved by a custom 16 channels integrated Pre-Amplifier Shaping Amplifier (PASA) circuit fabricated in 0.35 µm CMOS technology.

The PASA output is connected to a 10-bit ADC, which digitizes the signal. Once the signal is in the digital domain, it is processed by a set of digital circuits. Starting from a first level trigger signal (L1), these digital circuits perform baseline correction, tail cancellation, zero suppression, formatting, and data storage in a multiple-event memory. Only when a second level trigger (L2) is received, the latest event data stream is frozen in the data memory until its complete readout takes place. The ADC and digital functions are implemented in a custom 16 channels integrated circuit called ALTRO (ALICE TPC ReadOut) ([ALTRO]), which was fabricated in 0.25µm CMOS technology.

Finally, each Front-End Card (FEC) contains 128 channels and is connected to the pad plane by means of six flexible cables. A maximum of 25 FECs are controlled by a Readout Control Unit (RCU), which interfaces the FECs to the DAQ, the trigger system, and the Detector Control System (DCS). The RCU broadcasts the trigger information to the individual FEC modules and controls the readout procedure. Both functions are implemented via a custom bus, the ALICE TPC Readout bus, which provides a data bandwidth up to 400 Mbyte/s. The interfacing of the RCU modules to the trigger and to the DAQ follows the standard data-acquisition architecture of the experiment ([ALICEDAQ]).

In summary, the PASA + ALTRO readout has high integration and power consumption <40mW/ch. This system was designed for an event rate of ~1KHz. However, the requirements for future TPCs are more severe in terms of integration and power consumption.

2.3 Conclusions

This chapter has presented several readout electronics for TPCs. Some of them are currently installed and working, others are only in study or development.

The first front-end presented was the MicroBooNE readout electronics, which has very low integration density, making this system unsuitable for future TPCs.

The next front-end presented was the AFTER chip, which is suitable only for applications with very low event rates. This feature allows to profit of low power consumption optimized architecture. On the other hand, this system has well separated analog and digital processing sections. Therefore, the low integration makes difficult the use of this front-end for the ILC/CLIC TPCs and the limit on the event rate makes impossible its use in the PANDA TPC.

A new approach using TimePix was presented. The main disadvantage of this front-end electronics is that, at the moment, it cannot distinguish different tracks arriving to the same pixel inside the time window. Consequently, this approach cannot be considered for the readout of TPCs. However a redesign of this front-end is being carried out.

A very interesting approach based on TDCs was presented. The main advantage of this system is the very low data volume. However, the current low integration density and high power

consumption make this system unsuitable for high granularity TPCs. However, the concept has been tested and further developments are being planned.

Finally, the PASA + ALTRO was presented, which is the readout of the ALICE TPC. This system mixes sensitive analog ADC circuits with high-speed digital processing whereas the low-noise amplifiers are still kept separate. Its integration is higher with respect to any of the other front-end electronics, but still not enough for the future TPCs explained in the last chapter. In conclusion, the density and power consumption exclude this system for future TPCs.

After analyzing several front-end electronics systems, it is concluded that none of them fulfill the strict requirements of future TPCs. For this reason a novel front-end electronics is proposed: the S-ALTRO chip.

The S-ALTRO is an evolution of the PASA + ALTRO front-end electronics. Although it inherits its main features from these two ICs, it will additionally include - higher integration, lower power consumption, larger flexibility and further functionality. The S-ALTRO provides the integration of multiple front-end preamplifier channels, shaper, ADC and digital signal processor integrated into the same chip. This plan is to integrate 64 channels in 130 nm CMOS technology with an estimated power consumption of 0.5mW/channels using power pulsing technique into this new ASIC. More details of the S-ALTRO are explained in chapter 3.

TABLE 2-2 summarizes the front-end electronics features.

TABLE 2-2 Readout electronics summary

TPC Readout	Integration	Ch/chip	Events Rate	Power	Data Reduction	Radiation hardness	Technology
MicroBooNE + FPGA	Very low	32	-	-	YES	NO	-
AFTER + ADC + FPGA	Low	AFTER=72 ADC=1	0.3 Hz	(a) AFTER <0.8mW/ch	NO	NO	AFTER= 350nm
TimePix	Very high	65536	(b)	~14µW/ch	Low volume of Data	~ up to 200 krads	250nm
ASDQ + TDC	Low	ASDQ=8 TDC=32	-	~50mW/ch	Low volume of Data	YES	ASDQ= Rad. tolerant analog bipolar TDC=250nm
PASA + ALTRO	High	PASA=16 ALTRO=16	1KHz	<40mW/ch	YES	~ up to 160 krads	250 nm
S-ALTRO	Very High	64	-	<0.5mW/ch (c)	YES	-	130 nm

a = ADC and FPGA power consumption no consider.
b = TimePix cannot distinguish tracks arriving to the same pixel at different timing.
c = Using power pulsing technique.

Chapter 3 S-ALTRO Chip Overview

3.1 Introduction

The S-ALTRO is a multi-purpose charge-amplifying, digitizing, processing and read-out chip. It is designed for TPCs, although in principle is suitable for any application that needs to sample charge signals with a 10-bit dynamics and up to 40 MHz frequency.

The S-ALTRO charge-amplifying block consists of a single ended charge sensitive amplifier, followed by pole-zero cancellation networks and a 4th-order low pass filter. Next, an embedded analog-to-digital converter digitizes the signal. After digitization, a pipelined data processor is able to remove from the input signal a wide range of perturbations, related to the non-ideal behavior of the detector, temperature variation of the electronics, environmental noise, etc. The signal is then compressed by removing all data below a programmable threshold, except for a specified number of pre- and post-samples around each peak. This produces non-zero data packets. Eventually, each data packet is marked with its time stamp and size, so that the original data can be reconstructed afterwards, and stored in the multi-acquisition memory which has a readout bandwidth of 300Mbyte/sec.

The S-ALTRO is a further development of its predecessor, the ALTRO (ALICE TPC Read Out) chip, shortly presented in chapter 2, but with higher integration (shaping amplifiers are now integrated in the same chip), lower power consumption, enhanced and more versatile signal processing. This ASIC plans to integrate 64 channels in 130 nm CMOS technology with an estimated power consumption of 0.5mW/channel using power pulsing technique with ~1.5% duty cycle (ILC).

This chapter addresses in detail the S-ALTRO architecture and functionality.

3.2 S-ALTRO chip architecture overview

One S-ALTRO consists of 64 complete and identical channels which are run in parallel. They are logically arranged as a grid and interconnected as such allowing a three dimensional approach for zero-suppression and the search for physical pulses. This interconnection is a new feature presented in this chip which provides a much more effective glitch rejection.

The common control logic is in charge of the interface between the outside world and the S-ALTRO chip, the storage of the configuration and the trigger manager.

The acquisition channel is comprised of four basic functional parts, see Figure 3.1:

- Programmable charge sensitive shaping amplifier (PCA): a front-end block to amplify, shape and convert into a differential output voltage the charge signals generated by GEM, MICROMEGAS or MWPC detectors.
- Analog-to-digital convertor (ADC): converts the analog input into a digital stream with 10-bit dynamic range and up to 40MS/s sampling rate.
- Digital processor and multi-event buffer: removes from the input signal a wide range of perturbations, suppress the pulse tail, compresses the signal and produces non-zero data packets. The multi-event buffer stores the data packets until a readout instruction is received.

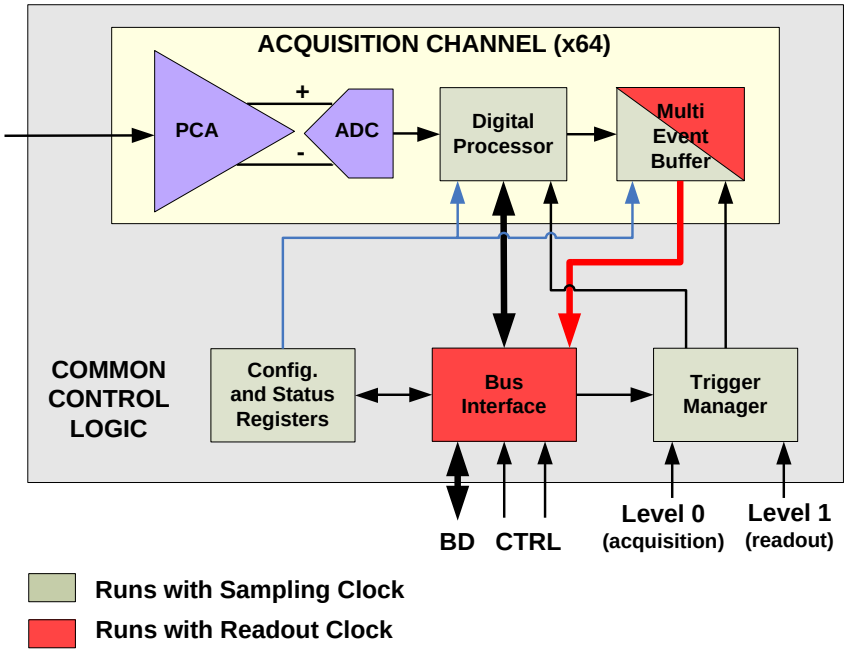


Figure 3.1 S-ALTRO block diagram

Figure 3.2 shows the digital processor block diagram. The operation mode depends on the data-path programmed via multiplexers (not all the paths are useful), which makes the system

suitable to serve a wide range of applications. Just the four most useful data-path modes are explained in the next sections. The circuit blocks that are not used in a given mode of operation can be disabled in order to reduce the power consumption.

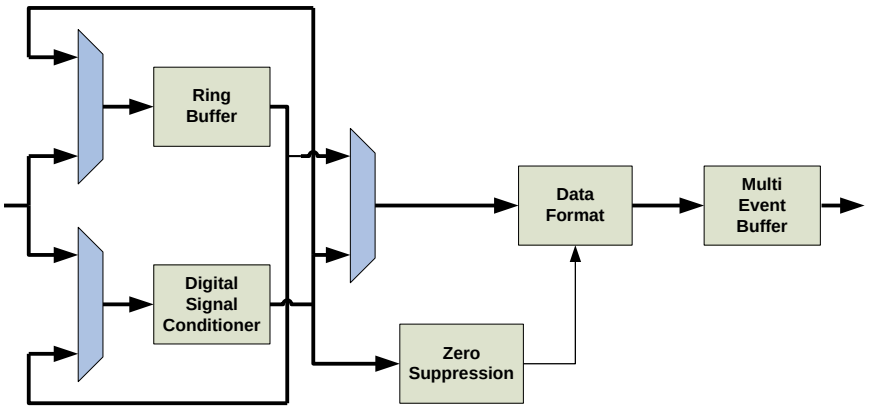


Figure 3.2 Digital processor block diagram

The digital processor consists of the following sub-modules described in detail later in the chapter:

- Ring Buffer (RB): has the same functionality as a FIFO, which allows saving data before the trigger arrives.
- Digital Signal Conditioner (DSC) or Digital Signal Processing (DSP): is used to remove any systematic or non-systematic perturbations from the signal. Baseline variations are compensated and long signal tails are removed.
- Zero Suppression (ZS): creates a flag when the signal is above a programmable 3D threshold (pulse finding, PF), except for a specified number of pre- and post-samples around each peak.
- Data Format (DF): removes all data out of the pulse using the ZS flag and gives a data format including the pulse time-stamp and length.
- Multi Event Buffer (MEB): This is the on-chip storage element for acquired data. It serves as temporary storage and/or a randomizer.

Next sections explain the different useful modes of operation.

3.2.1 Mode 1

This mode is probably the most commonly used, see Figure 3.3. The data is digitized, processed, zero-suppressed and stored. In this case, the zero suppression unit makes use of the pulse finder performing a 3D zero-suppression.

This mode requires two external triggers:

• A level zero trigger (L0) starts the acquisition, which will last for a programmable acquisition time. The outcome of the signal processing chain is written into the MEB.

• Upon a level one trigger (L1) the data written to the MEB is validated. This validation can happen at any time after the L0, but must have happened before the next L0 since data is overwritten otherwise.

In view of the future applications, this is the generic configuration. The applications differ only in the way the triggers are generated:

• ILC or CLIC: The beam pass generates L0 and L1 triggers.

• LHC: The L0 and L1 triggers come from other "trigger detectors".

• FAIR: L0 is triggered at the beginning of a run and read out concurrently (in study).

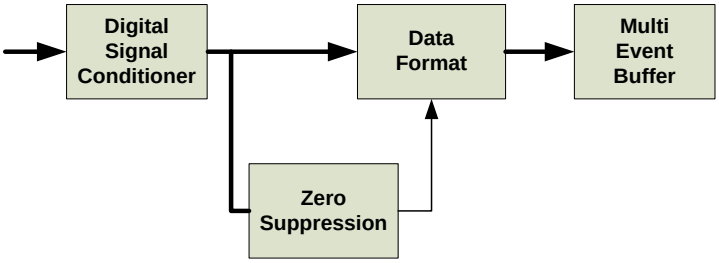


Figure 3.3 Data path 1 block diagram

3.2.2 Mode 2

This second mode of operation is an extension of mode 1, where a ring buffer is inserted between ADC and DSC, see Figure 3.4. The ring buffer allows a shift of the acquisition window towards time before the trigger. This mode is useful in cases where the trigger has a big latency.

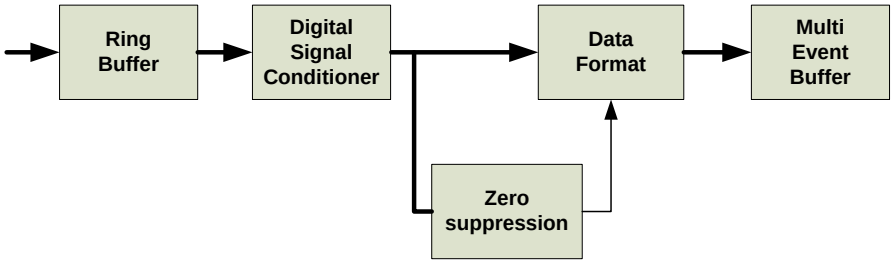


Figure 3.4 Data path 2 block diagram

3.2.3 Mode 3

The third mode has the DSC and RB swapped and the pulse finder is used to enable writing into the MEB, see Figure 3.5.

In this case the applications also differ only in the way how triggers are generated:

- Detector calibration: the signal is conditioned, but only channels with a pulse are validated by L1 (selective read-out).
- Oscilloscope mode: The pulse can also trigger the data acquisition, which acts as L0 and L1 at the same time. The system does not need any external trigger and works like an oscilloscope.

Both modes are very useful for detector calibration.

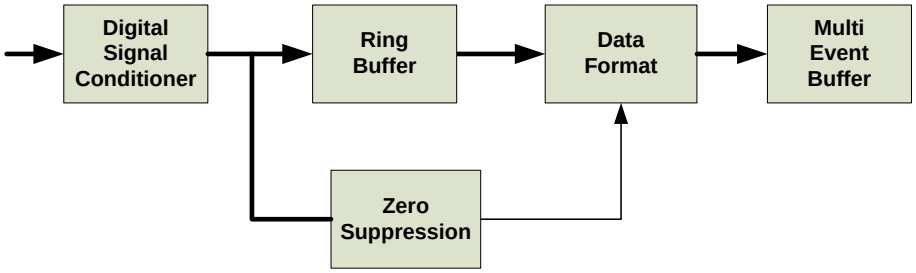


Figure 3.5 Data path 3 block diagram

3.2.4 Mode 4

This mode of operation is an extension of mode 3, although in this case the unprocessed signal data is saved where a pulse is found.

Mode 4 is basically useful for calibration purposes, where the unprocessed signal data (raw data) is saved only in channels where a pulse is found.

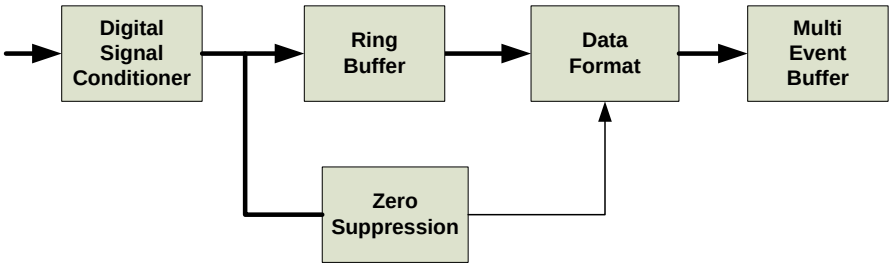


Figure 3.6 Data path 4 block diagram

3.3 Programmable charge sensitive shaping amplifier

The PCA circuit consists of a single ended Charge Sensitive Amplifier (CSA), followed by a pole-zero cancellation network and two low-pass filtering stages, see Figure 3.7.

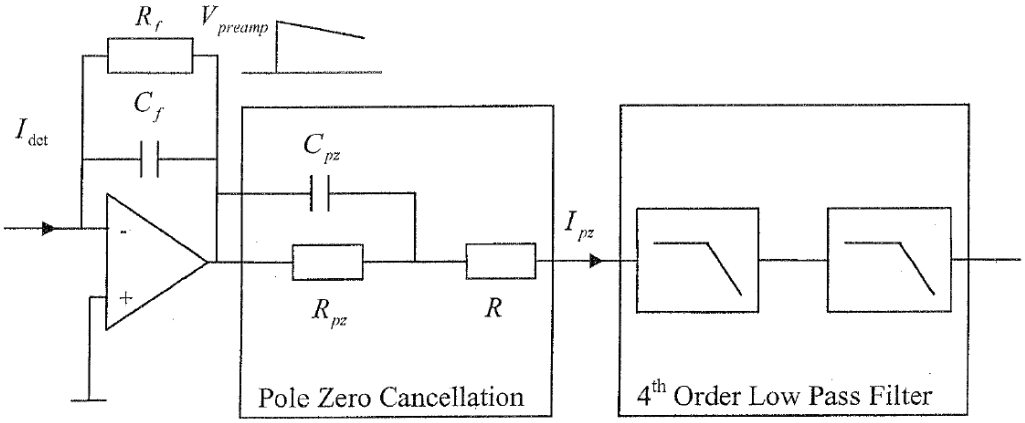


Figure 3.7 Programmable charge sensitive amplifier block diagram

The feedback capacitance of the CSA is continuously discharged by a MOS transistor biased in the Mega Ohm region in order to minimize the current noise. The implemented non-linear pole-zero networks allows high rate operation while maintaining good cancellation of the pole introduced by the preamplifier.

The first shaping filter consists of a scaled replica of the CSA in order to save power but still maintaining the same DC operational point, which is essential for the implementation of the pole-zero network. The second low-pass filtering stage further limits the signal bandwidth before the ADC and, in addition, converts the single ended input into a differential output in the range 0.25V-1.25V, corresponding to 2V peak-to-peak. The bandwidth will depend on the peaking time, although it will be around 5MHz. The power consumption of a single CSA is ~ 8mW.

The output response to an input current pulse is a semi-Gaussian signal, where some parameters of the CSA, like the gain and the shaping time, are programmable by some dedicated pads. The main parameters are:

- Conversion gain: 12, 15, 19 or 27 mV/fC.
- Peaking time: 30, 60, 90 or 120 ns.
- Polarity: positive or negative pulses.
- Decay bias: from 0.24 μs to 2.8μs.

The circuit described was prototyped in a 16 channel chip, produced in 2007 and used widely for several tests exploring the whole space of possible settings. Some measured results from one of the PCA prototype using the ALTRO chip for readout are shown.

Figure 3.8 shows that the impulse response function is very close to the theoretical semi-Gaussian. Figure 3.9 shows that the measured peaking times are very close to design values (the missing and noisy channels are due to the set-up used). Similar tests were done on a large number of chips showing similar results.

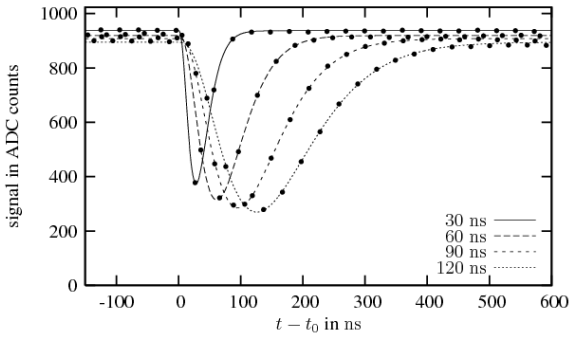


Figure 3.8 Different peaking times for fixed conversion gain: 27 mV/fC

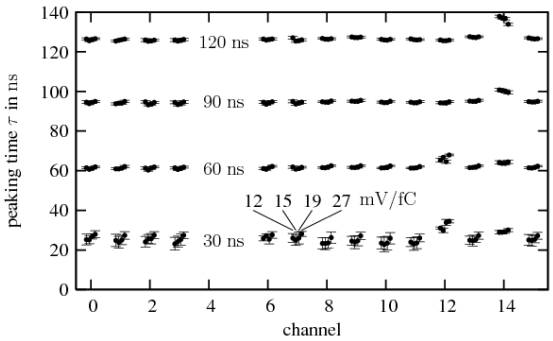


Figure 3.9 Measured spread in peaking time for different settings of peaking time and conversion gain

On the other hand, the equivalent noise charge with respect to peaking time and input capacitance was simulated, see Figure 3.10. Minimum noise is achieved for minimum input capacitance and longest peaking time.

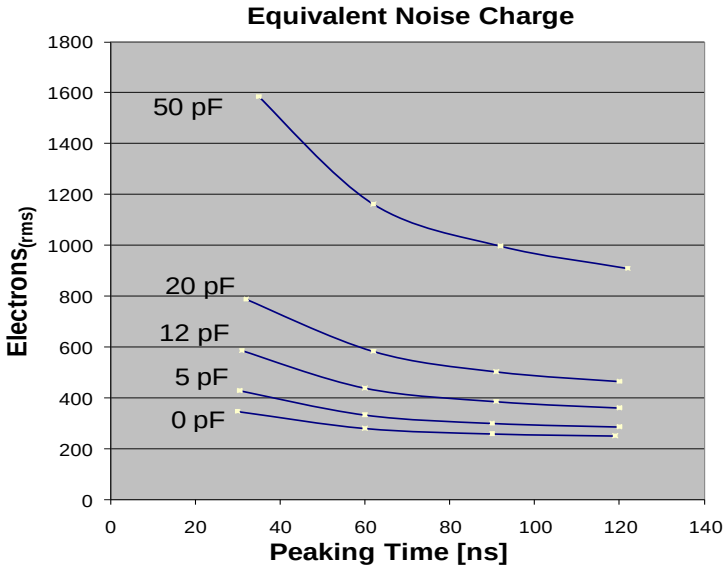


Figure 3.10 Simulated equivalent noise charge versus different peaking time settings

3.4 Analog-to-digital conversion

The S-ALTRO ADC is based on the 10 bits ADC IP block implemented in 130nm CMOS technology and developed at CERN ([FRANCA]). The block diagram is shown in Figure 3.11.

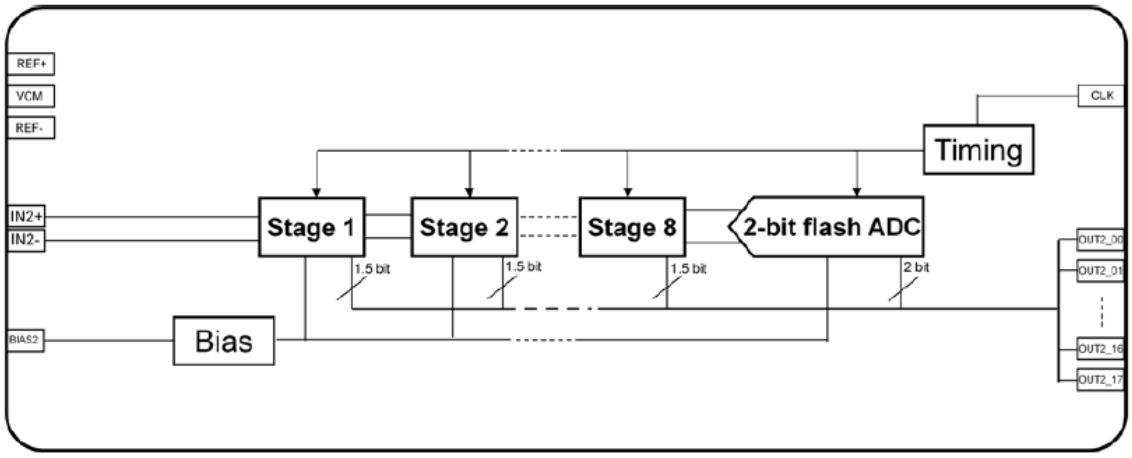


Figure 3.11 ADC block diagram

This ADC has been designed to be differentially driven (IN2+, IN2-), where both inputs of a given channel should be centred on the same common mode voltage (VCM) and kept within the voltage references range (REF+ and REF-). The nominal operating frequency of this ADC is 40MS/s, however, the sampling frequency can vary from 20MS/s-40MS/s, so that it is possible (or even required) to adjust the power consumption by tuning the biasing currents (BIAS2) of the eight internal operational amplifiers of the ADC. The CLK is the clock signal that drives the different tasks of the ADC blocks (sampling, comparing, multiplying, etc). Finally, the digital outputs (from OUT2_00 to OUT2_17) are the CMOS driven digital outputs of the ADC.

This ADC is based on a pipelined structure implemented with switched capacitors in eight 1.5-bit stages and one 2-bit stage. The outputs of these conversion stages are combined in a digital correction block to form a 10-bit word and remove the redundancy. One of the intrinsic characteristics of the pipelined ADC is that it requires several clock cycles to complete a conversion. The data latency depends on the stage resolution and clocking scheme. In this implementation the latency is 7 clock cycles.

Simulations have shown that the sampling switches guarantee that the signal distortion stays below 72dB over a 20MHz bandwidth for the worst process corners. The power consumption per channel is ~20 mW at 20 MS/s and ~33 mW at 40 MS/s.

This ADC has 2 power domains: an analog domain for the amplifiers which require a low-noise supply and a digital domain for comparators and switches which create noise, requiring close decoupling of the PINS. The two grounds must be kept at the same voltage, and the two V_{DD} have the same nominal value of 1.5V.

3.5 Digital processor

The digital processor consists of five main blocks, see Figure 3.2: ring buffer (RG), digital signal conditioner (DSC), 3D zero suppression (ZS), data formatter (DF) and multi-even buffer (MEB). Moreover, the DSC can be divided in other three sub-blocks: the baseline correction 1 (BC1), the digital shaper (DS) and the baseline correction 2 (BC2).

The next sections explain in detail the functionality of each of these blocks.

3.5.1 Ring buffer and multi-event buffer

Each S-ALTRO channel is equipped with 8k of 10-bit wide memory. This memory is split up into one part that serves as a RB and the remaining part that is used as the MEB.

The following partitions are possible:

- no RB, 8k MEB
- 1k RB, 7k MEB
- 2k RB, 6k MEB
- 4k RB, 4k MEB

From outside, the memory block looks like one single dual port memory, see Figure 3.12. However, internal controls select among the partitions. Both ports can be used simultaneously.

The RB has the same functionality of a FIFO, shifting the data stream of the acquisition window towards time before the trigger.

On the contrary, the MEB stores the data stream coming from the DF to be eventually readout. This memory that could be 8k, 7k, 6k or 4k, 10-bits wide is at the same time partitioned in a programmable number of buffers (4 or 8). When the data stream is validated through the L1 trigger, the write address pointer goes to the next partition block. In the case that all the memories are occupied, the commands to process new data streams are ignored. Partitions are free after readout.

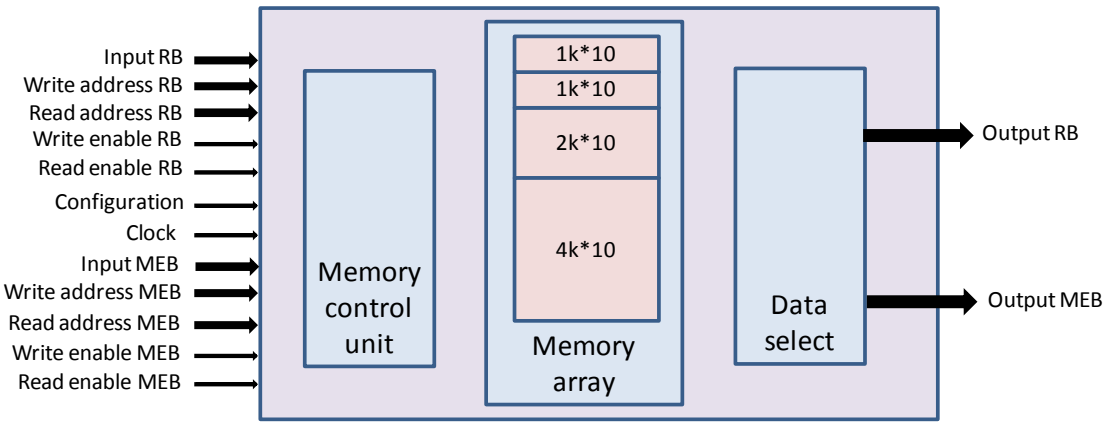


Figure 3.12 Channel memory architecture block diagram

3.5.2 Digital Signal Conditioner - Baseline Correction 1

The Baseline Correction 1 (BC1) is the first stage of the digital signal conditioner and its main task is to remove the low frequency perturbations and systematic effects. Some examples of these effects are temperature variations, power variations or perturbations induced by the switching of the gating grid in multi-wire proportional chambers. Figure 3.13 shows an example of two types of perturbations which will be removed with this filter.

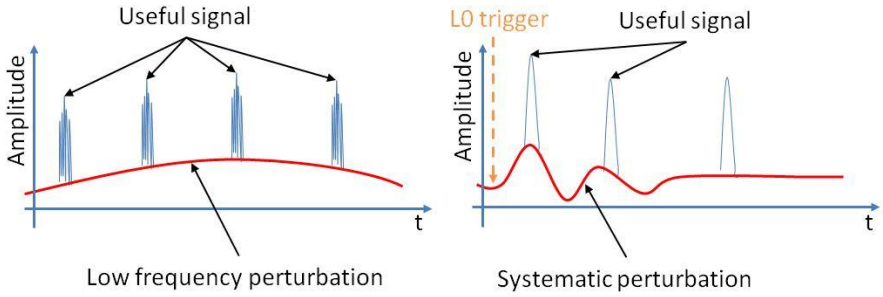


Figure 3.13 Types of perturbation

The BC1 circuit has three different modes of operation:

- Subtraction Mode: this mode performs a subtraction of a given value from the input signal coming directly from the ADC output. In turn, this mode is divided in other three sub-modes depending on the origin of the given values to be subtracted.

    1) Fix-subtraction: the value to be subtracted is constant for the entire time window. Typically used to remove a fixed offset from the input signal.

    2) Time dependent subtraction: the value to be subtracted comes from an internal memory, where previously the values were stored. This case is typically applied

to remove the perturbations from the pulsed gating grid. After an analysis of this effect in the ALICE TPC, it was concluded that the depth of the memory should be 256 addresses.

3) Self-calibrated subtraction: an IIR filter calculates the value of the baseline outside the processing window and subtracts it from the input signal. When the level 0 trigger arrives, the last baseline calculated value is frozen in a register.

- Conversion Mode: conversion function values are stored in the BC1 memory. When the level 0 trigger arrives, the BC1 acts like a look-up-table where the BC1 input addresses the BC1 memory.

- Test Mode: a pattern is saved in the BC1 memory and later it is used to feed the digital filters. The BC1 memory pattern emulates the data coming from the ADC. The pattern is created by numerical analysis software or data stored from a real detector.

The modes have been presented individually, however they could be combined offering a wide range of possibilities. TABLE 3-1 shows a summary of the most commonly used modes of operation.

TABLE 3-1 BC1 modes of configuration

BC1		Configuration					
Modes		Option A	Option B	Option C	Option D	Option E	Option F
	1	√	√		√		
Subtraction	2		√	√	√		
	3			√	√		
Conversion						√	
Test							√

The hardware implementation and optimizations of this block with respect to the ALTRO chip are explained in detail in chapter 4.

3.5.3 Digital Signal Conditioner - Digital Shaper

TPCs signals have rather complex shapes. The complexity of these signals depends on the type of readout chamber, chamber geometry, gas composition and voltages applied.

Undershoots and long tails are the most disturbing effects for different reasons. For instance, a long signal tail together with a high occupancy environment creates pile up effects, which make the zero suppression block inefficient. On the other hand, undershoots after the pulses perturb the measurement of the amplitude after zero suppression. Both effects can be removed with the digital shaper choosing the right filter parameters. Figure 3.14 shows an example of these effects.

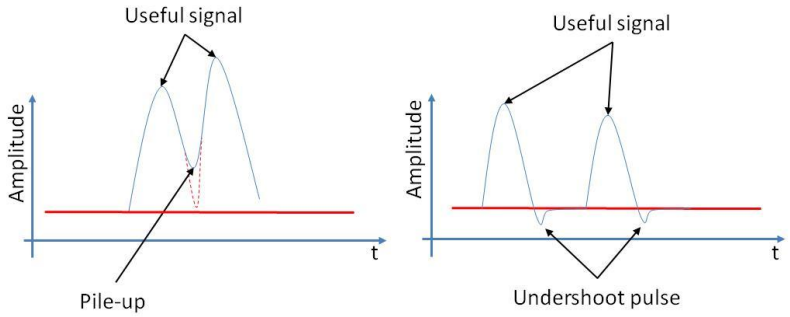


Figure 3.14 Long tail and undershoot examples

A flexible filter like the digital shaper (4th order pole-zero cancellation) is always useful in such cases.

Other applications of this filter are the delay of the peaking time, the symmetrization of the semi-gaussian shape or the conversion from bipolar to unipolar signals. Figure 3.15 shows the correction of a non-symmetric pulse. The output has been shaped with delayed peaking time and more symmetric shape. Figure 3.16 shows the conversion from bipolar input to unipolar output. The output has been shaped to compensate the negative undershoot, reduce the peaking time and narrow the signal.

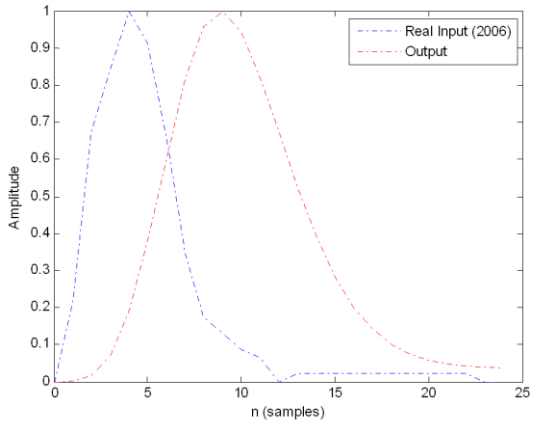


Figure 3.15 Simulation of the DS to symmetrize a semi-gaussian shape and delay the peaking time

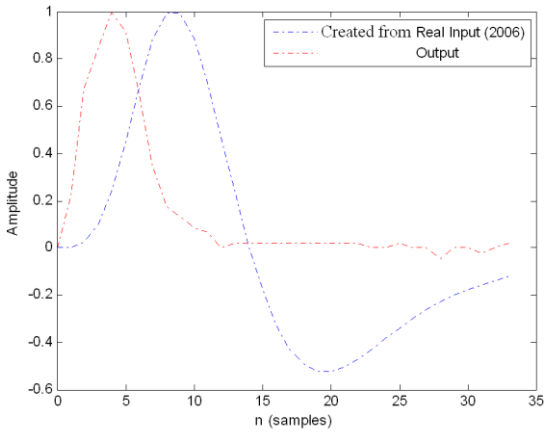


Figure 3.16 Simulation of the DS to correct from bipolar input to unipolar output

The next chapter presents an extensive study of different possible architectures for the DS. Moreover, the architectures are compared in terms of hardware resources, overflow and errors due to round-off and coefficient quantification.

3.5.4 Digital Signal Conditioner - Baseline Correction 2

The Baseline Correction 2 (BC2) corrects non-systematic perturbations inside the processing window. These perturbations can have different frequencies depending on the origin, for instance temperature drifts.

The BC2 is needed because the BC1 does not correct non-systematic signal perturbations inside the acquisition window and the DS cannot remove them as they are not related to the pulse shape. After the BC2 the signal is ready to be zero-subtracted.

The BC2 is based on two main blocks, a double threshold scheme and a flexible moving average filter (MAF).

The double threshold scheme, with thresholds above and below the signal, creates an acceptance window that follows the variations of the signal. When a very fast signal arrives (useful pulse) the samples are out of the acceptance window and the baseline calculation is frozen. Inside the acceptance window, the baseline is updated based on the average of a programmable number of samples.

Finally, the value of each input is corrected using the last value calculated by the moving average filter. At this point, the signal is sitting on 0, and anything below this value will be clipped to 0. If there were effects to be observed below the baseline, a discretionary offset can be added. Figure 3.17 shows the basic principle.

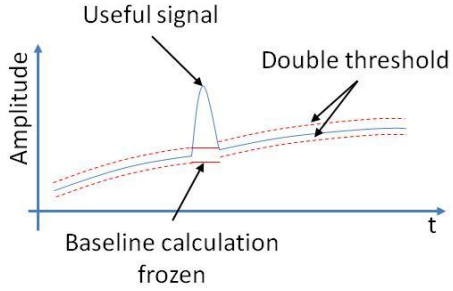


Figure 3.17 BC2 principle

The implementation details are explained in the next chapter.

3.5.5 3D zero suppression

This technique is based on the removal of data below a threshold which contains no useful information, considered as noise. The zero suppression technique is widely used in the HEP community due to its efficiency in compressing the data while preserving the relevant information (pulse amplitude and time)

The configuration of the threshold is always a trade-off between storing too little signal data or too much noise. However, to reduce the noise sensitivity some filters include a glitch filter and

the possibility to store a programmable number of samples before and after the pulse above threshold. The glitch filter checks for consecutive samples above the threshold. In order to guarantee that the zero suppression never increases the data volume, whenever two consecutive pulses (sequences of samples above threshold) are too close in time, they will be merged in a single sequence such that time stamp, pulse length pre- and post-samples do not have to be duplicated.

Figure 3.18 shows an example of one dimension zero suppression implemented in the ALTRO chip where the techniques mentioned were implemented. When the data for the zero suppression comes from only one channel it is called one-dimensional (1D) zero suppression.

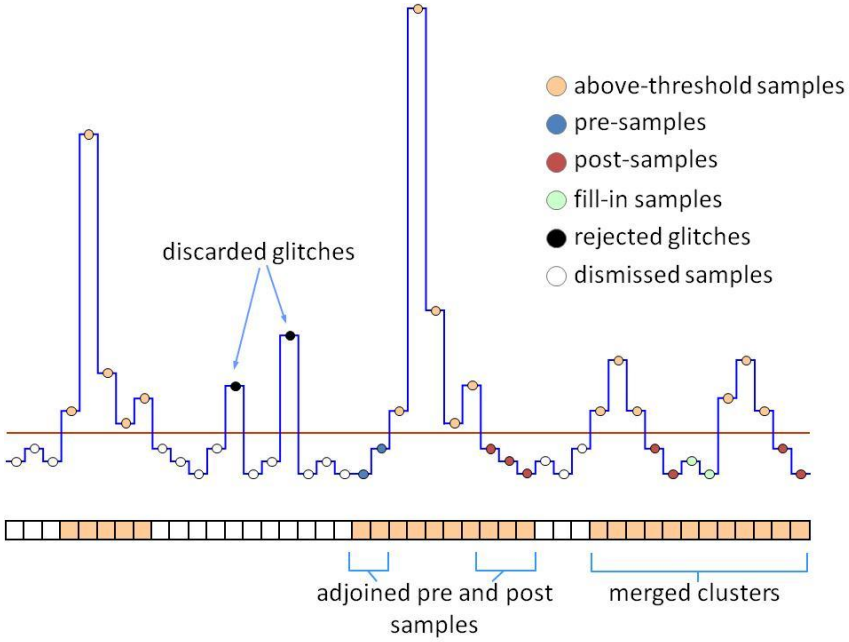


Figure 3.18 One-dimensional zero suppression example

The S-ALTRO chip plans to introduce a three-dimensional (3D) zero suppression scheme, which is based on three main functions: pulse finder, inter-channel communication and inter-chip communication.

3.5.5.1 Pulse finder

A pulse finder searches pulses around its channel at the current time 'T' in three dimensions (two spatial and time dimensions). Figure 3.19 shows two examples, one for a detector signal and other for a noise signal, both in spatial and time dimensions. The spatial dimensions shows that the detector signal has few channels over threshold while the noise signal just one channel presents signal over the threshold. Same example is shown for the time dimension.

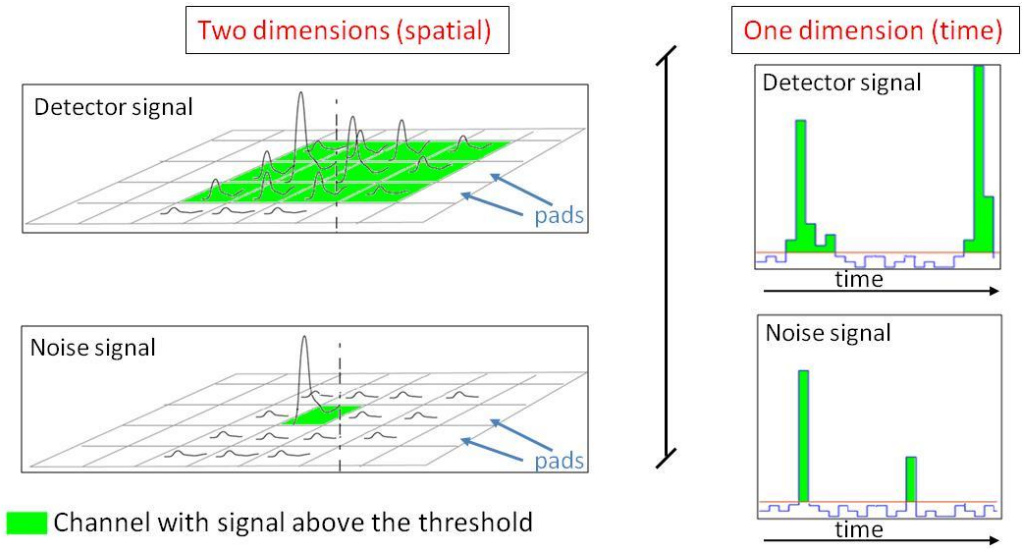


Figure 3.19 Three dimensions pulse finder example

The Pulse Finder criteria for a pulse are as follows:

- The value of the channel at time T has to exceed a threshold, called high threshold.
- A number of adjacent channels at times T-1, T and T+1 have to exceed another threshold, called low threshold.
- Finally, the number of channels exceeding the low threshold at T-1, T and T+1 have to exceed another threshold, called threshold n. If this happens, the pulse is validated.

Figure 3.20 shows an example of the pulse finder criteria where the number of channels exceeding the low threshold is 12. Therefore, if the threshold n is less than 12, the pulse is validated.

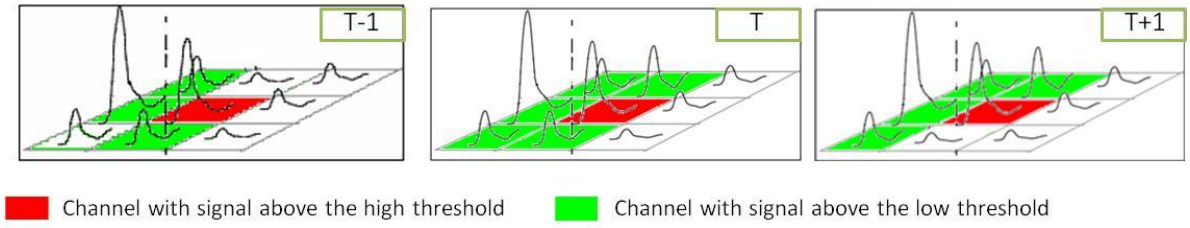


Figure 3.20 Pulse finder criteria example

When the pulse is validated, a 'hit found' signal is generated. This signal is used to suppress the samples available to the data channels zero suppression unit and multi event buffer, as well as to those of the adjacent channels via the inter-channel distribution network, explained in the next sub-section.

The different thresholds are set channel by channel to adjust better to the different noise characteristic and border effects.

3.5.5.2 Inter-channel and inter-chip communication

The pulse finder is based on the communication among adjacent channels inside and outside the S-ALTRO chip, called inter-channel and inter-chip communication.

Inside each S-ALTRO chip there are 64 channels arranged as a grid, and each channel transmits two signals to its adjacent channel. However, even if all channels are identical, the interconnection between them cannot be identical due to their different location (core and border). See Figure 3.21.

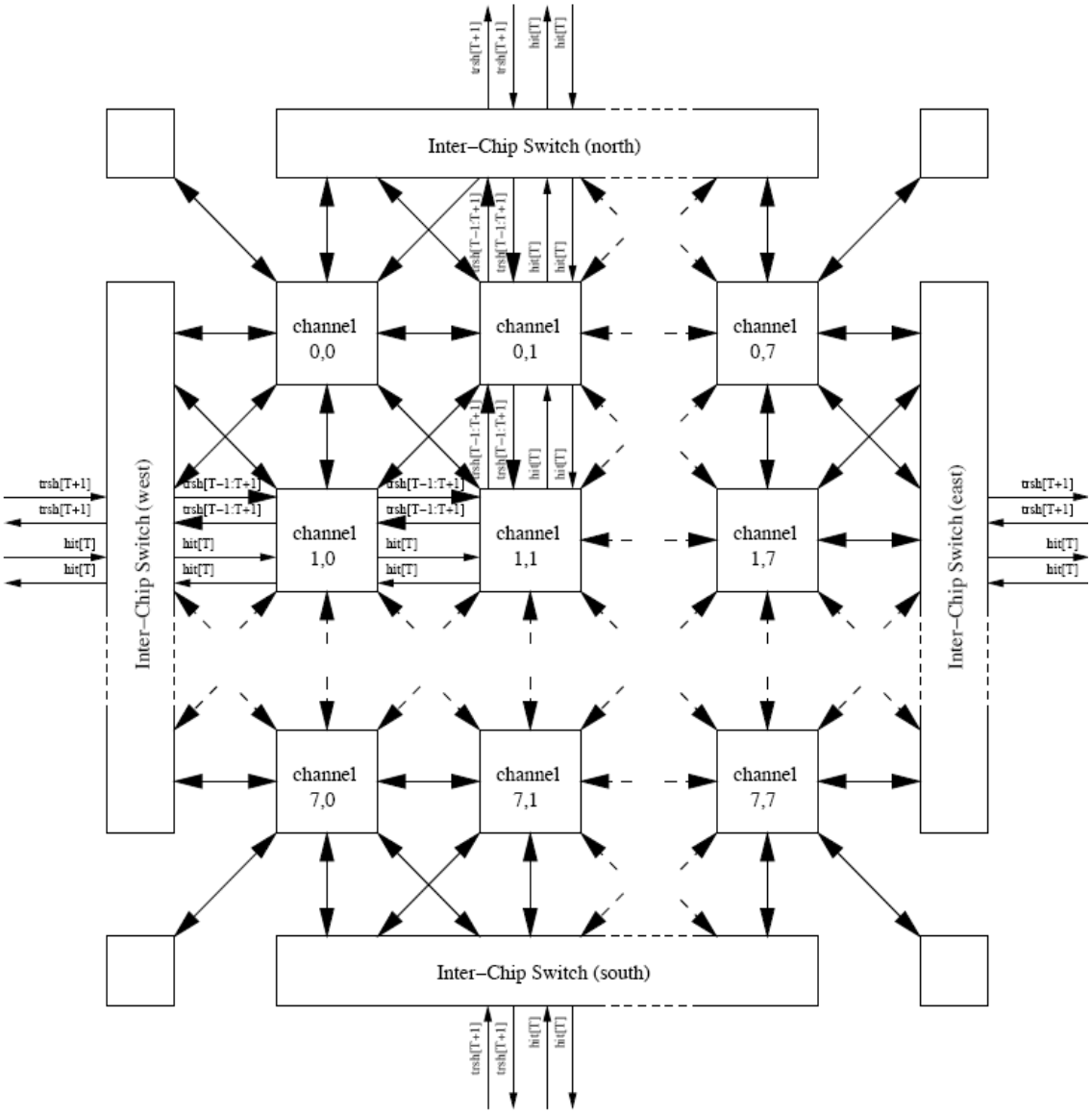


Figure 3.21 Inter-channel and inter-chip communication block diagram

The inter-channel communication corresponds to the channels in the core, for instance, channel 1,1 in Figure 3.21. The core channels do not need anything special to interconnect them because all the information is contained within the chip. The information sent to the adjacent channels is:

- Channel above the low threshold at times T-1, T and T+1.
- Channel above the high threshold at time T (hit).

The channel inputs can be masked to zero to ignore the information arriving from a dead channel or simply disable the 3D zero suppressing scheme.

The border channels need to get information from adjacent chips. The communication with the adjacent chips differs with respect to the inter-channel communication. In this case, the inter-chip communication needs to transmit just two signals:

- Channel above the low threshold at time T-1. The signals at times T and T+1 can be generated by the inter-switch units.
- Channel above the high threshold at time T (hit).

The inter-chip communication is divided in four inter-switch units, which connect the different borders to the adjacent chips. The corners are a special case, which are connected individually to the adjacent chips. Same as for channels, the input information to the inter-switch units can be masked to zero to ignore the information arriving from a dead chip or simply disable the inter-chip communication.

There are two different possibilities for the inter-switch units:

- Full interconnection: all the signals are sent to the neighbour chips. Number of lines depends on the number of channels/chip. For instance, for 64ch/chip -> 32 x 4 lines
- One line interconnection: a logical OR of all the signals is sent per side. Number of lines does not depend on the number of channels/chip. For instance, always 4 x 4 lines.

A simulation of both inter-switch possibilities is presented in Figure 3.22. It is shown that there are no big differences in the results. However, the full interconnection needs 9 times more lines for a 64 channels chip, thus increasing the hardware resources and noise introduced. Therefore, the full interconnection is discarded.

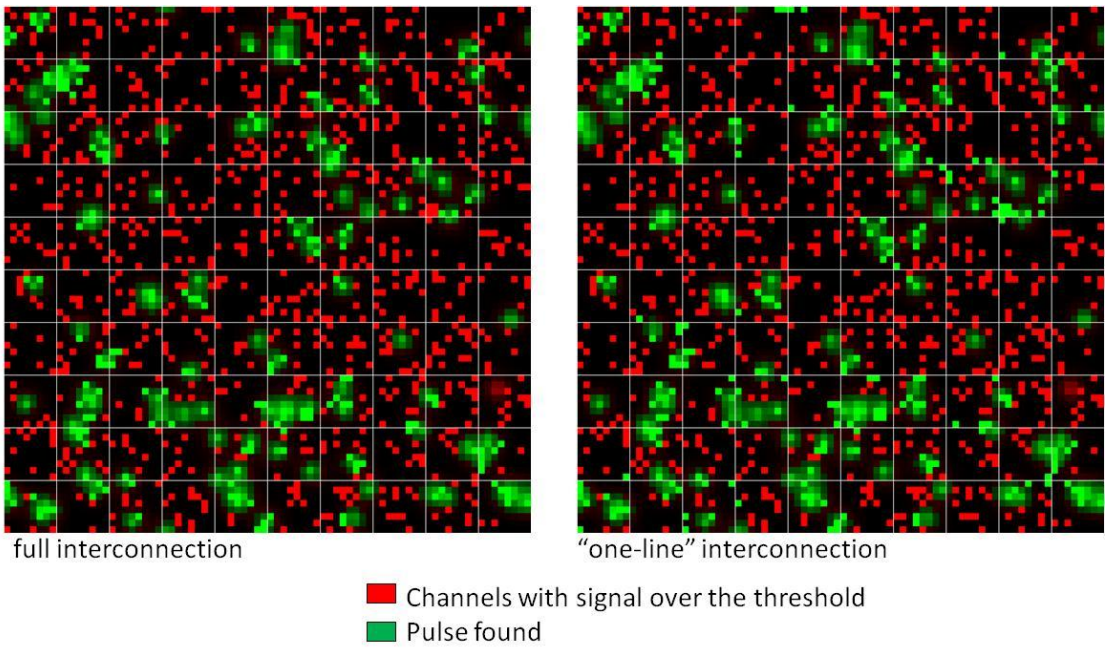


Figure 3.22 Interconnection scheme simulation

3.5.6 Internal data format

The removal of zeros between pulses would suppress the time information. However, a technique called 'run length encoding' (RLE) is performed to keep the information efficiently in 16-bit data format. The RLE stores each pulse by the position in time, the length and the current amplitude. The time information is related to the number of zeros suppressed between pulses. The length corresponds directly to the number of samples in the pulse. Finally, the amplitude is the 10-bit numeric value above the threshold.

The internal data format starts with the chip ID and the event/channel ID. The chip ID is for bookkeeping purposes only, while the channel ID is crucial to provide information of the channel. The data format continues with the number of zeros (RTS), the number of samples of the pulse (DL) and, finally, the stream of samples packed into 16 bits wide. The following pulses are packed with the same structure. See Figure 3.23.

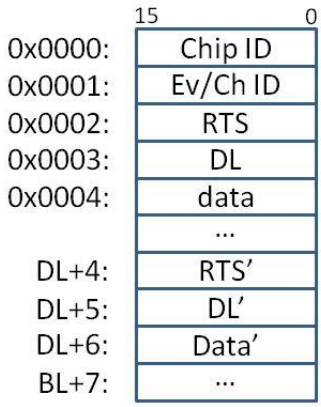


Figure 3.23 Data format sequence

This data format has two limitations related to an overflow of the DL and RTS, both 65535. Any number of bits could be overflowed in the free-running scheme. For this reason, in the case of an RTS overflow an empty cluster will be introduced and in the case of DL overflow the pulse will be divided in two blocks.

Another potential limitation is that this data format requires a minimum of two samples below the threshold in order to have enough time to pack all the necessary information. This requirement is easily achieved merging the pulses as explained in the last section. Figure 3.24 shows an example where the minimum RTS length is not respected and the data format unit would need to write the data and the new RTS value at the same time.

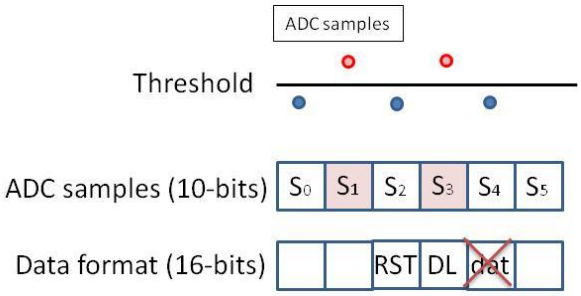


Figure 3.24 Data format requirement example

On the other hand, the internal data format is wider than the ADC samples. Therefore, after eight consecutive ADC samples above the threshold the output word is partially empty. To solve that the data format unit waits three clock cycles every 8 ADC samples above the threshold. See Figure 3.25.

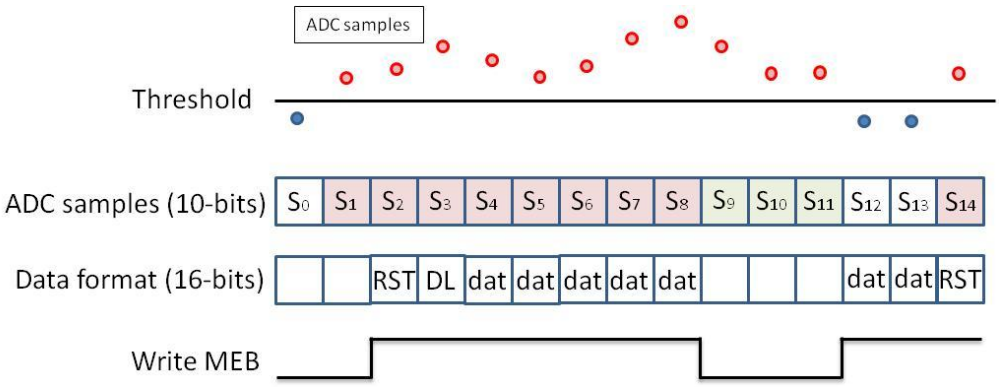


Figure 3.25 Data format unit for longer length than eight ADC samples above threshold

Another important consideration is that the internal data format does not include any information about the end of the event. That will be stored in an auxiliary memory which includes the event length of the 64 channels. See Figure 3.26.

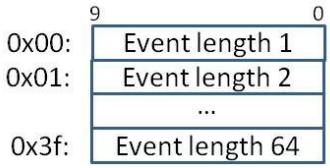


Figure 3.26 Event allocation table

3.6 Interface

The S-ALTRO bus consists of 16 address/data lines, one select line, one data valid line, two level triggers, a global reset and two clocks. Besides those, the S-ALTRO chip has 8 outputs and 8 inputs for the 3D zero suppression, which can be optionally used or left unconnected. The S-ALTRO interface lines are shown in TABLE 3-2.

TABLE 3-2 S-ALTRO interface lines.

Signal Name	Function	Number of bits	Direction	Polarity
DATA	Address / Data	16	Bi-directional	H
SELECT	Address / Data selection	1	Bi-directional	L
VALID	Data valid	1	Input (pull-up)	L
LVL0	Level-0 Trigger	1	Input	L
LVL1	Level-1 Trigger	1	Input	L
GRST	Global Reset	1	Input	L
SCLK	Sampling Clock	1	Input	-
RCLK	Readout Clock	1	Input	-
ZS_IN	3D zero suppression inputs	8	Input (pull-down)	H
ZS_OUT	3D zero suppression outputs	8	Output	H

Hereafter there is a short description of the interface lines:

DATA: it is a 16-bit bidirectional bus address/data. Depending on the configuration of the bus there are different address spaces which are shown in TABLE 3-3.

TABLE 3-3 DATA address space

	Bit number	Function	Description
Transaction 1 (address)	15	Transaction	To distinguish between transaction 1 and transaction 2. The transaction 1 corresponds to value 0.
	14	Parity bit	Parity bit of the 16 bits of the bus. The parity bit allows the detection of single bit errors in the transmission.
	13 - 8	Not implemented	Fixed to 0.
	7	S-ALTRO/other	To distinguish between instructions to the S-ALTRO or to another address space.
	6	Broadcast	The address refers to all the S-ALTRO connected to the bus and all the channels. In this case, the channel address is ignored and the transaction 2 is not needed.
	5 - 0	Instruction code	Can be either write/read a status register or a command. Some examples will be shown later in the section.
Transaction 2 (address)	15	Transaction	To distinguish between transaction 1 and transaction 2. The transaction 2 corresponds to value 1.
	14	Parity bit	Parity bit of the 16 bits of the bus. The parity bit allows the detection of single bit errors in the transmission.
	13 - 0	Channel address	During the instruction cycle these bits are compared with the hard-wired address. From the most significant bit, 1bit select the branch address, 4bits the board, 3 bits the S-ALTRO address in the board and 6 bits the channel address.
Data	15 - 0	Data	Carries the data when writing or reading registers or readout command.

SELECT: it is a bidirectional line. Normally, it is configured as an input selecting if DATA correspond to address or data. Just in the case of readout command this line is used as output to validate each sample from DATA.

VALID: it is an input with a pull-up resistor. When it is asserted indicates that a valid word is placed in the DATA bus and the communication protocol starts.

LVL0 and LVL1: input lines which represent the level 0 and level 1 trigger explained at the beginning of the chapter.

GRST: it is a global low level reset. This reset does not clear the status registers, although it initializes the counter and state machines. The status registers can only be cleared overwriting on them.

SCLK and RCLK: sampling and readout clock lines. Sampling clock can have a maximum frequency of 40MHz, while the readout clock can have a maximum of 80MHz. The readout clock is the engine of the interface.

ZS_IN and ZS_OUT: these lines are needed for the 3D zero suppression scheme. However, if the 3D zero suppression is not needed, those 16 lines could be left unconnected.

3.6.1 S-ALTRO protocol

The S-ALTRO protocol requires three transactions of the 16-bit bus to write or read the status registers, two transactions to write or read the status registers in broadcast mode and just one transition to send a command. All the instructions of the S-ALTRO start when VALID is asserted. TABLE 3-4 shows few examples of instruction codes.

TABLE 3-4 Instruction code examples

Name	Address	Number transactions	Data width	Broad-cast	Meaning
W_K1	00	3	13	No	Write the filter coefficient K1 (DS)
R_K1	01	3	13	No	Read the filter coefficient K1 (DS)
W_K2	00	3	13	No	Write the filter coefficient K2 (DS)
...	...	...	...	...	...
W_K1	00	2	13	Yes	Write the filter coefficient K1 (DS)
R_K1	01	2	13	Yes	Read the filter coefficient K1 (DS)
...	...	...	...	...	...
ALLRDO	3A	1	-	-	Command chip readout
SWTRG	3B	1	-	-	Command software trigger
...	...	...	...	...	...

- Write/read status register example: In this case the S-ALTRO acts as slave and an external control acts as master. The operation is synchronous with the clock RCLK. The operation starts in the rising edge of the RCLK, on which VALID is sampled low. SELECT line chooses if the DATA bus should be decoded as address or data. Therefore, the first two cycles SELECT line is held to low (address), and the third one to high (data). Figure 3.27 shows an example of the chronogram.

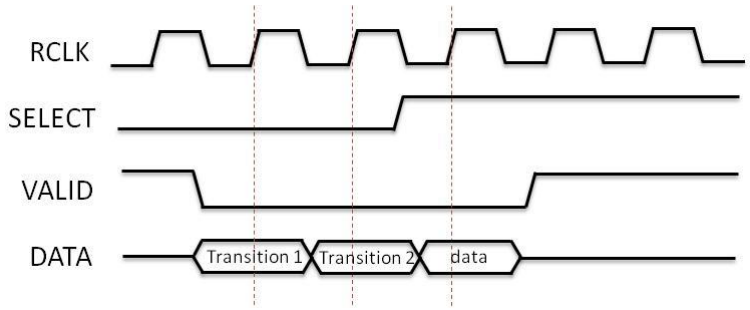


Figure 3.27 Chronogram of write/read status register protocol

- Send a command (except readout command): same as before, the S-ALTRO acts as slave and an external control acts as master. The operation is synchronous with the clock RCLK starting in the rising edge of the RCLK, on which VALID is sampled low. The SELECT line is held to low because no data is needed. In this case, just one cycle is needed to decode the instruction. Figure 3.28 shows an example of the chronogram.

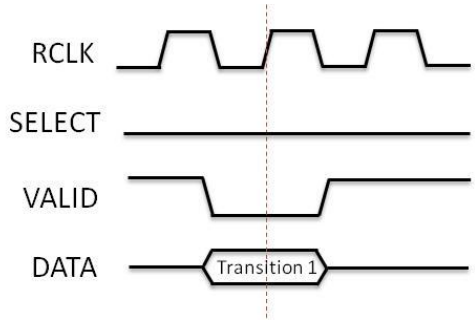


Figure 3.28 Chronogram of command protocol

- Send the readout command: the readout command is a special case where the S-ALTRO changes, after decoding the readout command, to be the master and the external control to be the slave. The operation of sending the readout command is the same as before, however in this case after 4 clock cycles the S-ALTRO pass to be the master and transmits the data trough the DATA bus validating it at the falling edge of the line SELECT. Figure 3.29 shows an example of the readout command.

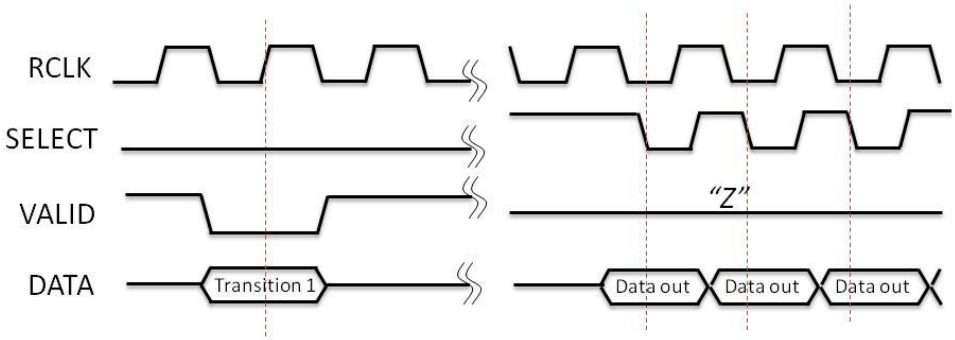


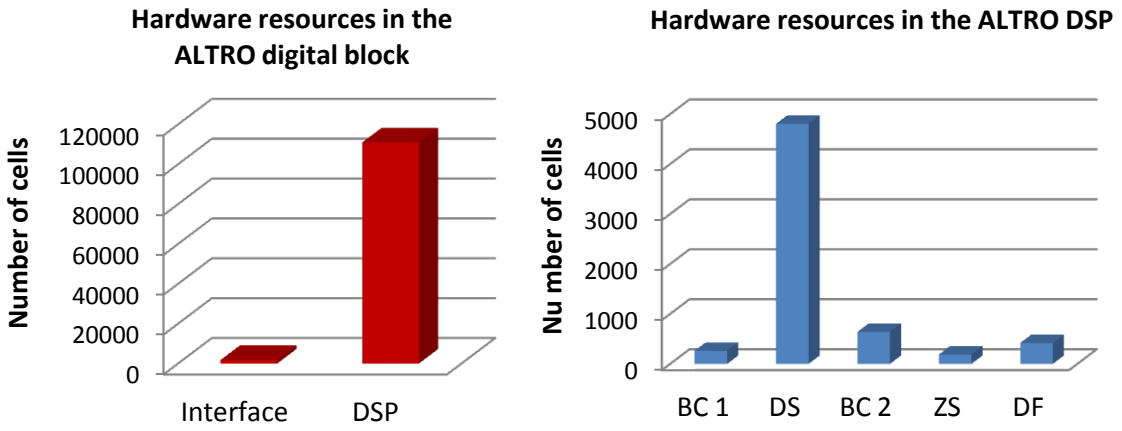
Figure 3.29 Readout command

Chapter 4 S-ALTRO Filter Optimization

4.1 Introduction

The S-ALTRO digital signal processing is an evolution of the ALTRO. This chapter presents the optimization in terms of power consumption, digital noise, higher degree of flexibility, architecture, stability of the BC1, the DS and the BC2 circuits. Moreover, these optimizations are compared with the ALTRO chip filters. Given its simplicity, the ZS block did not require any further optimization. While the DF proposed for the S-ALTRO chip, presented in chapter 3, has a completely different architecture.

The first step is to study the ALTRO hardware resources distribution. Figure 4.1 a) shows that the ALTRO digital circuitry is divided in two main blocks (Interface and DSP) with very different amount of hardware resources. Figure 4.1 b) shows the hardware resources distribution in the ALTRO DSP. The DS stands out as the main factor in terms of area and power consumption. Therefore, a great deal of effort was made to optimize this block.



a) Digital block *b) DSP chain*

Figure 4.1 ALTRO hardware resources

The first issue of any filter design is to understand how information is contained in the signals. In this particular case, the TPC signals contain the information in the time domain. The relevant information carried by the detector pulse in the time domain is the pulse time of arrival and amplitude. For these reasons, it is natural to design and optimize the filter in the time domain, e.g. using the step response function, instead of characterizing the circuit in the frequency domain.

One crucial aspect in the design and optimization of filter architectures is the choice between Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) filters. The TABLE 4-1 table summarizes different factors for both filters ([OPPEN]). These will be considered later in the chapter when making this decision.

TABLE 4-1 Summary IIR versus FIR

	IIR Filters	FIR Filters
Phase	difficult to control, no particular techniques available	linear phase always possible
Stability	can be unstable, can have limit cycles	always stable, no limit cycles
Order	less	More
History	derived from analog filters	no analog history
Others	polyphase implementation possible	can always be made causal

Moreover, one of the important figures of merit of a filter is the costs. This is measured in terms of hardware complexity, chip area and computational speed. These factors are more or less directly related to the order of the filter required to meet a given specification.

4.1.1 Power consumption

The power consumption of a circuit determines the quantity of heat it dissipates. This heat, the chip package and cooling system determine the number of channels that can be integrated in a single chip and the speed at which they are able to switch.

The design parameters to optimize the power consumption are:

- **Architecture level**: defines the choice of algorithm and amount of concurrency (parallel versus pipelined). This chapter presents the architecture level optimization of the DS, the main block in terms of power consumption and area. The number of cells in the ALTRO DS is more than three times all the other blocks put together.
- **(Micro-)Architecture level**: defines the IC solution (general purpose versus specific application). The very high integration requirement for the S-ALTRO chip makes the custom design (Application-Specific Integrated Circuit, ASIC) the only suitable solution for this application.
- **Circuit level**: defines transistor size, power supply and thresholds. Sizing and thresholds are only an option in customs design. However, in this ASIC design flow, these options are set by available libraries. This chapter presents a circuit level optimization for the full digital block based on the power supply reduction.

The optimizations at higher abstraction levels tend to have greater potential impact. For instance, circuit techniques can reach improvements in the 10-50% range, while architecture optimizations can have orders of magnitude power reduction. However, the optimizations within different levels are not independent of each other. For example, the choice of the power supply at the circuit level can lead to a change in the architecture level.

4.1.2 Digital noise

The implementation of digital filters introduces noise to the system. However, there is always a trade-off between hardware resources and noise optimization. There are two main sources of digital noise: coefficient quantization and round-off noise.

The coefficients in the digital filters are the quantized values of a rational system. The quantization moves the poles and zeros to new positions in the z-plane, modifying the original response of the filter. If the structure is very sensitive to these changes the filter may no longer fulfill the requirements.

On the other hand, the round-off noise is due to any truncation or rounding. This noise is for example introduced at the output of each multiplier, the product of two (b+1)-bit fixed-point binary numbers yields a multiplier (2b+1)-bit wide. Truncation or rounding is usually performed just after the multiplier.

In neither of these cases, round-off or truncation, a precise analysis using nonlinear systems is required. However, the most effective approach is to simulate the simplified linear system and measure its performance.

Another very important issue of linear filter models analysis is to choose the digital word length such that the digital system fulfills the requirements and at the same time requires a minimum amount of hardware resources. As explained in detail later, the DS determines the word length of the signal processing chain. The same word length is kept for the rest of the filters. This is a very important optimization with respect to the ALTRO chip, where a truncation was made after every filter.

4.2 Baseline Correction 1

Baseline correction 1 functionality was explained in chapter 3. This section presents the optimization of its hardware implementation.

Perturbations of different sources can affect the baseline of the input signal. Several of these perturbations often occur in combination with each other, creating complex effects in the signal baseline. One approach to correct this perturbation would be to design filters which cancel the frequencies of the perturbations. This method would not work in the cases where the signal has the same frequency components as the perturbation and in any case, would need high order filter ([MOTA]).

The most efficient way of correcting the baseline inside the processing window is to subtract from the input signal the computed baseline. Knowing the time dependency of the perturbation, the most appropriated solution is to correct this systematic effect by a look-up table where the correction values are stored and subsequently subtracted from the input signal. The stored values for baseline correction in the ALTRO chip have 1LSB accuracy ([ALTRO]). However, the baseline values are calculated with better accuracy than 1LSB. The accuracy is defined by the noise in the system. In particular, ALICE TPC can have accuracy in the baseline of 0.25 LSB. For this reason, in the S-ALTRO the subtraction is made with 0.25LSB accuracy, explained in detail in section 4.2.1.

On the other hand, to correct the baseline outside the processing window the ALTRO chip implements a fix IIR filter which makes the average of the input and the last baseline value without considering if the input is part of the pulse or of the baseline. An optimized architecture for the IIR is presented and explained in detail in section 4.2.2.

The block diagram of the S-ALTRO BC1 circuit is shown in Figure 4.2. *Time* signal comes from an internal counter which starts counting when the L1 trigger arrives and continues until the end of the time window. This signal is used to update the address in the memory for the subtraction or the test modes, explained in chapter 3. The input signal *Samples* comes directly from the ADC output. Whereas *SamplesIIR, Threshold Low, Threshold High* and *Acqn* are the parameters stored in a register for the IIR configuration, explained in detail later. On the other

hand, the *FPD* signal is a parameter stored in a register and it corresponds to the fixed value used in the subtraction mode. Finally, the output signal, *dout*, passes directly to the next filter stage without any truncation.

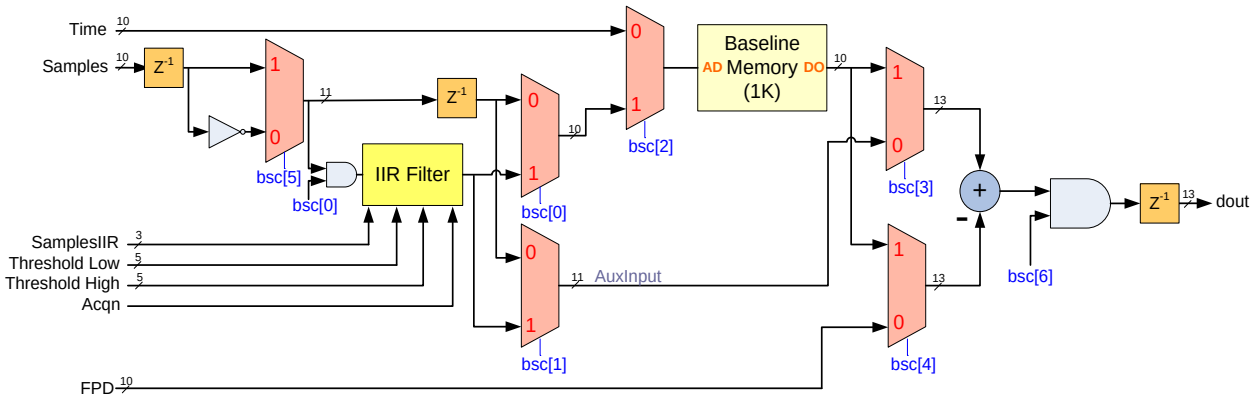


Figure 4.2 BC1 block diagram

Considering just the optimized BC1 hardware architecture in the ALTRO implementation, the design will have an increase of 7.9% in hardware resources (no area). As shown in Figure 4.1, this filter is very small compared to the full DSP. Therefore, the little hardware resources increase does not have an impact in the full chip. However, it will have the significant advantages presented in sections 4.2.1 and 4.2.2.

4.2.1 Digital noise optimization

In this case the subtraction of the baseline values is made with 0.25LSB accuracy, reducing the digital noise introduced in the system with respect to the ALTRO design. This is part of a circuit which performs the subtraction of a previous calculated baseline stored in the baseline memory, which is repeated many times in the BC1 circuit.

The optimization consists of using the baseline memory output divided by 4 (shifted to positions to the right) in case of the subtraction, although it keeps it aligned for the other functionalities. Figure 4.3 explains this concept.

It is important to stress that the 10 bit values stored in the memory for the mode “AuxInput – Baseline Memory” should have 0.25LSB accuracy. Consequently, the maximum value could go up to 255ADC counts. This covers the variation in the baseline, which for the ALICE TPC detector does not exceed 100 ADC counts. On the other hand, a fix pedestal value (FPD) between 0 and 1023 ADC counts can be used simultaneously in case that the baseline has an offset abode 255ADC counts.

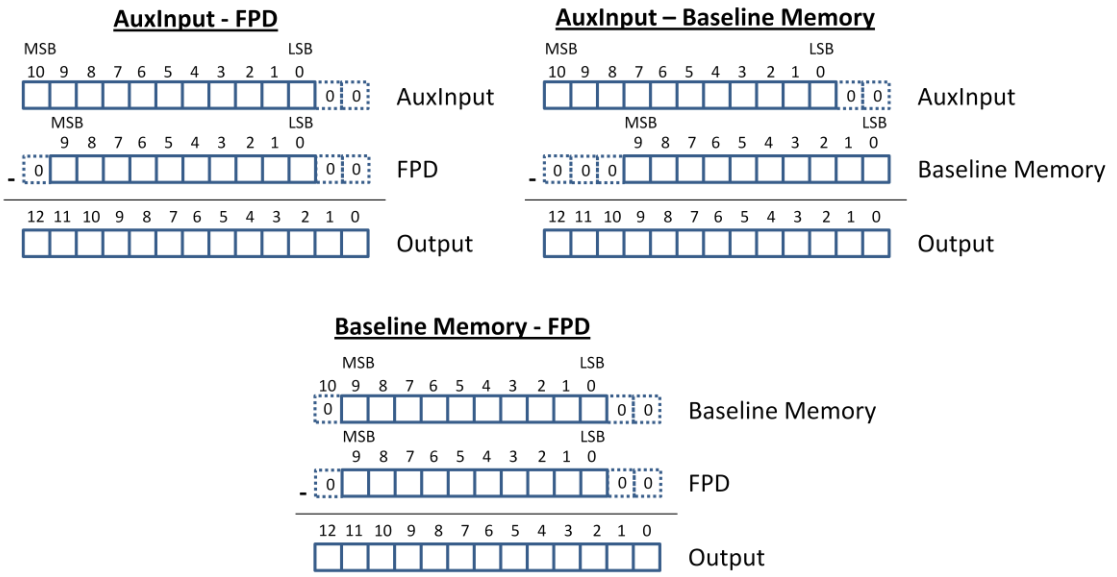


Figure 4.3 Diagram of the baseline memory shifts in the BC1

A simplified model of the noise introduced with the baseline subtraction is shown in Figure 4.4. In this model, the ADC noise is also considered. The filter noise is treated as an additive noise signal. This analysis is based in the following assumptions ([OPPEN]):

1. The error sequence er[n] is a sample of a stationary random process.
2. The error sequence is uncorrelated with the sequence x[n].
3. The random variables of the error process are uncorrelated.
4. The probability distribution of the error process is uniform over the range of quantization error.

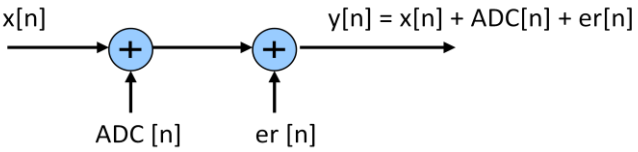


Figure 4.4 Additive noise model for the subtraction mode

The ADC and digital noise variance are defined in eq. 4.4. The total digital noise introduced in the subtraction mode is defined in eq. 4.5. The signal variance in the circuit is defined in eq. 4.6. A common measure of the degradation of a signal by additive noise is the signal-to-noise ratio (SNR) which is defined as the ratio of signal variance to noise variance. It is expressed in decibels (db), see eq. 4.7. In conclusion, the SNR in the optimized BC1 has increased in 1.5db, see Figure 4.5.

$$\sigma^2_{ADC} = \frac{2^{-2\cdot bits}}{12} \cdot (V_{max} - V_{min})^2 \quad ; \quad \sigma^2_{er} = \frac{2^{-2\cdot bits}}{12} \qquad \text{(eq. 4.4)}$$

$$\sigma^2_{y\_noise} = \sigma^2_{ADC} + \sigma^2_{er} \qquad \text{(eq. 4.5)}$$

$$\sigma_x^2 = \frac{1}{12} \cdot (V_{max} - V_{min})^2 \qquad \text{(eq. 4.6)}$$

$$SNR(db) = 10 \cdot \log\left(\frac{\sigma_x^2}{\sigma_{y\_noise}^2}\right) \qquad \text{(eq. 4.7)}$$

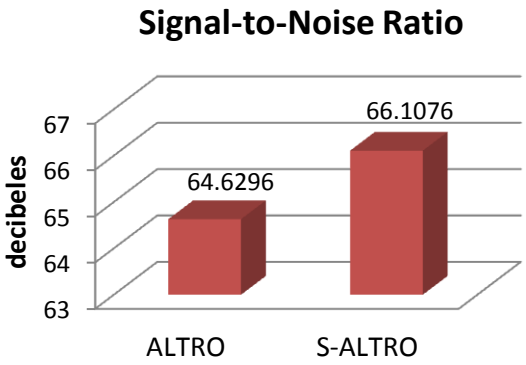


Figure 4.5 Signal-to-Noise Ratio comparison

4.2.2 Flexibility optimization

As explained in the introduction, there are two possible architectures to implement filters: IIR or FIR. In this case, the expected baselines are rather small variations in amplitude and very low frequency components. Therefore, the main parameter to define the filter is the hardware efficiency. As summarized in the introduction, IIR filters are usually lower order and, therefore, more hardware efficient. Moreover, a first order filter is enough to follow these baselines outside the processing window. The stability is assured because the poles are always inside the unity circle independently of the configuration (see eq. 4.10).

This IIR filter calculates the baseline outside of the processing window and has been optimized to choose the time response of the filter. Therefore, it is adaptable to different perturbations.

On the other hand, a double threshold is introduced to avoid pulses in the calculation of the baseline. This is very important issue in high occupancy applications, since pulses can arrive outside of the acquisition window. It determines hence, when the window for the adaptive baseline correction is computed and updated. When the input signal is out of the boundaries given by the double threshold window, the baseline value is frozen. In this double threshold scheme, the output signal is compared with an upper and lower bound, programmable per channel.

The IIR filter is divided in two parts, the double threshold scheme and the proper IIR filter. See Figure 4.6. Where, *DataIn* and *DataOut* are the input and output of the filter respectively. *Acqn* determines the processing window. *N* defines the speed of the filter, low N approximates faster to the baseline although the calculation is less accurate and vice versa. *Threshold Low* and *Threshold High* fix the double threshold bounds and *Valid* disables the double threshold scheme for a fixed period of 12 sampling clock cycles after a reset to make sure that the baseline value is inside the double threshold scheme.

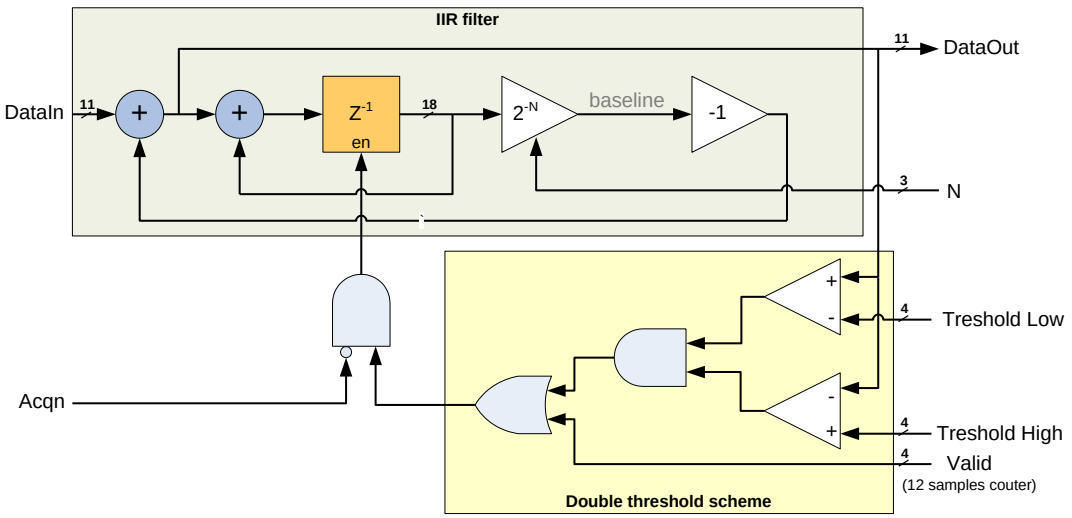


Figure 4.6 IIR filter with double window enable

The IIR filter equations are eq. 4.8 and eq. 4.9. The respective transfer functions are eq. 4.10 and eq. 4.11.

$$baseline[n] = \frac{1}{2^N} \cdot DataIn[n] + \frac{(2^N-1)}{2^N} \cdot baseline[n-1] \qquad \text{(eq. 4.8)}$$

$$DataOut[n] = DataIn[n] - baseline[n] \qquad \text{(eq. 4.9)}$$

$$\frac{baseline[n]}{DataIn[n]} = G(z) = \frac{\frac{1}{2^N}}{1-\frac{(2^N-1)}{2^N} \cdot z^{-1}} \qquad \text{(eq. 4.10)}$$

$$\frac{DataOut[n]}{DataIn[n]} = H(z) = 1 - G(z) = \frac{\frac{(2^N-1)}{2^N} - \frac{(2^N-1)}{2^N} \cdot z^{-1}}{1-\frac{(2^N-1)}{2^N} \cdot z^{-1}} \qquad \text{(eq. 4.11)}$$

Figure 4.7 and Figure 4.8 show the step response of the IIR filter for different *N*. Clearly, the response time (in samples) of the filter depends on *N*, larger *N* increases the response time and the accuracy calculation (less digital noise). This parameter should be set depending on the baseline in the application. If *N*=1 the IIR has the same behavior than the ALTRO AUTOCAL ([ALTRO]).

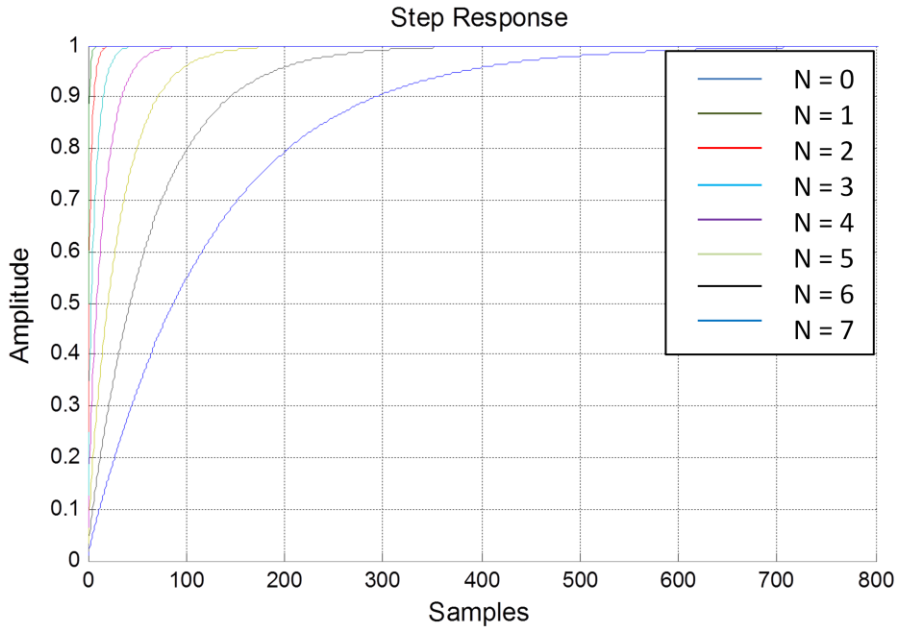


Figure 4.7 Step response of BC1 IIR filter

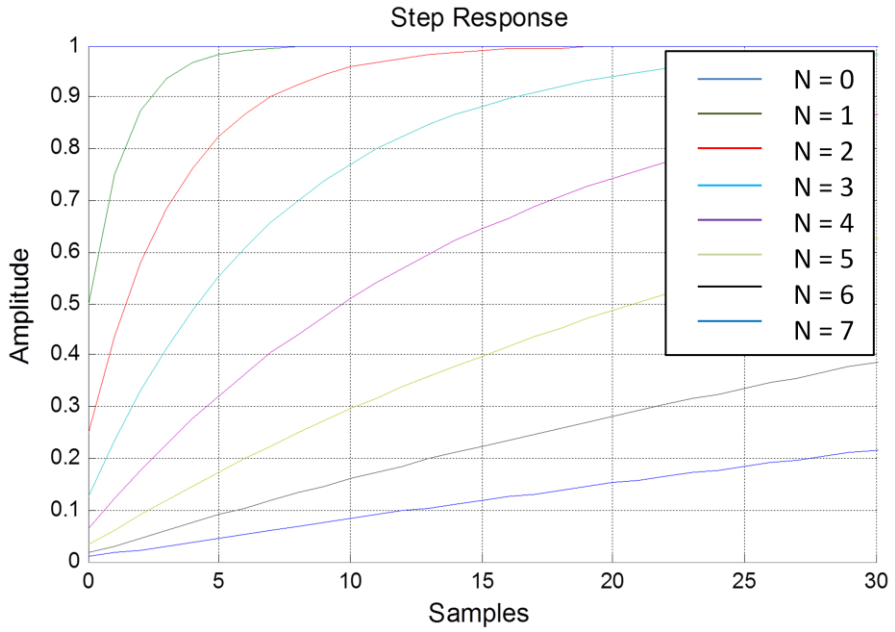


Figure 4.8 Zoom of the step response of BC1 IIR filter

4.3 Digital Shaper

As mentioned in the introduction, the DS is the main filter in terms of area and power consumption in the digital signal processing.

Section 4.3.1 analyzes many filter topologies. Later, section 4.3.2 presents the conclusions of the topology analyses. Finally, section 4.3.3 shows the optimization of the DS with respect to its predecessor.

4.3.1 Topology study

The filter design methodology results in a particular system function which must be implemented with certain architecture. Usually the criterion is based on least hardware resources. However, there are other parameters such as output noise generated or sensitivity to coefficient variations to be taken into account when choosing optimum filter architecture.

In this section, an analysis of the basic IIR architectures to perform pole-zero cancellation filter is presented. There are two basic forms of IIR filters, direct form I and direct form II. The IIR direct form I and direct form II represent a linear time-invariant system where the rational system function is shown in eq. 4.12. N and M represent the order of the poles and zeros respectively. The hardware representations will be shown in the next section.

$$H(z) = \frac{-\sum_{k=0}^{M} b_k z^{-k}}{1+\sum_{k=1}^{N} a_k z^{-k}} \qquad \text{(eq. 4.12)}$$

However, some hardware transformations can be made keeping the same system function between input and output. An example of these hardware transformations are the transposed forms shown in the next section. Each rearrangement introduces a different computational algorithm for the same system.

At the same time, the systems can be divided using two methods, cascade or parallel. The cascade form factors the numerator and denominator polynomials and the parallel form divides the system as a partial fraction expansion. However, cascade form coefficients are directly the poles-zeros and the system is less sensitive to coefficient quantization ([OPPEN]). Simulations have shown that a cascade form of first or second order filters fulfill the sensitivity to coefficient requirements.

A new approach based on trapezoidal and triangular filters (FIR+IIR) is reviewed and compared with the typical IIR pole-zero cancellation approach.

The next topology analyses will focus on two main factors, hardware resources and output noise.

4.3.1.1 First order IIR classical architectures

This section studies the different first order architectures for IIR filters. The first order filter system function is a particular case of eq. 4.12, where M=N=1. Therefore, the system function for a first order filter is shown in eq. 4.13.

$$H(z) = \frac{-b_0 - b_1 \cdot z^{-1}}{1+a_1 \cdot z^{-1}} \qquad \text{(eq. 4.13)}$$

As explained in the introduction, truncation or rounding is usually performed just after the multipliers. In this system, the products are truncated before the addition due to hardware simplicity. Another important consideration in the analyses is that the parameters of the DS for this application are positive and close to each other in value.

Hereafter it is shown the study of the four most popular IIR filter architectures: direct form I, direct form II, transposed direct from I and transposed direct form II.

- Direct form I

Figure 4.9 shows the direct form I architecture of eq. 4.13.

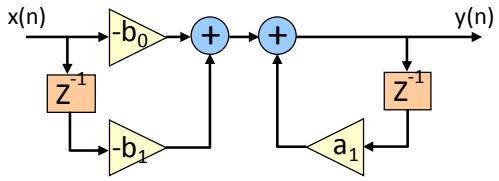


Figure 4.9 Direct form I block diagram

This architecture needs three multipliers, two adders and two registers.

Considering the same assumptions as in the section 4.2.1 and the simplified linear noise model of Figure 4.10, a noise analysis is performed. There are three noise sources $er_{b0}[n]$, $er_{b1}[n]$ and $er_{a1}[n]$. However, analyzing the circuit revealed that all the noise sources are injected between the part of the system implementing the zeros (left) and the part implementing the pole (right). Therefore, the noise sources can be added in one single noise source, eq. 4.14. In this architecture, the noise sources are filtered just for the pole.

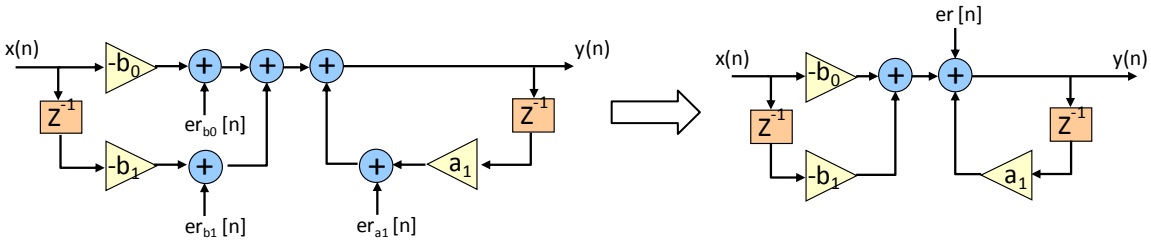


Figure 4.10 First order IIR direct form I linear noise model

$$er[n] = er_{b0}[n] + er_{b1}[n] + er_{a1}[n] \qquad \text{(eq. 4.14)}$$

The impulse response corresponding to the pole in the system is defined as $h_{ef}[n]$. Following the procedure explained in detail in ([OPPEN]), the total noise variance and mean at the output are defined in eq. 4.15 and eq. 4.16 respectively. Where, as mention before M=N=1.

$$\sigma_f^2 = (M+1+N)\cdot\frac{2^{-2B}}{12}\cdot\sum_{n=-\infty}^{\infty}\left|h_{ef}[n]\right|^2 = 3\cdot\frac{2^{-2B}}{12}\cdot\frac{1}{1-{a_1}^2} \qquad \text{(eq. 4.15)}$$

$$m_f = (M+1+N)\cdot -\frac{2^{-2B}}{2}\cdot \sum_{n=-\infty}^{\infty}\left|h_{ef}[n]\right| = 3\cdot\frac{2^{-2B}}{2}\cdot\frac{1}{1-a_1} \qquad \text{(eq. 4.16)}$$

Finally, the total power noise at the output is defined by eq. 4.17. Total power noise equation remains the same for all the architectures.

$$P_f = \sigma_f^2 + m_f \qquad \text{(eq. 4.17)}$$

- Direct form II

Figure 4.11 shows the direct form II architecture of eq. 4.13.

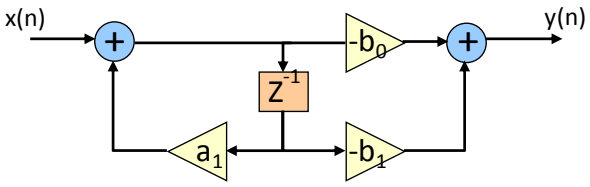


Figure 4.11 Direct form II block diagram

This architecture needs three multipliers, two adders and one single register. However, there is a critical aspect in this architecture. The pole at the input has a positive feedback, having an increase of the internal values rather fast. As explained in detail later, this could trigger the need for an increase in the number of bits in the data path and therefore, cause a significant increase of hardware resources without any other advantage.

Noise analysis is carried out with the same procedure as for the direct form I. However, the noise sources are placed at different positions. The three noise sources injected are grouped one at the input and two at the output. In this case, er_a is filtered by the full system (one pole and two zeros), while er_b is directly at the output.

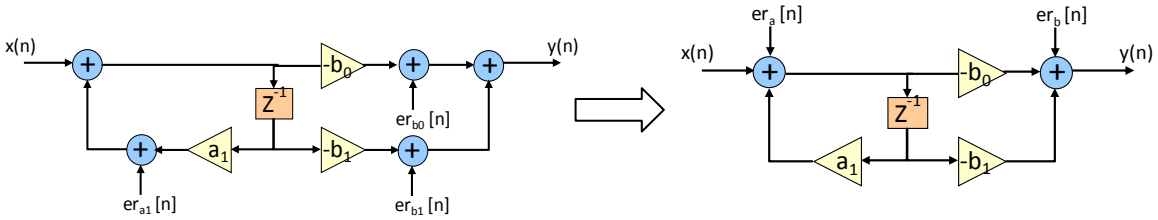


Figure 4.12 First order IIR direct form II linear noise model

The impulse response corresponding to the pole and two zeros is defined as h[n]. The total noise variance and mean at the output are defined in eq. 4.18 and eq. 4.19 respectively.

$$\sigma_f^2 = N\cdot\frac{2^{-2B}}{12}\cdot\sum_{n=-\infty}^{\infty}|h[n]|^2 + (M+1)\frac{2^{-2B}}{12} =$$

$$= \frac{2^{-2B}}{12}\cdot\frac{{b_1}^2 - 2\cdot a_1\cdot b_1\cdot b_0 + {b_0}^2}{1-{a_1}^2} + 2\cdot\frac{2^{-2B}}{12} \qquad \text{(eq. 4.18)}$$

$$m_f = N \cdot -\frac{2^{-2B}}{2} \cdot \sum_{n=-\infty}^{\infty} |h[n]| - (M+1)\frac{2^{-2B}}{2} =$$

$$= \frac{2^{-2B}}{2} \cdot \frac{b_1+b_0}{1+a_1} - 2 \cdot \frac{2^{-2B}}{2} \qquad \text{(eq. 4.19)}$$

- Transposed direct form I

Figure 4.13 shows the transposed direct form I architecture of eq. 4.13.

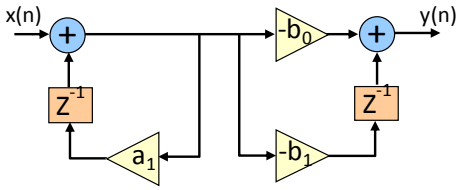


Figure 4.13 Transposed direct form I

This architecture needs the same hardware resources as its original (direct form I). However, this architecture has the same problem as the direct form II. The pole at the input has a positive feedback with the potential problem of overflow in internal nodes.

The same noise analysis as in the other architectures has been followed. In this case, the er_{a1} is filtered by the full system, er_{b1} is filtered just for one zero and er_{b0} is directly at the output.

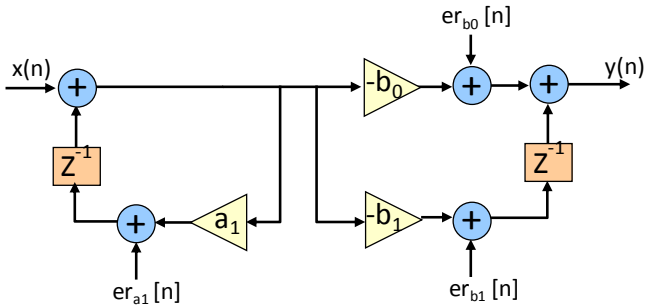


Figure 4.14 First order IIR transposed direct form I linear noise model

The impulse response corresponding to the zero at b1 is defined as $h_{ef2}[n]$. The total noise variance and mean at the output are defined in eq. 4.20 and eq. 4.21 respectively.

$$\sigma_f^2 = (N+M+1) \cdot \frac{2^{-2B}}{12} \cdot \sum_{n=-\infty}^{\infty} |h[n]|^2 + M \cdot \frac{2^{-2B}}{12} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef2}[n]\right|^2 + \frac{2^{-2B}}{12} =$$

$$= 3 \cdot \frac{2^{-2B}}{12} \cdot \frac{{b_1}^2 - 2 \cdot a_1 \cdot b_1 \cdot b_0 + {b_0}^2}{1-{a_1}^2} + \frac{2^{-2B}}{12} \cdot (1+b_1^2) + \frac{2^{-2B}}{12} \qquad \text{(eq. 4.20)}$$

$$m_f = (N+M+1) \cdot -\frac{2^{-2B}}{2} \cdot \sum_{n=-\infty}^{\infty} |h[n]| + M \cdot -\frac{2^{-2B}}{2} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef2}[n]\right| - \frac{2^{-2B}}{2} =$$

$$= 3 \cdot \frac{2^{-2B}}{2} \cdot \frac{b_1+b_0}{1-a_1} - \frac{2^{-2B}}{2} \cdot (1+b_1) - \frac{2^{-2B}}{2} \qquad \text{(eq. 4.21)}$$

- Transposed direct form II

Finally, Figure 4.15 shows the transposed direct form II architecture of eq. 4.13.

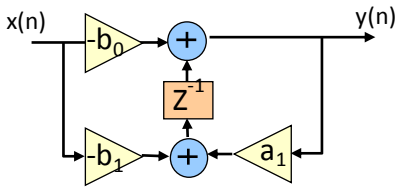


Figure 4.15 Transposed direct form II

This architecture needs the same hardware resources as its original (direct form II). However, this architecture does not have a positive feedback in the input. This fact significantly reduces the absolute values of the internal nodes, as shown in simulations later.

In this case, the noise sources can be grouped in two. The er_0 is filtered by the pole and er_1 is filtered by one pole and one zero.

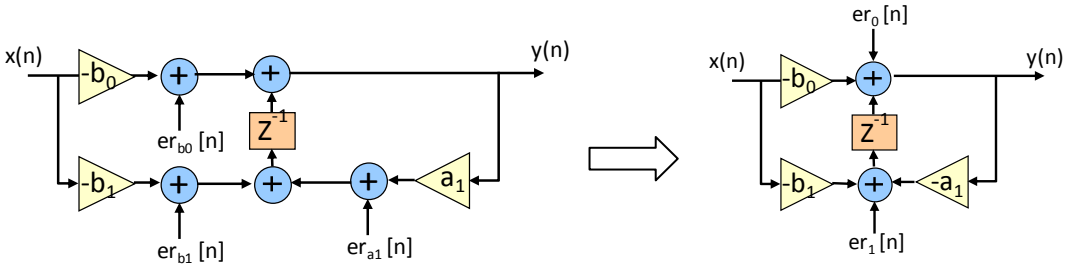


Figure 4.16 First order IIR transposed direct form II linear noise model

The impulse response corresponding to the zero at b1 is defined as $h_{ef3}[n]$. The total noise variance and mean at the output are defined in eq. 4.22 and eq. 4.23 respectively.

$$\sigma_f^2 = \frac{2^{-2B}}{12} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef}[n]\right|^2 + (M+N)\frac{2^{-2B}}{12} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef3}[n]\right|^2 =$$

$$= \frac{2^{-2B}}{12} \cdot \frac{1}{1-{a_1}^2} - 2 \cdot \frac{2^{-2B}}{12} \cdot \frac{b_1^2}{a^2-1} \qquad \text{(eq. 4.22)}$$

$$m_f = -\frac{2^{-2B}}{2} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef}[n]\right| - (M+N)\frac{2^{-2B}}{2} \cdot \sum_{n=-\infty}^{\infty} \left|h_{ef3}[n]\right| =$$

$$= \frac{2^{-2B}}{2} \cdot \frac{1}{1+{a_1}^2} + 2 \cdot \frac{2^{-2B}}{2} \cdot \frac{b_1}{a_1+1} \qquad \text{(eq. 4.23)}$$

4.3.1.2 Second order IIR filters

This section discusses the advantages and disadvantages of the second order IIR filters. The second order filter equation is a particular case of eq. 4.12 where M=N=2. The system function for a second order filter is shown in eq. 4.24.

$$H(z) = \frac{-b_0 - b_1 \cdot z^{-1} - b_2 \cdot z^{-2}}{1 + a_1 \cdot z^{-1} + a_2 \cdot z^{-2}} \qquad \text{(eq. 4.24)}$$

This system function allows the use of complex poles-zeros in the digital shaper which would give an extra degree of freedom in the choice of the position of the poles and zeros. The first order filters have the obvious limitation that poles and zeros can only lie in the real axis rather than occupying the full circle. The choice of poles-zeros in both cases is marked in red in the Figure 4.17.

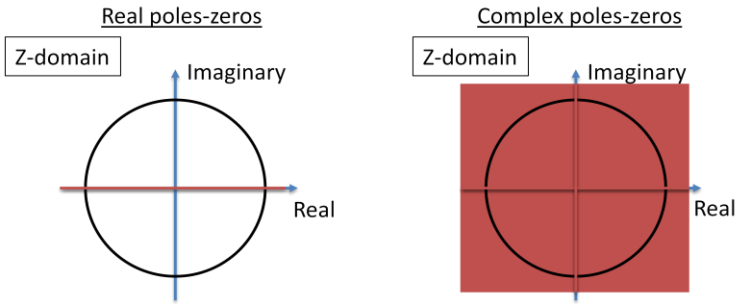


Figure 4.17 Pole-zero placements for digital filters

Same case than for the first order IIR filters, there are a set of different hardware architectures whose implement the system function of eq. 4.24. However, hereafter the different filter architectures will not be discussed again. Just the features of the second order filters for certain architecture will be presented, for instance, a transposed direct form II is used for the comparison.

Configuration A is shown in Figure 4.18 and corresponds to a cascade of 2 first orders IIR transposed direct form II filter. Configuration B is shown in Figure 4.19 and corresponds to a second order IIR transposed direct form II filter.

The number of registers and multipliers is the same for both architectures. However, the number of adders is bigger in the configuration A. Following the assumption that the first order poles and zeros are positive and close to the unity ([MOTA]), the second order parameters b_1 and a_1 are bigger than the unity ($b_1=b_{11}+b_{21}$, $a_1=a_{11}+a_{21}$). Therefore, the data width would increase. Consequently, the overall hardware resources in the configuration B increase with respect to the configuration A.

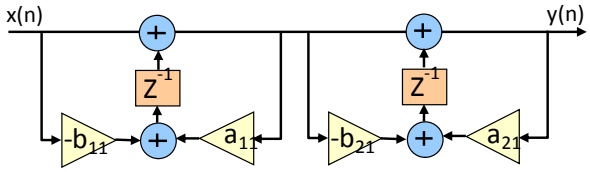


Figure 4.18 Cascade of 2 first order IIR transposed direct form II

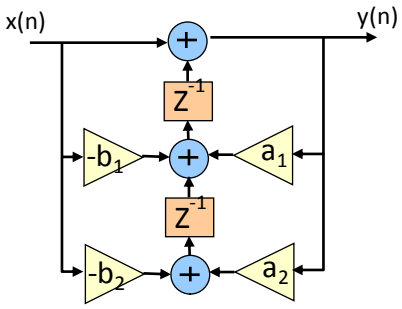


Figure 4.19 Second order IIR transposed direct form II

Same round-off noise analysis than in the last section has been followed. From the results of the eq 4.22 and eq 4.23, the total noise variance and mean at the output of the configuration A are defined in eq. 4.25 and eq. 4.26 respectively.

$$\sigma_f^2 = 2 \cdot \frac{2^{-2B}}{12} \cdot \frac{1}{1-{a_1}^2} - 4 \cdot \frac{2^{-2B}}{12} \cdot \frac{b_1^2}{a^2-1} \qquad \text{(eq. 4.25)}$$

$$m_f = 2 \cdot \frac{2^{-2B}}{2} \cdot \frac{1}{1+{a_1}^2} + 4 \cdot \frac{2^{-2B}}{2} \cdot \frac{b_1}{a_1+1} \qquad \text{(eq. 4.26)}$$

While, from the same equations, the total noise variance and mean at the output of the configuration B are defined in eq. 4.27 and eq. 4.28.

$$\sigma_f^2 = \frac{2^{-2B}}{12} \cdot \frac{1}{1-{a_1}^2} - 4 \cdot \frac{2^{-2B}}{12} \cdot \frac{b_1^2}{a^2-1} \qquad \text{(eq. 4.27)}$$

$$m_f = \frac{2^{-2B}}{2} \cdot \frac{1}{1+{a_1}^2} + 4 \cdot \frac{2^{-2B}}{2} \cdot \frac{b_1}{a_1+1} \qquad \text{(eq. 4.28)}$$

Eq. 4.25-28 indicates that the second order IIR transposed direct form II would reduce the round-off noise. Nevertheless, it would increase the quantization noise due to the higher order ([OPPEN]).

The second order filter can implement the same system function of a cascade of 2 first order filters using these parameter relations: $b_1=b_{11}+b_{21}$, $b_2=b_{11}\cdot b_{21}$, $a_1=a_{11}+a_{21}$, $a_2=a_{11}\cdot a_{21}$. However, a new method of parameter calculation should be investigated to find the optimum complex poles and zeros. A first study has shown that for TPC applications there is not a big advantage of using complex poles-zeros because the poles and zeros are quite close to the unity. Consequently, the use of complex poles-zeros cannot provide greater flexibility.

Finally this architecture was ruled out from the possible implementations because it does not introduce substantial advantages, it increases the hardware resources, it makes the calculation of the filter parameters complicated and it introduces extra quantization errors due to the second order stage.

4.3.1.3 FIR filters. New filter concepts for the DS

Finally, two filters are briefly presented which are becoming very popular in the latest digital signal processing design for HEP with field-programmable gate arrays (FPGAs).

These designs are a combination of FIR+IIR filters. There are many topologies; however this section just focuses on two filters, the triangular filter for timing information and the trapezoidal filter for the maximum energy calculation. See Figure 4.20.

Figure 4.20 Typical output of triangular and trapezoidal filters

- Triangular filter: the timing information is contained at the maximum energy directly from the crossing of both straight lines. Figure 4.21 shows the block diagram of a typical triangular filter, presented in ([GERACI]). *L* represents the number of taps on each side of the triangular output.

- Trapezoidal filter: the energy information is contained in the flat top. Figure 4.22 shows the block diagram of a typical trapezoidal, presented in ([GERACI]). *L* represents the numbers of taps on each side and *T* the taps on the top.

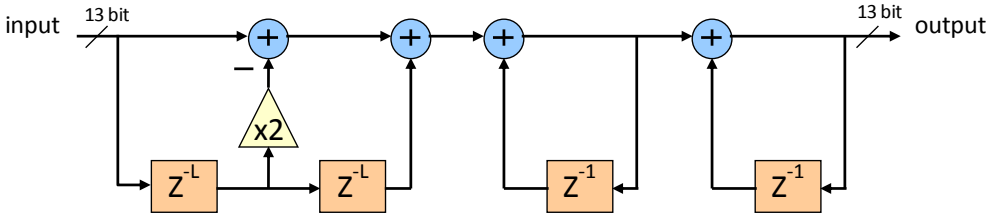


Figure 4.21 Triangular filter block diagram

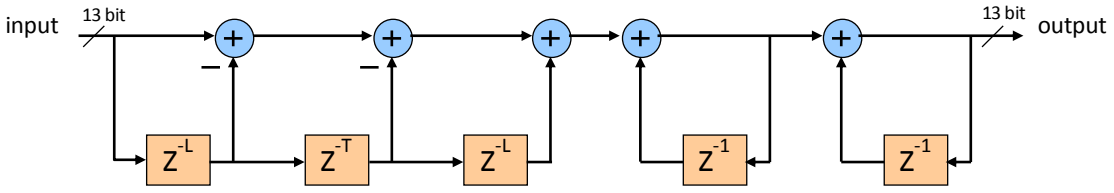


Figure 4.22 Trapezoidal filter block diagram

These filters are a plausible solution for programmable logic system where the number of taps could be adjusted for each application or where there is not a very strong area/power limitation. However for an ASIC like S-ALTRO, the amount of hardware resources required by these architectures is too large and its integration is not feasible.

4.3.2 Conclusions of the topology study

Even if some conclusions were made in the last section, hereafter are summarized the main considerations that led to the choice of the architecture of the digital shaper.

Triangular and trapezoidal filters were ruled out from the possible implementations because the large amount of hardware resources required does not match with the S-ALTRO strict area and power consumption requirements.

The second order IIR filter has the main drawback of an increase in the hardware resources and big complexity in the calculation of the complex poles-zeros, without significant improvement in the output.

Finally, a methodic analysis of the first order IIR architectures was made. Starting from the hardware resources point of view, a priori looks like there are no big differences between the architectures. However, there is a very important aspect to remark. The positive feedback in the input of direct form II and transposed direct form I makes those architectures very sensitive to overflow errors for this application. The consequence is an increase of the hardware resources without gaining any extra advantage. On the other hand, the output noise analyses of the transposed direct form II and the direct form I conclude that the transposed direct form II introduces less noise to the system.

It has been concluded that the transposed direct form II is the optimum architecture for the DS in this application. Next section shows in detail the optimization of the DS with respect to the previous version.

4.3.3 DS Optimization

The DS in the ALTRO chip was implemented by a cascade of 3 first order IIR direct form II filters ([MOTA]). Each stage of the filter is controlled by two coefficients (Li and Ki, with i = 1, 2 and 3), which are programmable and can take any value in the interval [0:1[.

The filter implemented has, in the Z-domain, the transfer function given in eq. 4.29.

$$H(z) = \frac{1-L_1 \cdot z^{-1}}{1-K_1 \cdot z^{-1}} \cdot \frac{1-L_2 \cdot z^{-1}}{1-K_2 \cdot z^{-1}} \cdot \frac{1-L_3 \cdot z^{-1}}{1-K_3 \cdot z^{-1}} \qquad \text{(eq. 4.29)}$$

Figure 4.23 shows the hardware implementation of the ALTRO DS. The input and output of the filter are 11-bits width in 2's complement format, but all the computations are done in 18-fix-point arithmetic. The extra five MSB were added to avoid the overflow error and two extra fractional bits to minimize the round-off noise ([MOTA]).

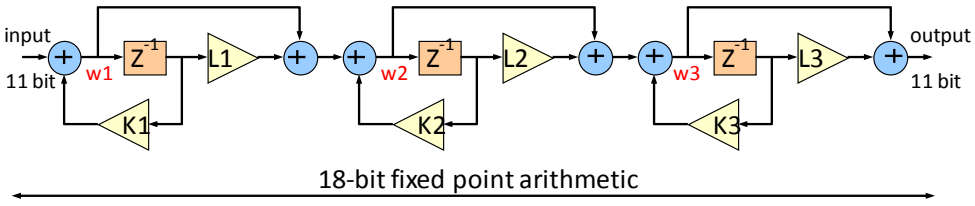


Figure 4.23 ALTRO DS architecture

This hardware implementation is composed of 3 registers, 6 adders and 6 multipliers, 18-bits wide. This data path width has a strong impact in the multiplier complexity (e.g. an 18-bits wide multiplier has almost twice the number of gates of a 13-bits one).

As explained, the DS filter accounts for a large fraction of the total digital power consumption. It is thus very important to find an equivalent implementation of the filter that could be more power efficient. Since the power consumption is proportional to the number of active gates, the possibility of implementing the same transfer function using a different architecture with narrower data path without paying additional penalty on overflow or round off noise was studied.

4.3.3.1 Power consumption optimization

An alternative hardware implementation of eq. 4.29 is presented in Figure 4.24. The DS is now implemented by a cascade of 3 first order IIR transposed direct form II filters.

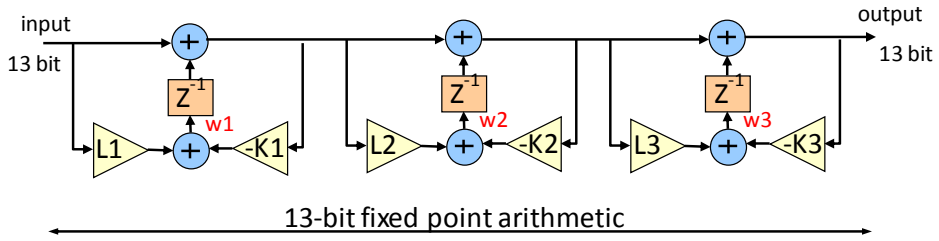


Figure 4.24 Proposed DS architecture

In this alternative implementation, the input and output of the filter are 13-bits wide in 2's complement format, and all the computations are done in 13-bit fix-point arithmetic. Two fraction bits are used to minimize the round off noise, as explained in detail in 4.3.3.3 section. Moreover, this architecture needs no additional bits for overflow handling for the type of signal shapes produced by the TPC detector, studied in detail in 4.3.3.2 section.

Verilog code was written to describe the two DS filters. This was then synthesized with Synopsys ([SYNOP]). Figure 4.25 shows the comparison in terms of number of gates for the two circuits. As a result of the narrower data path of the proposed architecture, the number of gates is reduced to approximately half. Consequently, silicon area is reduced by the same factor.

On the other hand the switching activity in the system for an input with 10% occupancy is reduced roughly to half, reducing the power consumption to the same factor.

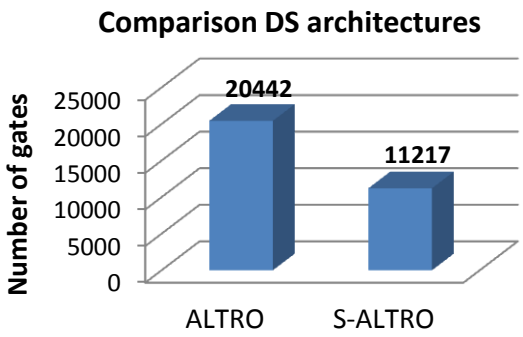


Figure 4.25 Number of Gates for the DS architectures

Considering just the new DS architecture in the ALTRO implementation, the hardware resources of the digital block would have decreased to 2/3.

A very important advantage of the proposed architecture is that the procedure to calculate the filter parameters could be the same as the ones used for the ALTRO chip. All the research about how to calculate efficiently the parameters in the ALTRO DS ([ROSSEG]) are totally compatible for this new architecture.

4.3.3.2 Overflow analysis

The possibility of overflow is an important consideration in the implementation of IIR systems using fixed-point arithmetic. Using a set of measurement data acquired on a TPC prototype ([MOTA]), the probability of overflow can be investigated. Figure 4.26 and Figure 4.27 show the signal values of the nodes (w1, w2, w3) for the architectures of Figure 4.23 and Figure 4.24, respectively.

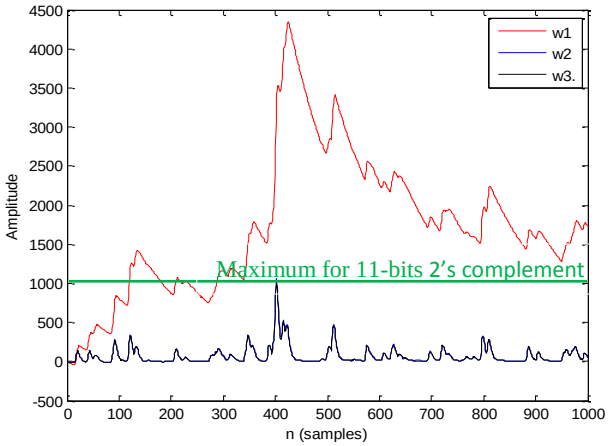


Figure 4.26 Nodes in the ALTRO DS

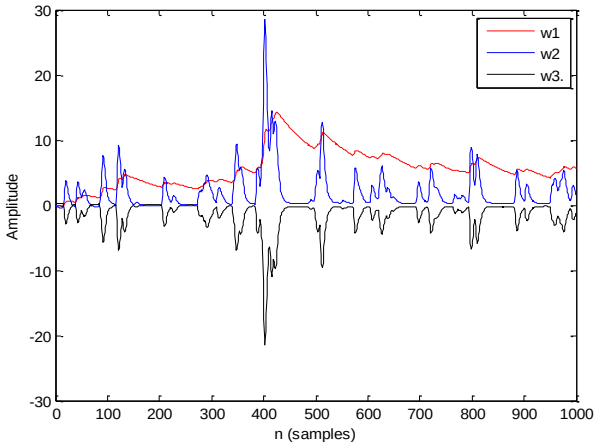


Figure 4.27 Nodes in the S-ALTRO DS

Figure 4.26 shows that in the original DS architecture the first node (w1) has sometimes values above the maximum amplitude range (11-bits 2's complement amplitude range), requiring thus 5 extra magnitude bits to avoid overflow ([MOTA]). While Figure 4.27 shows that in the proposed architecture the values in the nodes are always below the maximum. Therefore, for typical TPC data there is no overflow error.

The reason for the different overflow behavior lies in the details of the two architectures. In the ALTRO DS, the value in the nodes (w1, w2, w3) may increase rapidly because positive feedback is used in every stage of the filter (see Figure 4.23). However, in the second architecture, the feedback is always negative (see Figure 4.24) constraining the growth of the signal.

4.3.3.3 Digital noise analysis

The S-ALTRO and ALTRO DS architectures are divided in a cascade of first order filters. Therefore, there is not an increase in the quantization errors.

On the other hand following the assumptions of the section 4.2, a simple linear-noise analysis was made to characterize the round-off noise generated in the filter. In this model the ADC noise is also considered. The simple linear-noise model presented in Figure 4.28 allows to characterize the noise generated in the system by averages such as the mean and variance and to determine how these averages are modified by the system.

The ADC and round-off noise variance are defined in eq. 4.30 and eq. 4.31, respectively. Each noise source is filtered by the system. The output noise variance is defined in eq. 4.32. The signal variance is defined in eq. 4.33. While, the output signal variance is defined in eq. 4.34. Finally, the SNR is defined in eq. 4.35.

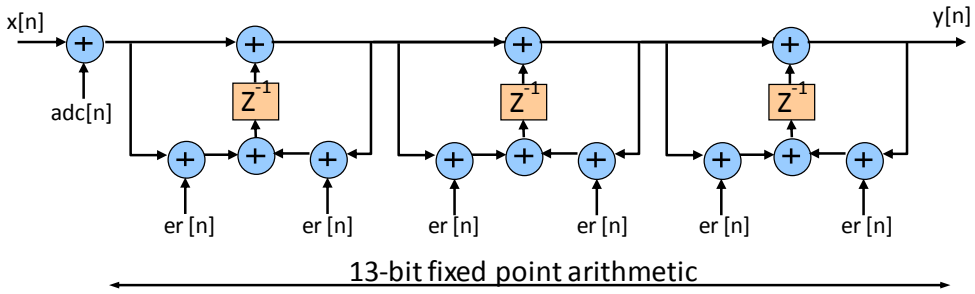


Figure 4.28 ALTRO DS linear-noise model

$$\sigma^2_{ADC} = \frac{2^{-2\cdot bits}}{12} \cdot (V_{max} - V_{min})^2 \qquad \text{(eq. 4.30)}$$

$$\sigma^2_{er} = \frac{2^{-2\cdot bits}}{12} \cdot (V_{max} - V_{min})^2 \; ; \qquad \sigma^2_{ei} = \sum_{i=0}^{n} \sigma^2_{er} \qquad \text{(eq. 4.31)}$$

$$\sigma^2_{y\_noise} = \sigma^2_{ADC} \cdot \sum_{n=-\infty}^{\infty} |h[n]|^2 + \sigma^2_{ei} \cdot \sum_{n=-\infty}^{\infty} |h_e[n]|^2 \qquad \text{(eq. 4.32)}$$

$$\begin{cases} \sigma_x^2 = \frac{1}{12} \cdot (V_{max} - V_{min})^2 & \text{(eq. 4.33)} \\ \sigma_y^2 = \sigma_x^2 \cdot \sum_{n=-\infty}^{\infty} |h[n]|^2 & \text{(eq. 4.34)} \end{cases}$$

$$SNR(db) = 10 \cdot \log\left(\frac{\sigma_y^2}{\sigma_{y\_noise}^2}\right) \quad \text{(eq. 4.35)}$$

Figure 4.29 shows the trend of the SNR as a function of the word length. The curve tends to a SNR of the 66.22 dB, which is the theoretical SNR predicted for the 10-bit ADC, with an increasing number of bits. It can be seen from the graph that almost no improvement is obtained for words wider than 13-bit. A good trade-off between accuracy and circuit complexity can thus be achieved with a 13-bit word, that is, by using 11 bits to represent the magnitude plus two fractional bits.

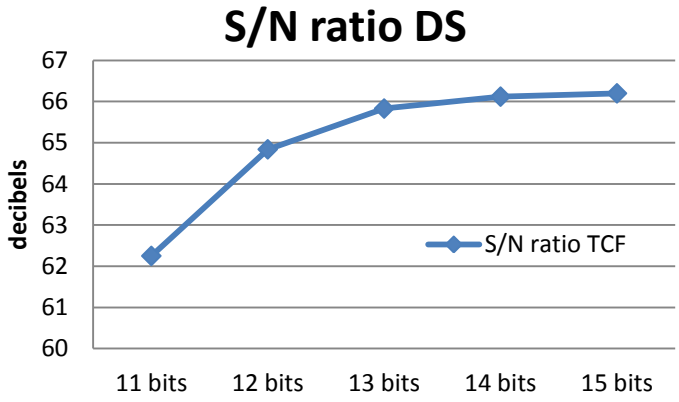


Figure 4.29 DS signal to noise ratio

4.4 Baseline Correction 2

Baseline correction 2 functionality was explained in chapter 3. This section is focused on the optimization of its hardware implementation.

The baseline inside the processing window can have relatively fast variations. Therefore, the filter presented in section 4.2.2 cannot be used in this case. A typical filter that could fulfill the requirement is the Moving Average Filter (MAF). This filter is a very simple FIR with a fast computation algorithm.

The MAF is faster than other digital filters for few reasons. First, there are only two operations per value. Second, there are not multiplications involved (long time consuming operation). Third, the algorithm can be carried out with integer representation (more than an order of magnitude faster than floating point).

The BC2 circuit is divided in two blocks, double threshold scheme and a MAF. Figure 4.30 shows the BC2 block diagram.

First, the 13-bit two's complement input *din* is converted to a 13-bit unsigned signal by adding 4096 which simplifies the architecture of the MAF. Next, the double threshold scheme determines the acceptance window for the baseline calculation. For that, the input signal is compared with an upper and lower bound which are calculated from the baseline by adding or subtracting the bounds. These bounds, thr_{hi} and thr_{lo}, are programmable per channel through three parameters, one constant per channel and two global values which define the margins above/below. Next, the value of *bsl* goes to the control logic which allows the selection of pre- and post- samples in the generation of the exclusion window and generates an enable signal to the MAF. The *config* input programs the number of pre and post samples. The *TapsEn* input is used to configure the MAF, as explained in detail later. On the other hand, the *offset* input can be useful to keep information above zero, preventing it from being lost before clipping. Finally, at the output of the BC2 the signal is clipped within a range between 0 and 1023 and reduced to a 10 bit word.

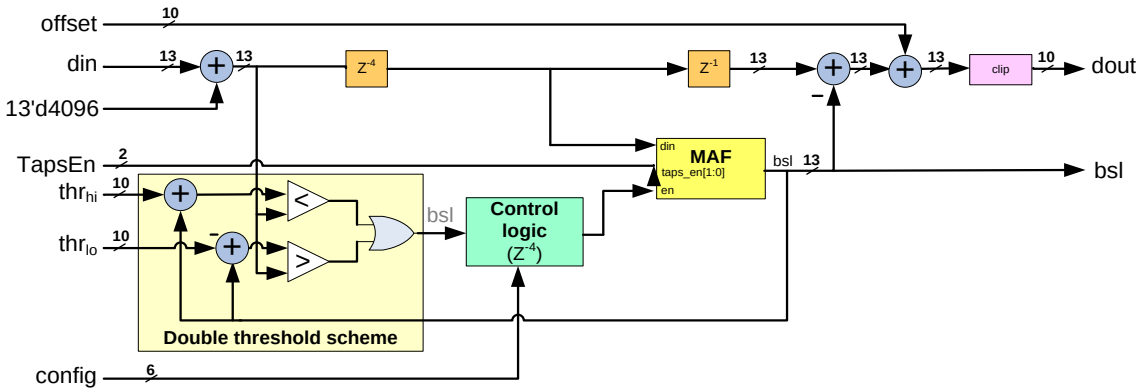


Figure 4.30 BC2 block diagram

The main difference of the S-ALTRO BC2 with respect to the ALTRO chip is the optimized Moving Average Filter (MAF) for greater flexibility and optimized digital noise reduction, explained in detail in sections 4.4.1 and 4.4.2 respectively. However, considering just the new BC2 in the ALTRO implementation, the design would have an increase of 4% in hardware resources.

4.4.1 Flexibility optimization

The ALTRO chip implements an 8 tap FIR structure with transfer function in the Z-domain given by eq. 4.34.

$$x[n] = x[n-1] + \frac{u[n]}{8} + \frac{u[n-8]}{8} \qquad \text{(eq. 4.34)}$$

However, greater filter flexibility is achieved in the S-ALTRO BC2 by adding the possibility of choosing the number of stages in the MAF, expressed in eq. 4.35.

$$x[n] = x[n-1] + \frac{u[n]}{M} + \frac{u[n-M]}{M} \;\; ; \;\; \text{M = 2, 4 or 8} \qquad \text{(eq. 4.35)}$$

Figure 4.31 shows the MAF block diagram, where *Din* and *Bsl* are the input and output respectively. *En* enables the shift registers and *TapsEn* changes the number of stages in the filter.

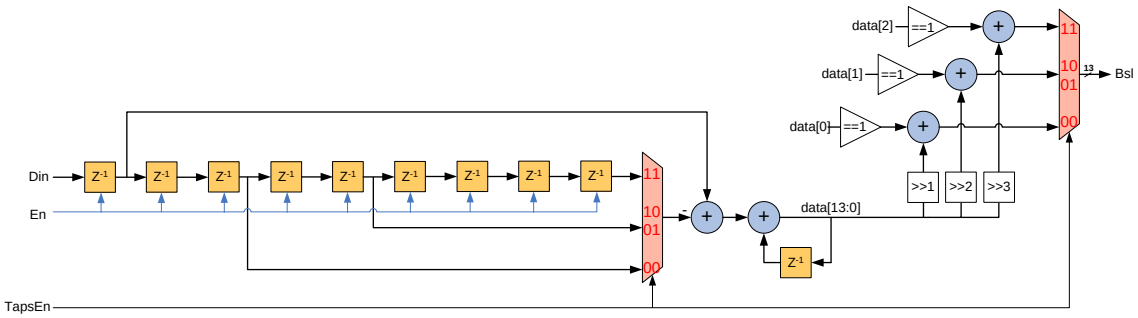


Figure 4.31 MAF block diagram

The number of stages modifies the step response of the filter and, therefore, can adjust the processing to different inputs. Figure 4.32 shows the step responses of the MAF with respect to M. If M = 8, the FIR has the same behavior than eq. 4.34. M can vary as a power of 2, from 2 to 8, simplifying the hardware by avoiding the use of multipliers.

As expected, the MAF has faster response time with respect to the IIR filter presented in the section 4.2.2. For the same average of two samples, the IIR BC1 has a response time of 7 samples, while the MAF has a response time of 2 samples.

In this case, the hardware realization needs only two adders and a programmable shifter by $\log_2(M)$ bits. A greater number of taps (registers) would lead to an increase of power consumption. Consequently, a trade-off between flexibility and power consumption was made and simulations showed that 8 taps were enough to process the input signal for HEP applications.

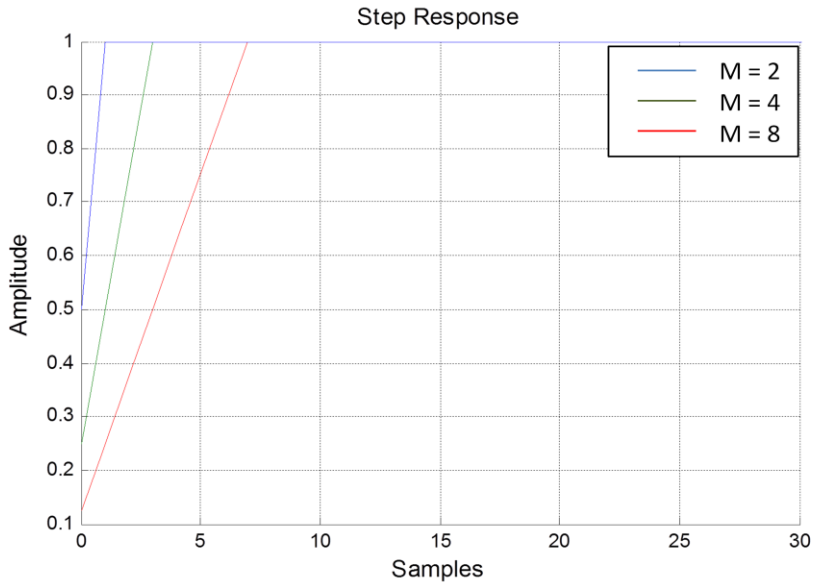


Figure 4.32 BC2 MAF filter step response

4.4.2 Digital noise optimization

The ALTRO MAF truncates the output of the MAF which introduces an extra digital noise. As part of the MAF optimization, the output is rounded-off.

Figure 4.33 shows the noise model of the MAF quantization error. The error introduced in the system depends on the quantization method used; truncation or round-off.

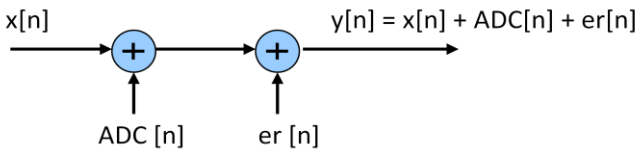


Figure 4.33 ALTRO MAF truncation noise model

The two's-complement round-off mean and variance are defined in eq. 4.36. While the two's-complement truncation mean and variance are defined in eq. 4.37. Finally, the output noise is defined in eq. 4.38.

$$m_e = 0 \quad ; \quad \sigma_e^2 = \frac{2^{-2B}}{12} \qquad \text{(eq. 4.36)}$$

$$m_e = -\frac{2^{-2B}}{2} \quad ; \quad \sigma_e^2 = \frac{2^{-2B}}{12} \qquad \text{(eq. 4.37)}$$

$$\sigma_{er}^2[n] = \sigma_e^2 + m_e^2 \qquad \text{(eq. 4.38)}$$

On the other hand, the ADC noise variance, the total noise introduced and the signal variance in the circuit are defined in eq. 4.4, eq. 4.5 and eq. 4.6 respectively. SNR was defined as the ratio

of signal variance to noise variance, expressed in decibels (db), see eq. 4.7. As shown in Figure 4.34, the SNR in the BC2 has been increased in 0.34 db.

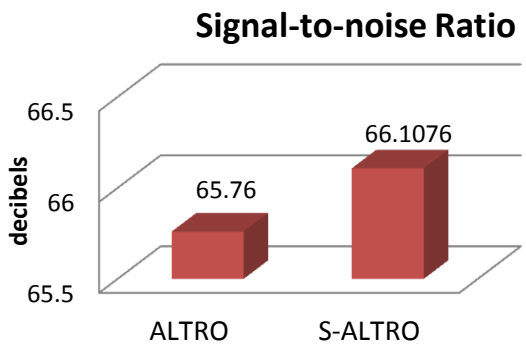


Figure 4.34 Signal-to-Noise Ratio comparison

4.5 Circuit level optimization

Another approach to reduce the power consumption of the logic is to minimize the power dissipated due to the switching activity of the logic gates. The dynamic power consumption of a CMOS logic circuit is given by eq. 4.39.

$$P_D = f \cdot C \cdot V_{DD}^2 \qquad \text{(eq. 4.39)}$$

Where V_{DD} is the supply voltage, C is a load capacitance and f is the switching frequency.

Since the power consumption is proportional to the square of V_{DD}, reducing V_{DD} is the most effective way of reducing the power consumption. Unfortunately, reducing the supply voltage also increases the propagation delay of the gates and thus reduces the maximum operation frequency of the circuit. The gate delay as a function of V_{DD} for a 130 nm CMOS NAND gate is shown in Figure 4.35.

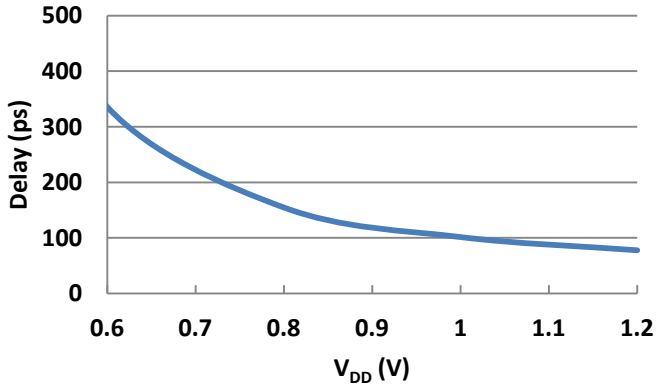


Figure 4.35 Gate delay as a function of V_{DD} for a NAND gate in 130nm

The critical timing path of the digital block is in the DS, more specifically in the multipliers of the IIR filters feedback paths. Using a 13-bits Booth Wallace two's complement multiplier, a delay of 8.6 ns was obtained for a 130 nm technology and a supply voltage of 1.2 V. If V_{DD} is reduced to 0.8 V the multiplier delay increases to 17.2 ns still allowing operation at 40 MHz. Therefore, if 0.8 V is used for the digital supply voltage, the power consumption of the circuit is reduced to 45 % in relation to the nominal operating voltage of 1.2 V for the technology used.

4.6 Conclusions

Different optimizations have been presented for the different stages of the DSP (BC1, DS, BC2) and for the interconnections between them.

The BC1 optimizations are focused on the increase of the SNR and flexibility. The technique of using the baseline memory output shifted in the case of the subtraction makes an increase of 1.5db in the SNR. On the other hand, the IIR filter presented increases the flexibility of the baseline correction filter outside the processing window as it is capable of following the signal more accurately. However, all these improvements have the drawback of an increase of 7.9% in hardware resources with respect to the old design. This filter is very small compared to the full DSP. Therefore, the little hardware resources increase does not have an impact in the full chip.

The DS is the biggest block in area and the most power consuming (84% of the total digital power). A great deal of effort was made to reduce its power consumption and area. Different architectures were presented and studied. It was concluded that the transposed direct form II is the optimum architecture for the DS in this application. This architecture allows for the reduction of the data-path from 18-bits (previous implementation) to 13-bits and thus is using a much simpler multiplier for the implementation of the IIR filters. As a result of this narrower data path the number of gates in the DS is reduced by almost a factor 2 with respect to the previous solution. Considering just the new DS architecture in the old design implementation, the hardware resources would have decreased to 2/3. Moreover, the switching activity in the system, e.g. for an input with 10% occupancy, is reduced roughly by a factor of 2, reducing the power consumption by the same factor.

The BC2 optimizations are also focused on the increase of the SNR and flexibility. An optimized MAF has been presented where the SNR has been slightly increased, 0.34db, and features greater flexibility. However, these improvements have the small downside of a resulting in 4% increase in hardware resources.

A circuit level optimization was also presented. The optimization consists of reducing the V_{DD}, to the minimum value that is still compatible to longer time delays. The timing critical path of the digital block is in the DS, concretely in the multipliers of the IIR filters feedback paths. The reduction of the power supply down to 0.8V maintaining fast operation would reduce the power consumption in the digital circuit to 45% with respect to what it would be obtained if the nominal supply voltage (1.2 V) was used.

Figure 4.36 summarizes the improvements in the digital block in terms of power, area and signal to noise ratio.

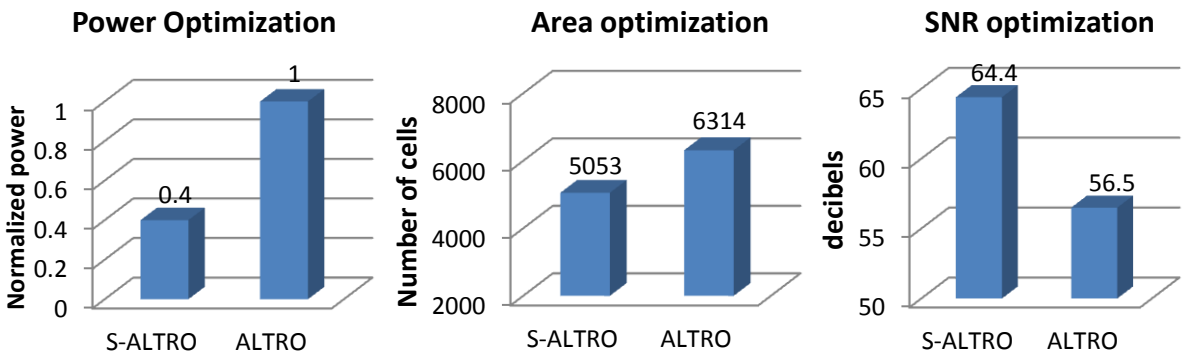


Figure 4.36 Power consumption, area and SNR optimization summary

In conclusion, the power consumption of the digital block can be decreased to 40%, the hardware resources have been reduced to 80% and the SNR has been increased 7.9 db. These numbers are estimated from the optimizations presented in the chapter from a theoretical point of view.

Chapter 5 S-ALTRO Prototype Design

5.1 Introduction

This chapter presents the S-ALTRO prototype architecture and design. The main objective of this prototype is to test the integration of the analog sensitive amplifiers, ADCs and digital signal processing in a single ASIC. The optimized digital filters presented in Chapter 4 are also included in the processing chain. This prototype implements the ALTRO interface to reduce the testing time by re-using back-end electronics from the ALICE TPC project and make it compatible with current detectors.

Adding analog sensitive circuitry to digital switching logic is a very challenging task. The major problems are: near field coupling between neighboring circuits and coupling between widely separated circuits, through the chip substrate and power rails. As explained in detail later, a great deal of effort was made to isolate the analog and digital part adding BFMOAT, guard rings and having isolated power domains.

The full design flow of the S-ALTRO prototype has been carried out at CERN. This includes the floorplanning, placement, routing, timing calculation, power estimation, simulation and verification of the whole chip. All the blocks were designed at CERN with the exception of the memories, which were bought as IP blocks. The S-ALTRO prototype was produced in the third quarter of 2010 in IBM CMOS 130nm DM technology. The technology for this prototype is determined by the ADC, which needs high precision capacitors (Metal-Insulator-Metal, MIM) only available in DM[1] technology.

[1] DM or Dual Metal, last aluminum metal at a larger pitch for designs with 6 or more metal levels.

5.2 S-ALTRO prototype architecture overview

The S-ALTRO prototype integrates 16 channels operating concurrently on 16 independent analog signals coming directly from the detector. Each acquisition channel consists of a CSA, a 10-bit ADC with a nominal sampling rate of 40 MHz, a pipelined Digital Signal Processor and a Multi-Event Memory. See Figure 5.1.

The CSA and ADC blocks were presented in Chapter 3. The digital signal processor implements the optimized digital filters presented in Chapter 4. The Zero Suppression and Data Format are the same as used in the ALTRO chip ([BOSCH2]). The communication protocol (Common Control Logic) is based on the protocol of the ALTRO chip, although it has been adapted to the new features of the S-ALTRO prototype. Next section explains in detail the chip interface.

The main motivation for adopting the ALTRO chip interface and communication protocol was to use for the characterization of the S-ALTRO prototype part of the hardware and software already developed for the ALTRO chip. The S-ALTRO prototype characterization in a real detector is not the aim of this thesis.

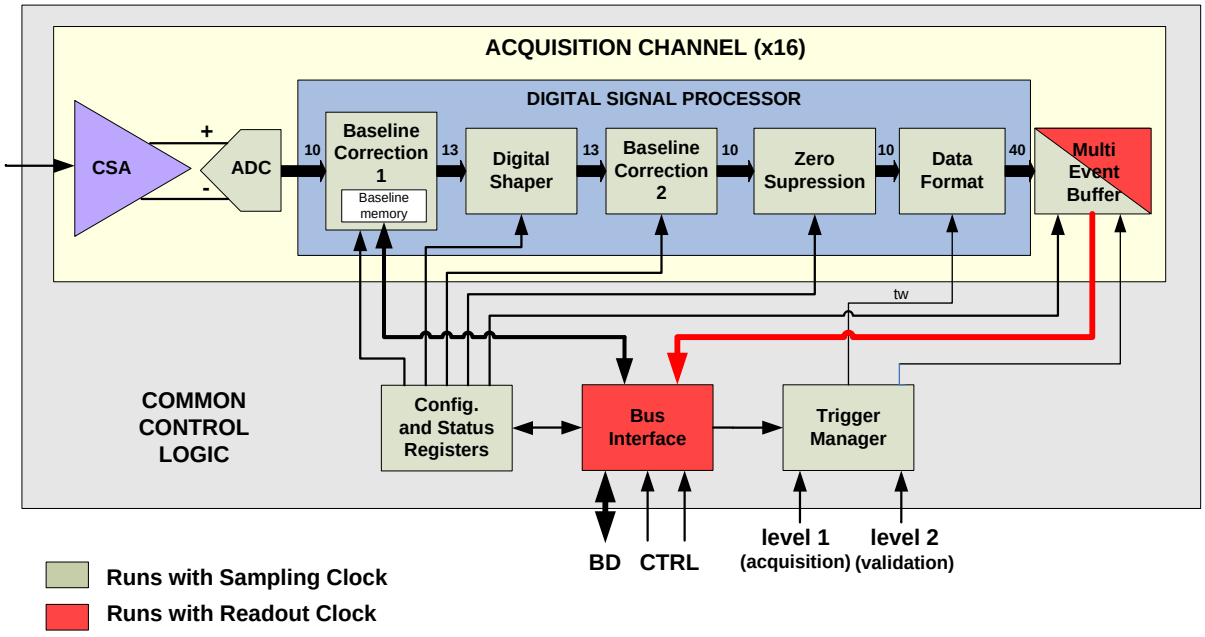


Figure 5.1 S-ALTRO prototype block diagram

5.2.1 S-ALTRO prototype common control logic

The interface has a digital bus composed of 40 bi-directional lines and 8 control lines. The 40-bit bus contains 20 address bits that define the S-ALTRO address space and 20 data bits. This addressable space contains the baseline memories, the configuration/status registers and a set of

commands. The most relevant S-ALTRO bus signals are summarized in TABLE 5-1. For further details of the logic and implementation see S-ALTRO prototype manual ([S-ALTRO]).

TABLE 5-1 S-ALTRO bus signals summary.

S-ALTRO BUS				
Signal Name	**Function**	**# bits**	**Dir.**	**Polarity**
AD	Address / Data	40	Bi-directional	H
WRITE	Write / Read	1	Input	L
CSTB	Command Strobe	1	Input	L
ACKN	Acknowledge	1	Output	L
ERROR	Error	1	Output	L
TRSF	Transfer	1	Output	L
DSTB	Data Strobe	1	Output	L
LVL1	Level-1 Trigger	1	Input	L
LVL2	Level-2 Trigger	1	Input	L
GRST	Global Reset	1	Input	L
SRST	Soft Reset	1	Input	L
SCLK	Sampling Clock	1	Input	-
RCLK	Readout Clock	1	Input	-

The new common logic features with respect to the ALTRO interface are:

- Soft reset: the soft reset (SRST) is an active low global reset which initializes only the counters and state machines. This would allow going to an initial state with no need of reinitializing the configuration registers.

- Chip readout command: reads the entire chip skipping the empty channels. This optimizes the readout time with respect to the ALTRO chip. Obviously, this improvement is particularly relevant for applications with low occupancy (many channels empty). For instance, the time for reading the 16 empty channels with the ALTRO channel readout command is 3.4 μs at 80MHz, while using the chip readout command is 762ns at 80MHz. It is more than 4 times faster.

- Empty channels register: this register shows the empty channels in this chip. This register could help reducing the readout time. Comparing with the same example as before, the time for reading this register is only 162 ns at 80MHz. It is more than 20 times faster with respect to the ALTRO system.

- Constant per channel register: adjusts the filter thresholds related to the noise per channel. Thresholds for BC1 and BC2 are defined as a combination of a *constant* per channel and a global value. The *constant* per channel defines the noise per channel, while the global values define the margins above and below that noise.

- Zero Suppression thresholds per channel: ZS threshold is implemented per channel. The ALTRO chip implemented one global threshold.

- Other configuration registers: Digital shaper includes two extra registers for the 4th order filter (L4, K4). The BC1 double threshold windows include new registers. New BC2 configuration bits are included.

- Multi-event buffer and baseline memory controls: memory control logics have been modified to switch always on the rising edge of the sampling clock. This is important to confine the switching noise in tiny time window following the rising edge clock. As it will be explained later, this is essential to minimize the noise induced during in the ADCs during the conversion of the analog signals. The ALTRO chip uses the rising edge to clock the registers and the falling edge to clock the memories.

5.3 S-ALTRO prototype design methodology

The design of this mixed signal ASIC has been divided in two flows, one flow for the digital circuit and other flow for the analog circuits (CSA and ADC). This chapter details the digital flow.

The first block of the S-ALTRO prototype was the CSA, produced in 2007, in IBM CMOS 130nm LM[2] CDB[3].

The second block of the S-ALTRO prototype was the ADC, produced in 2009, in IBM CMOS 130nm DM CDB. This block defined the technology of the S-ALTRO prototype due to the needed of high precision capacitors (Metal-Insulator-Metal, MIM) only available in DM technology. This implied porting the CSA to DM technology.

The digital circuit layout and prototype integration started in the first quarter of 2010, in IBM 130nm DM technology and OA[4] database. Figure 5.2 shows the S-ALTRO prototype methodology of the main blocks.

[2] Last Copper metal (LM) at a pitch for designs with 5 or more metal levels.

[3] CDB: constant database which allows for only two operations: creation and reading. Both operations are designed to be very fast and highly reliable. Since the database does not change while it is in use, multiple processes can access a single database without locking.

[4] Open Access is a community effort to provide interoperability, including unified data exchange among integrated circuit design tools through an open standard data API and reference database supporting that API for IC design.

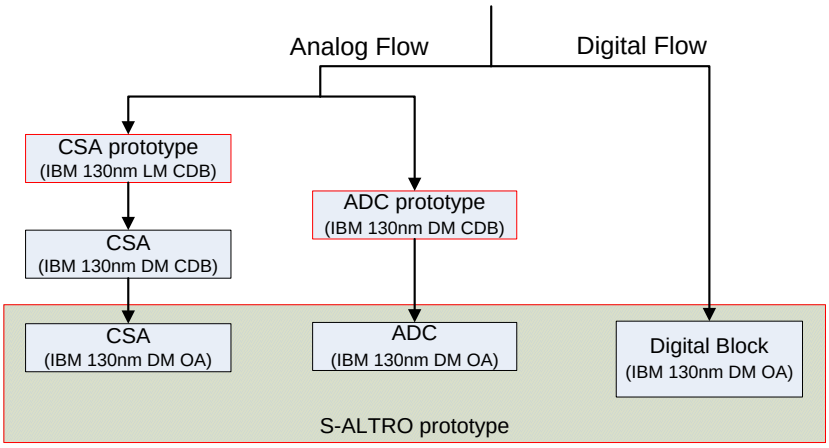
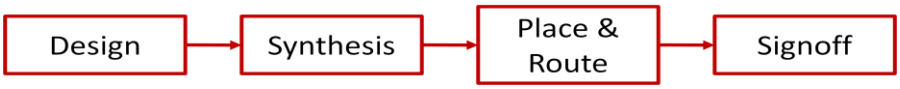


Figure 5.2 S-ALTRO prototype methodology

5.4 Digital flow

The digital flow can be divided in four steps: design, synthesis, place and route, signoff.



Design: the design starts with the description of the circuit using a hardware description language (e.g. Verilog) at Register Transfer Level (RTL). The code should be verified with simulations. Moreover, a very important aspect in this phase is the creation of the constraint file. The constraint file in this design defines the clocks, maximum input delay, minimum output delay, clock uncertainly and maximum transition time.

Synthesis: transfers the RTL code into a netlist of generic cells or mapped into logic cells from the library. At this point some optimizations in the RTL code were made to meet constraints such as timing, area or power. At the end of this step some simulations at gate level were done to check the functionality of the netlist.

Place and Route: consists of floorplanning, macro placement, power planning, placements of cells, clock tree synthesis, core fillers, routing of the nets, metal fills. Floorplanning and power planning are realized fully manually, while the rest are realized semi-automatically through scripts. Section 5.4.1 explains in more detail two of the most important issues, floorplanning and power planning. The place and route phase results in a full layout of the design.

Signoff: consists of a series of checks before submission:

- DRC: Design Rule Checking determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called design rules.
- LVS: Layout Versus Schematic determines whether a particular integrated circuit layout corresponds to the original schematic.

- IR-Drop/EM analysis: IR-Drop analysis computes the drop in the supply voltage that is seen as you move across the length of the supply line. Electromigration (EM) estimates the transport of the metal that is caused by ions moving in a conductor.
- Static Timing analysis is a method of computing the expected timing of a digital circuit without considering the dynamic behavior.
- Dynamic simulation computes the design with a set of test benches which emulates dynamic behavior of the ASIC.
- Power analysis estimates the power consumption of the chip. It can be based on statistical analysis or simulated-based.

The synthesis was carried out by using *Cadence Encounter RTL Compiler*. The place and route, IR-Drop/EM analysis, static timing analysis and power analysis was carried out within *Cadence SoC Encounter RTL-to-GDSII System*. Later, the design was exported to *Cadence Virtuoso* where the DRC and LVS were checked. At this point the digital block library is ready to be included in the top mixed signal design.

5.4.1 Floorplanning and power routing

Power consumption affects the overall structure of the floorplan and impacts the design of the power grid. The common issues to take into account are:

- Dynamic and leakage power consumption: this affects the power density which can cause thermal breakdown of the materials of the IC.

- IR-drop and Voltage drop: these are affected by the average power consumption and the dynamic power consumption respectively.

- Electromigration: is related to the cells in the design which draw current across the power mesh and can lead to breakdown of the grid.

All these effects could affect the overall reliability of the ICs and can eventually lead to chip failure.

One of the most critical aspects in an ASIC layout is the design of the power grid. The parameters to optimize are: the number of power pads, the number and width of stripes in the grid. There are three main steps:

- Estimation of power pads at the design to handle all the power and grounds needs for the whole chip. The number of I/O power cells is established supposing a current drive of 100mA per power pad

- Determine the metal layers for the power and ground routing; the top layers of metal provide the least resistance and will thus have the best IR-drop characteristics. For high speed designs these layer can be used to route clocks and high-fanout nets. The S-ALTRO prototype works at very low frequency compare to the technology capabilities. Therefore, the top layer will be used for the power routing.

- Define number and width of the power stripes and rings. This decision is a trade-off between too many or too wide that will take up valuable signal routing space, or too few or narrow that could make the IR-drop and EM characteristics of the ASIC unacceptable. To define this, multiple IR-drop and EM simulations were made and are presented later in this section.

The floorplan defines the placement of the main blocks of a design in the most efficient way in terms of area, power grid and/or routing capabilities. In this prototype, the memories occupy 42% of the total floorplan. Therefore, their placement determines efficiency of the automatic routing. The memory blocks are routed in metal 1, metal 2, and partially in metal 3. Moreover, pins are connected to the nets through metal 3 and metal 4. A first study showed that memories with horizontal orientation improve the routing, this fact is related to the pin location of the memories, see Figure 5.3. Its horizontal orientation gives more space for horizontal routing at lower metals, this is even more important in this particular case, where the floorplan is quite rectangular (ratio high/width is approximately 0.19).

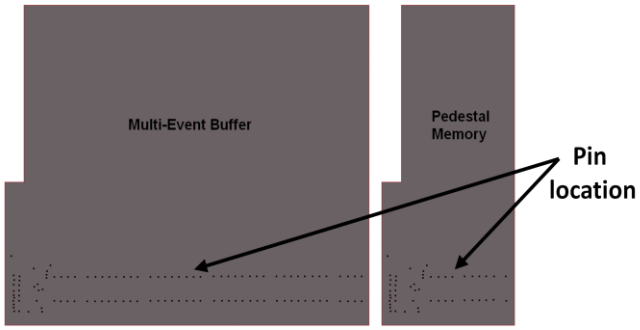


Figure 5.3 Location of the memory pin

Figure 5.4 shows an overview of the final floorplan. This floorplan is pad limited. The core area is fixed by the number of pads of the design. The placement of the I/O cells respects the standard package rules and its location depend on the respective switching noise of the pad. For example, static pads like the chip hardware address (fixed value per chip) are located closer to the analog part. The top part side is pads free, because it will be the connection to the analog block. Placement blockage has been included between memories to avoid the placement of standard cells.

In this design, the memories have higher power consumption with respect to the other blocks. To reduce the possibility of IR-drop issues, the memories are placed near the periphery of the die. This reduces the effective resistance between the power and ground pad cells and the high performance blocks, resulting in better IR-drop characteristics. In addition, to prevent electromigration issues it is preferred to place the memories at some distance to each other.

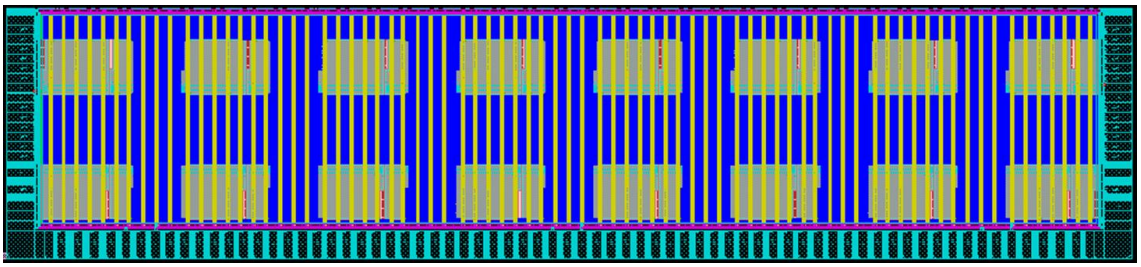


Figure 5.4 S-ALTRO prototype power plan

Once the power planning is defined it is always necessary to make sure that IR-drop and EM characteristics are appropriated and within specifications. *Soc Encounter* VoltageStorm analysis helps enabling a high capacity hierarchical sign-off power planning analysis. This analysis is based on a power calculation which could be statistical or simulation-based. Both analyses were performed at different phases of the design:

a) The statistical analysis: in the first phase it was used a statistical analysis with high stress conditions. TABLE 5-2 summarizes the analysis conditions.

TABLE 5-2 Statistical analysis conditions

Variable	Value
Sampling clock	50 MHz, 30% toggle
Readout clock	90 MHz, 30% toggle
Net Voltage	1.5 V
Voltage variation	10%
Temperature	25 C

Figure 5.5 shows the IR-drop map for the statistical analysis. The maximum IR-drop is 8.02 mV which is below the 1%. This is an acceptable loss. Figure 5.6 shows the current distribution in the power plans. The maximum current is 27.9 mA, which complies with the technology recommendations. The electromigration simulation shows that the mean time to failure is approximately 3 years. This value is relatively low for HEP applications, but as mentioned the analysis conditions does not exactly correspond to the real conditions. The estimated power consumption of the digital block in this analysis is 114 mW.

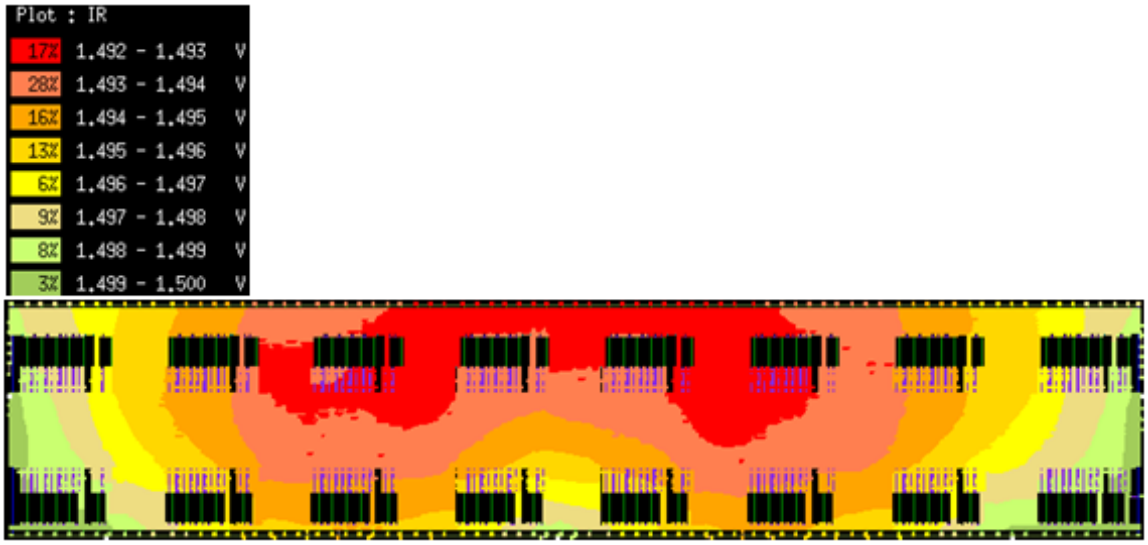


Figure 5.5 IR drop analysis

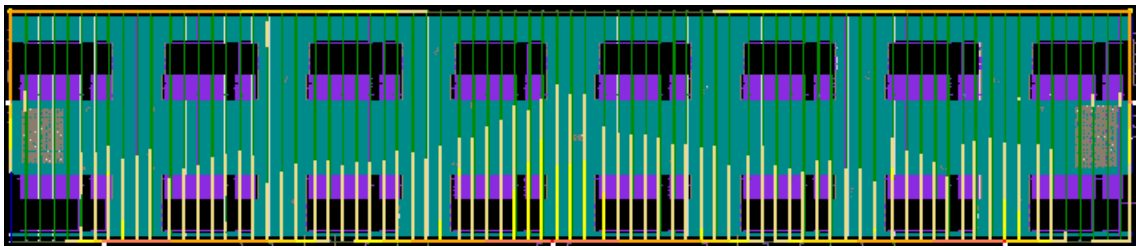


Figure 5.6 Current distribution in the power routing

b) The simulated-based analysis is the most realistic test because it is based on the switching activity (Value Change Dump, VCD file) of the circuit for a real simulation. In particular, the VCD has been created from a typical test of the S-ALTRO prototype, where the MEB is filled up with a pattern and read out subsequently. TABLE 5-3 summarizes the analysis conditions.

TABLE 5-3 Simulated-based analysis conditions

Variable	Value
Sampling clock	40 MHz
Readout clock	80 MHz
Net Voltage	1.5 V
Voltage variation	10%
Temperature	25 C

Figure 5.7 shows the IR-drop map for the simulated-based analysis. The maximum IR-drop is 1.75 mV (aprox 2‰). Figure 5.8 shows the current distribution in the power plans. The maximum current is 4.89 mA. The EM shows that the mean time to failure is approximately 15 years. The estimated power consumption of the digital block is 20.2 mW. Therefore, very low IR-Drop and maximum current are achieved in this layout. Moreover, the estimated mean time to failure fits to long term HEP applications.

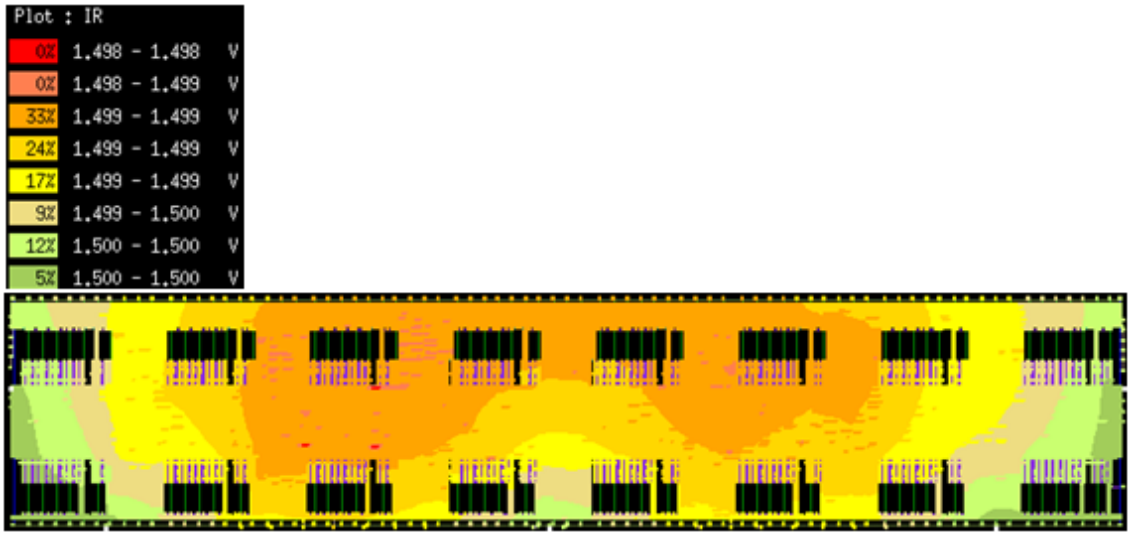


Figure 5.7 IR drop analysis

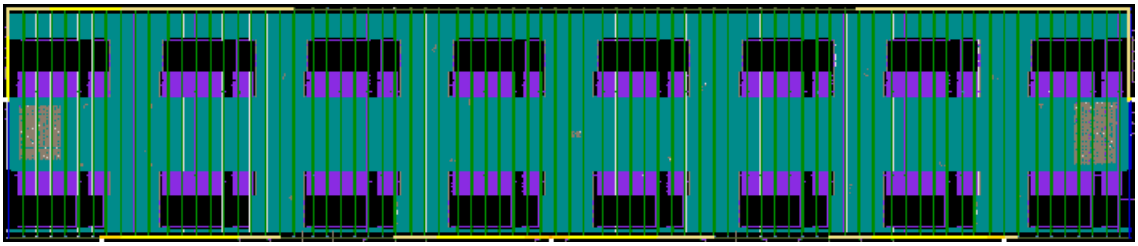


Figure 5.8 Current distribution in the power routing

5.4.2 Timing analysis

The process conditions are not fixed, temperature or supplies can change within certain range. Therefore, it is necessary to take into account the variations for a realistic timing analysis.

The timing analysis considers these and other variations with the corners: Slow, Typical, Fast. Slow corner is defined for Vdd 1.4V and 125°C, typical corner is defined for 1.5V and 25°C and fast corner is defined for 1.6V and -55°C. Timing analysis was carried out in three phases.

- First phase: during the layout process were checked the setup and hold time of all nets independently of their functionality by using *Cadence Soc Encounter*. The setup analysis considers the launch net as the maximum timing (Slow corner) while the capture net is considered as minimum timing (Fast corner). Hold analysis considers the launch net as the minimum timing (Fast corner) while the capture net is considered as maximum timing (Slow corner), see Figure 5.9. No timing violations were found.

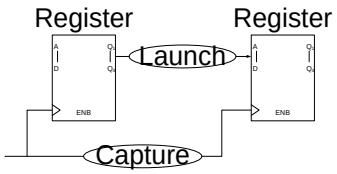


Figure 5.9 Register timing definitions

- Second phase: a set of test benches with different functionalities (e.g. control logic, digital signal processing) are defined to cover the main functionality of the S-ALTRO prototype. The ADC behavior is emulated in Verilog. The timing information is extracted from Cadence Soc Encounter and back-annotated into the netlist. See Figure 5.10. Again, these simulations did not report any timing violation.

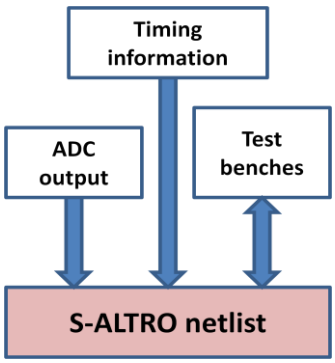


Figure 5.10 Timing analysis

- Third phase: corresponds to a comparison between the RTL code and the back-annotated design using the same set of test benches, see Figure 5.11. The objective is to verify that the physical layout behaves as the functional design.. Both descriptions are tested with the same stimuli files, verifying clock cycle by clock cycle that their responses match within a well define time window. In this design, a 5ns time window is defined for the fast corner, while a 10ns window is defined for the slow corner. *Comparescan* can compare multiple hardware simulation runs in a single simulation. It is flexible and programmable allowing a large number of applications.

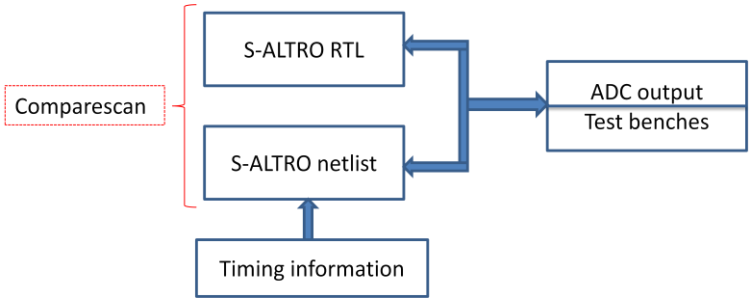


Figure 5.11 Timing comparison

5.4.3 Scan chain

The scan chain provides a simple way to set and observe every flip-flop of the digital circuit. This system needs four pads. Only two of them need to be specific for this application, the others can be multiplexed with other pads and controlled by *ScanModeChip* pad (See TABLE 5-4).

When *ScanModeChip* and *ScanEn* are asserted, every flip-flop in the design is connected to a long shift-register. The "Scan in" pin provides the data to the chain, and the "Scan out" pin is connected to the output of the chain. Using both clocks at the same frequency (*adcclk* and *rdoclk*), an arbitrary pattern can be entered into the chain and the state of each flip-flop can be read at the output.

The chain in this prototype has 13915 registers, considering both clocks running at 50MHz, an initial time of 278.3 μs is needed to see the first input to the Scan in pin.

TABLE 5-4 Scan chain pins/pads

Scan Chain pads	Scan Chain pins	Share pad	Active
ScanModeChip	-	-	High
ScanEn	-	-	High
-	Scan in	*cstbb*	-
-	Scan out	*tstout*	-

5.5 S-ALTRO prototype physical characteristics

Figure 5.12 shows a detailed view of the prototype layout. The CSAs are placed in a column in the left part of the chip starting from channel 15 on the top and going down to channel 0 on the bottom. The ADCs are placed next to the CSAs, minimizing the capacitance between them. Between CSAs and ADCs are placed the power lines of the analog block. The digital block (control logic + DSP) is placed on the right part in a common block for all the channels. It is important to mention that the memories are placed aligned with the corresponding analog channels to minimize the routing. Both analog and digital pads were placed around their respective cores before assembling.

Isolation of the analog and digital parts was achieved by adding BFMOAT and guard rings. BFMOAT is a high resistivity substrate region placed between different power domains to isolate them from each other. The effective substrate resistance between adjacent regions depends on the width and perimeter of the BFMOAT. While a guard ring is a continuous ring of n-diffusion in an n-well connected to VDD, and a ring of p-diffusion in a p-well connected to VSS.

Figure 5.13 shows with black lines these isolations. The two grey pads on the top of the diagram are needed to connect to ground the guard ring which surrounds the whole chip.

Different power domains were implemented to isolate completely the analog and digital blocks. There are five different power domains, shown in

Figure 5.13: CSA (yellow), ADC analog (blue), ADC digital (pink), digital core (light green), digital pads (dark green). Moreover, electrostatic discharge (ESD) protection diodes are included among the grounds to prevent grounds from being biased at different voltages.

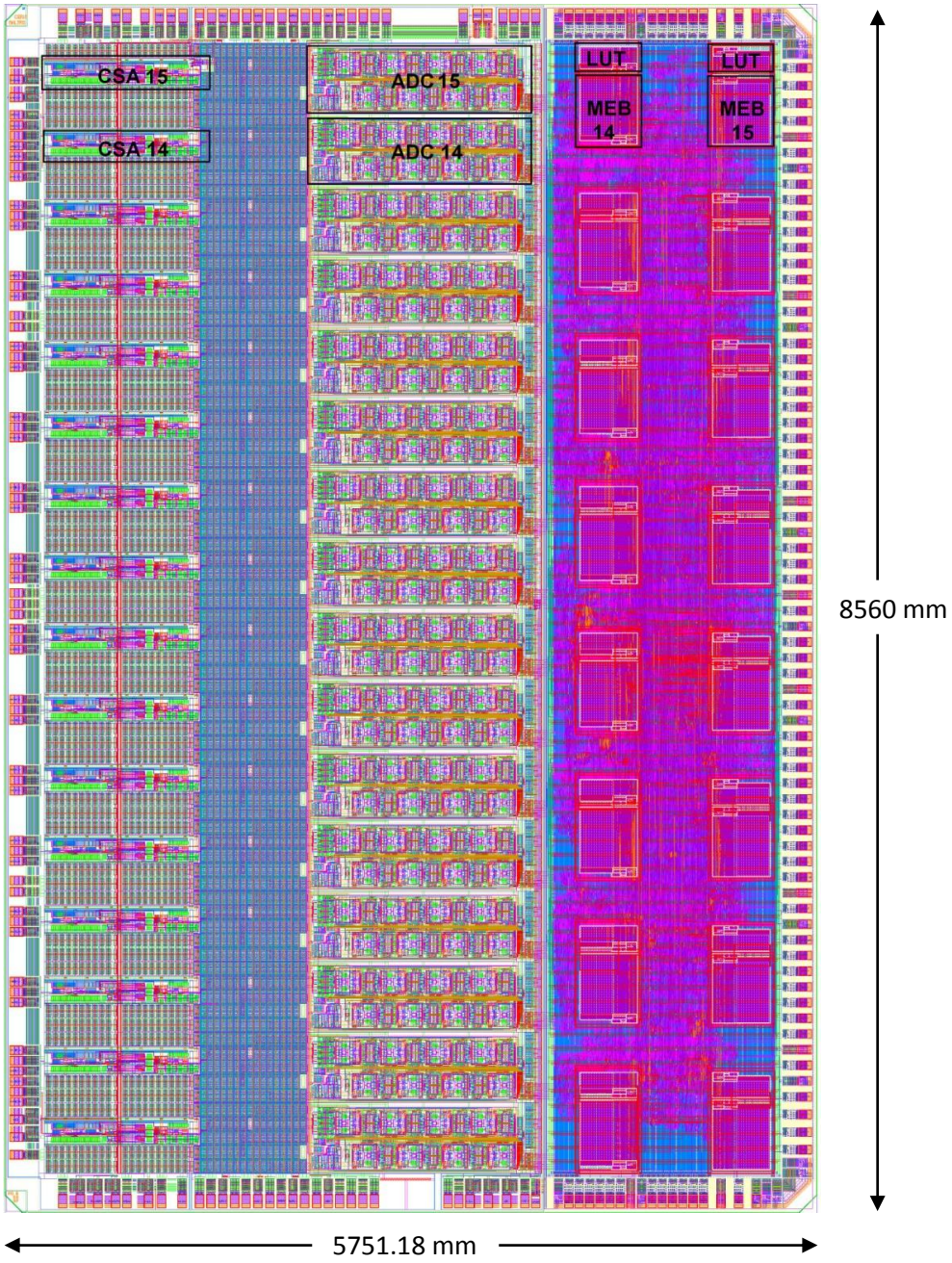


Figure 5.12 S-ALTRO prototype layout

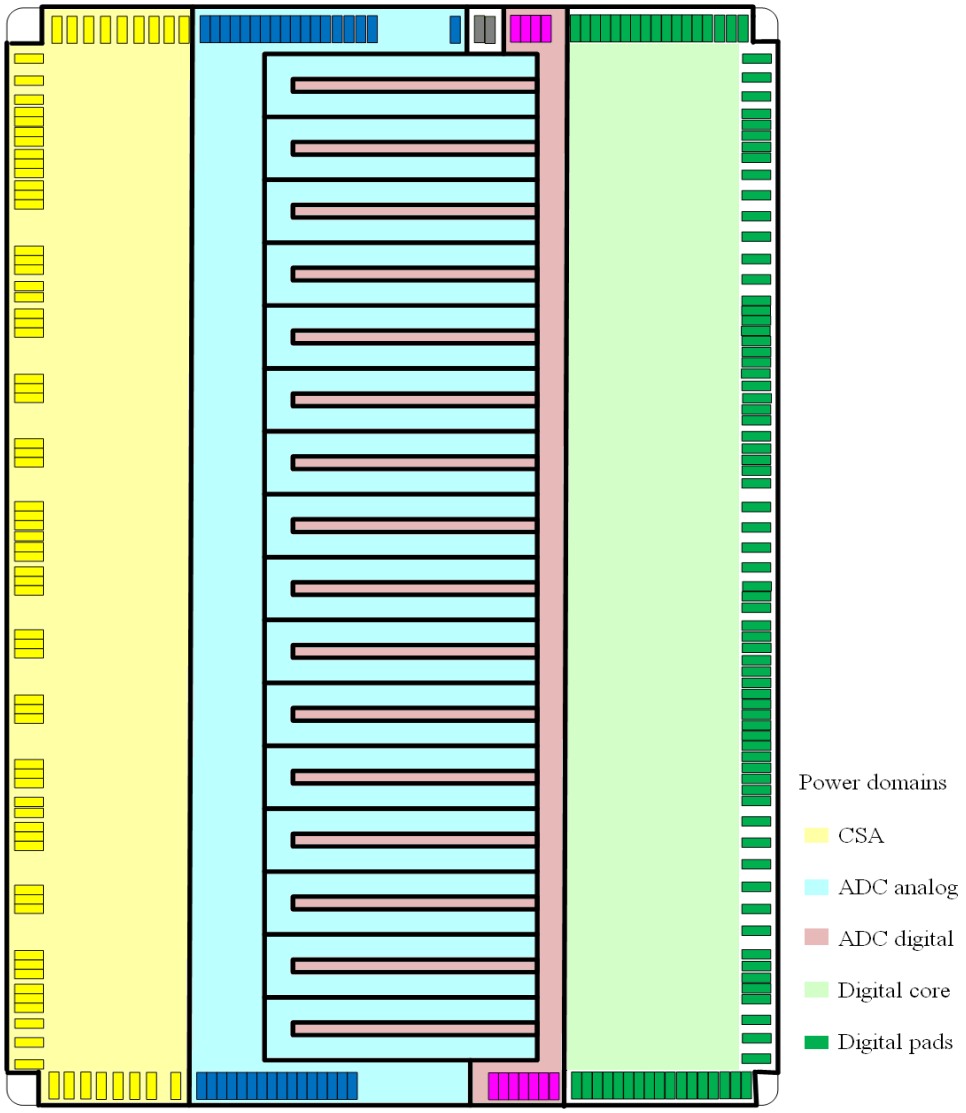


Figure 5.13 BFMOAT/guard ring block diagram and power domains diagram

The channel 15 can be used as test channel. This channel includes six switches to enable the CSA and ADC operation independently (see Figure 5.14). The *TestMode* pad controls all the switches enabling the auxiliary test pads. In test mode, the CSA output is accessible through two pins and an external input can be injected into the ADC.

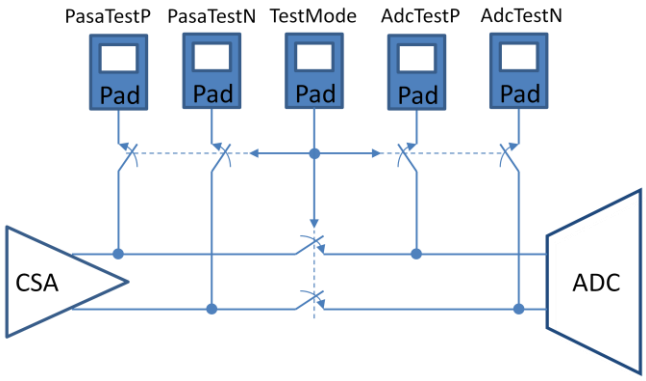


Figure 5.14 Test channel switches

5.5.1 Clock scheme

A critical aspect in the integration of this mixed signal ASIC is the sampling clock scheme. The same sampling clock is distributed to the ADCs and to the DSP. However, a phase shift between the arrivals times is needed to minimize the interferences of the DSP switching at the ADCs sensitive time.

The instant when the sampling clock reaches the DSP flip flops is the noisiest moment in the cycle. After that, the DSP produces reduced switching until 12.8ns later (worst case). From that point until the next cycle the digital block is quiet.

The most sensitive moments in the ADCs are the sampling time and the open gate comparators. The ADCs comparators need the full cycle to have a final result, although the last part in the cycle is the most sensitive. The right side of Figure 5.15 shows the ADC sensitive time with respect to the sampling clock (SCLK).

In this design the sampling clock signal is first split in two clock trees, one for the DSP and another for the ADCs. Each branch has a fixed delay which depends on the internal clock tree. The ADC internal clock tree has a delay of 0.34ns, while the DSP has a delay of 1.45ns.

The objective of the sampling clock distribution in the chip is that the sampling clock signal reaches first the ADCs and at least 0.81ns later (worst case) reaches the DSP flip flops. For this reason the sampling clock distribution in the chip has different delay for the ADCs and DSP, see left side of Figure 5.15. The ADCs branch has a delay of 1.03 ns and the DPS branch has a dealy of 0.73ns. This design allows a clean noise environment during the sampling time of the ADCs and in the most sensitive part of the comparators.

Moreover, two auxiliary pads are placed to operate with independent clock phases in the ADCs and in the DSP (CLKAux and CLKSelect). This implementation allows testing the influence of the digital logic switching noise in the system depending on the phase of the clocks.

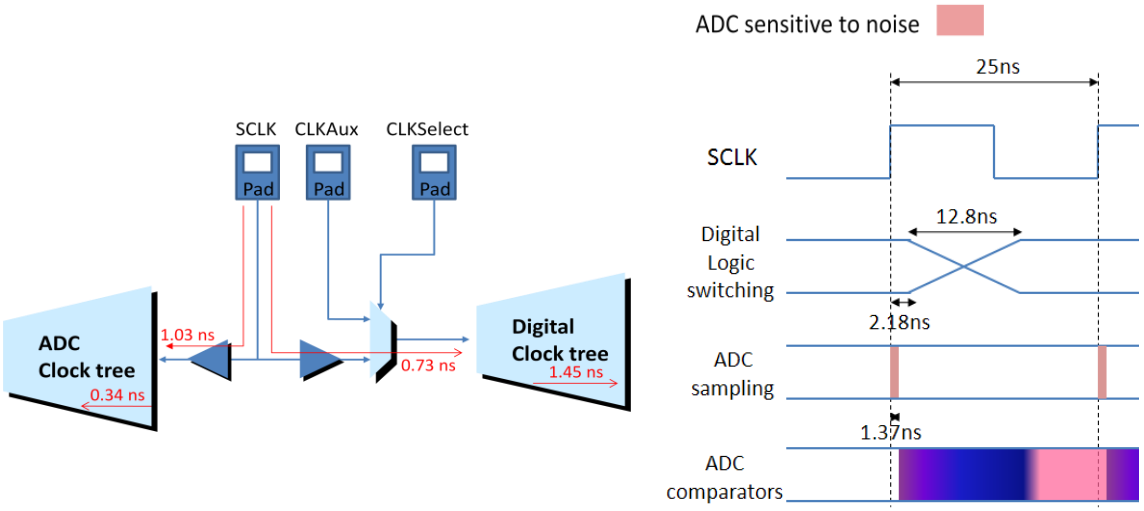


Figure 5.15 Clock scheme diagram

5.5.2 Package

Two different packages are foreseen for this prototype depending on the test phase. More details are provided in the next chapter.

- Pin Grid Array 181 (PGA181), see Figure 5.16. The 181-pin stubs are spaced at a pitch of 0.5 x 0.5 mm. The package body dimensions are 40 x 40 x 2.5 mm. The cavity for the silicon die is 12 x 12 mm.

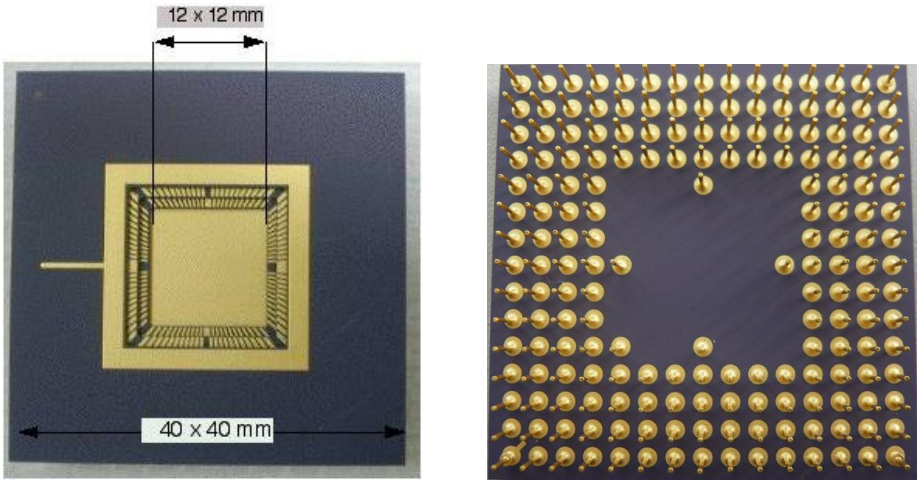


Figure 5.16 S-ALTRO PGA180 package

- Plastic Quad Flat Packages 208 (PQFP208), see Figure 5.17. The 208-pin stubs are spaced at a pitch of 0.5 mm. In this case, the package body dimensions are 28 x 28 x 3.0 mm and the cavity for the silicon die is also 12 x 12 mm.

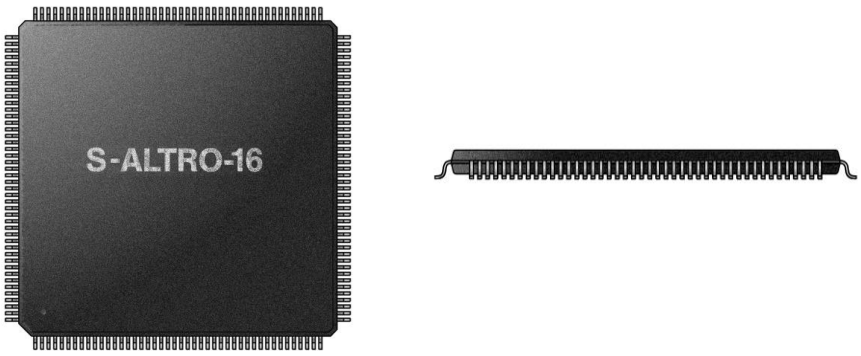


Figure 5.17 S-ALTRO CQFP208 package

5.6 S-ALTRO prototype mixed signal simulation

The objective is to simulate the full chain (CSA, ADC and DSP) to verify whole mixed signal chip assembling.

Figure 5.18 shows the mixed signal simulation block diagram. The detector model provides an analog signal similar to a real detector. The analog biasing configures the CSA. The digital test-bench is in charge of the communication with the S-ALTRO prototype sending commands and reading the outputs.

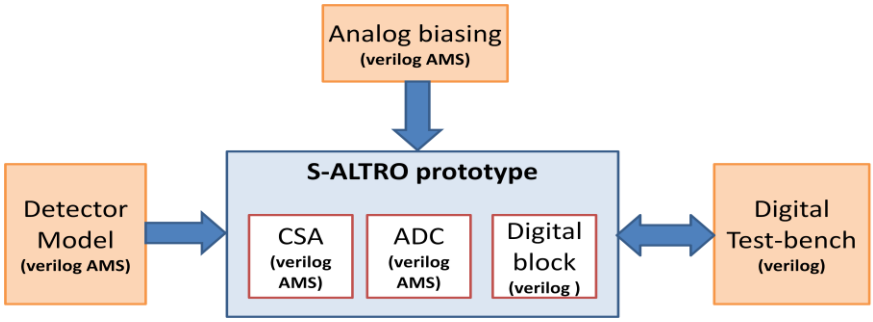


Figure 5.18 Mixed signal simulation

For this purpose, the analog blocks (CSA and ADC), the detector model and analog biasing were defined in Verilog AMS. The digital block was simulated at gate level using the functional view (Verilog) and the digital test-bench was implemented in Verilog.

The timing information was included in the simulation using different approaches. For the analog blocks, *Spectre* simulations of the extracted design were made to include the timing information in the Verilog AMS models. While for the digital block, the timing was extracted from *Cadence Soc Encounter* and back-annotated.

Finally, the simulations have shown that the pulse generated in the detector model is shaped by the CSA, sampled by the ADC, processed by the DSP and stored into the memories. Therefore, the assembling has been proven with these simulations.

Moreover, a specific simulation of the ADC and DSP synchronization is shown in Figure 5.19. The first signal corresponds to the external sampling clock, next two, to the ADC output and the DSP registers internal clock (fast corner). Last two signals represent the same case as before for the slow corner. The worst case margin is 15.4ns.

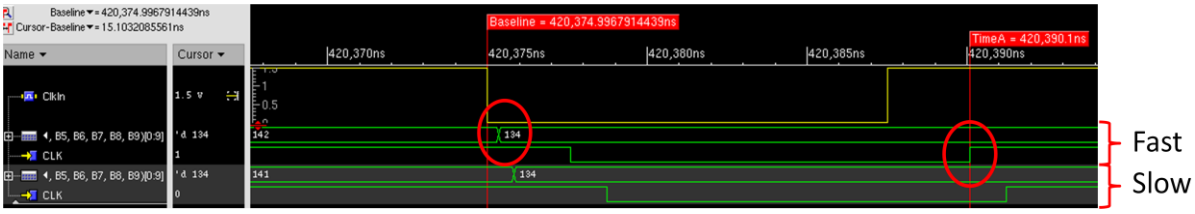


Figure 5.19 ADC output and DSP input simulation

Chapter 6 S-ALTRO Prototype Test Measurements

6.1 Introduction

This chapter describes the S-ALTRO prototype test board, the testing procedure and shows the most relevant test results. The tests are divided in 3 steps to isolate potential problems in the integration:

- CSA + ADC + Digital interface: The CSA and ADC have been tested and characterized by individual ASIC prototypes. Therefore, the objective is to validate their integration.
- DSP: evaluates the DSP behavior with respect to simulated outputs. Under the same configuration and inputs patterns, the tests in the lab and the simulations should have the same outputs for the digital processing.
- Full chain: the feasibility of the full chain integration is proved through measurements of noise and cross talk. Moreover, it is presented a detailed power consumption analysis and power pulsing technique.

The main objectives are the confirmation of the full integration feasibility, the verification of the power pulsing technique viability and the measurement of the power consumption reduction in the DSP.

6.2 Test board

A test board applies the stimulus signals to the device under test and measures its responses. This could be done with a single board where all the logic is included. However, the test board presented in this chapter has distributed logic to make it compatible to the current ALICE TPC back-end electronics ([ALICETPC]).

The architecture selected provides a grade of complexity to the tests, e.g. adding some extra synchronization with a control board. Nevertheless, it prepares the path for a fast connection to a real detector.

As explained in chapter 5, the S-ALTRO prototype offers a test channel where the block CSA, ADC and DSP are accessible individually. The test board also provides logic to access each block separately. This is a crucial issue in high integrated circuits.

Other important aspect in an ASIC is the final package. For the S-ALTRO prototype were foreseen two different options depending on the phase. The test board includes two sockets to be compatible with both packages: Pin Grid Array 181 (PGA181) and Plastic Quad Flat Packages 208 (PQFP208).

In the first phase, the measurements have been performed with a PGA181 package. Only ten samples were packaged in this phase. This kind of package has high input/output density and short electrical connections. However, the isolation between analog and digital inputs/outputs is very limited. For this last reason, this package is not optimum in terms of SNR and no measurements of effective number of bits or linearity are provided. Nevertheless, it is an economic solution which fulfilled the requirements of the first phase of the tests and it could be carried out in-house.

In a second phase, the remaining samples from the engineering run will be packaged in a PQFP208. This package has the inputs/outputs distributed around the four sides. The S-ALTRO prototype pad placement was optimized for this kind of package keeping the analog and digital domains isolated. A better SNR behavior is expected. Moreover, the benefits of using a classical SMD package are the soldering reliability and the manipulation simplicity.

A special care was taken with the analog input ports in the test board. Again, there are two configurations depending on the test phase. In the first test phase, a lemo connector connects an external pulse generator to all the S-ALTRO inputs. Each input has a jumper and a capacitor of 1.8pF, 3.2pF or even 88pF (depending on the configuration) which generates the input charge. On the contrary, in the second phase the S-ALTRO inputs will be connected to a real detector through HARWIN FIO 280R connector. The test board includes both input ports multiplexed.

Figure 6.1 shows a block diagram of the test board. For simplicity only components of the first test phase are included in this diagram. Figure 6.2 and Figure 6.3 show the front and back side of the test board.

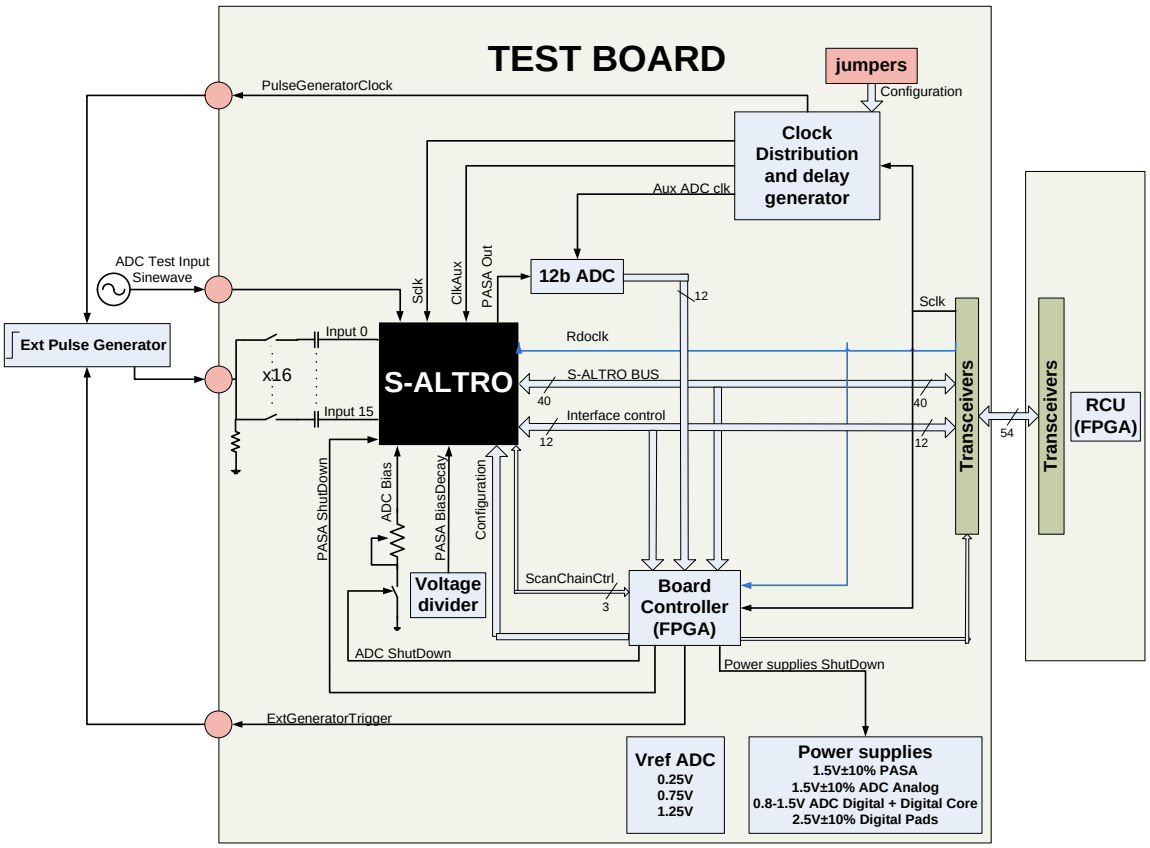


Figure 6.1 Test Board block diagram

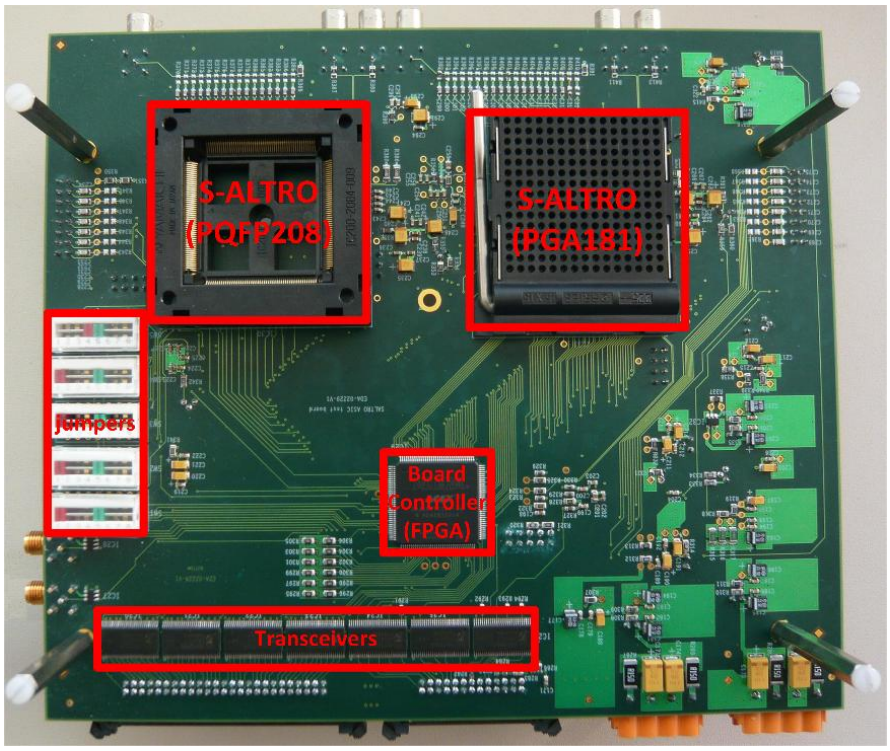


Figure 6.2 Test board front side

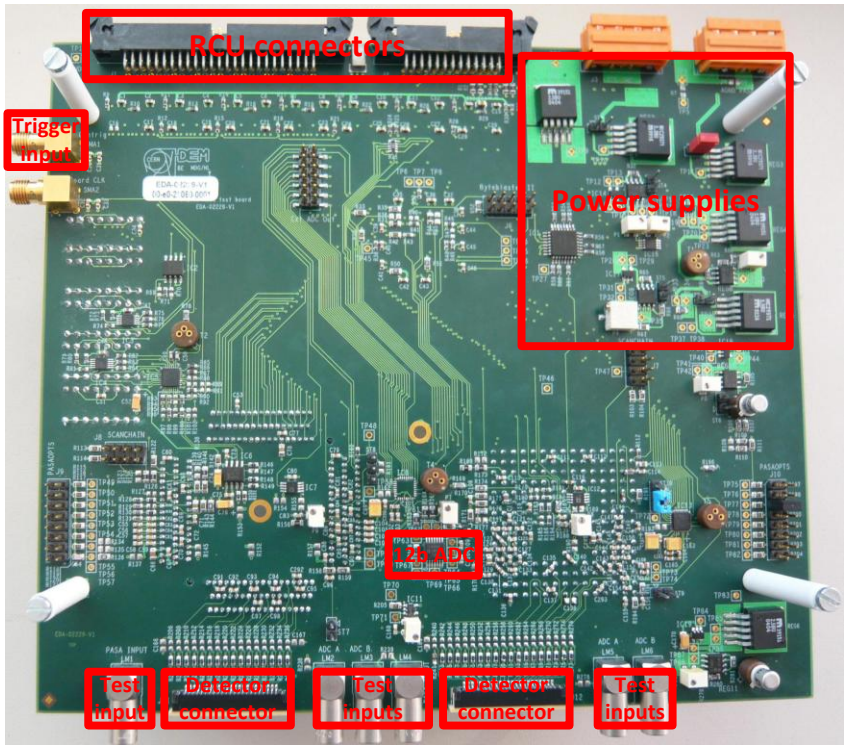


Figure 6.3Test board back side

- **Clock distributor and delay generator**

  The influence of the digital noise in the sensitive analog frontend is one of the most interesting aspects to study in this prototype. The S-ALTRO chip has the possibility of using different sampling clock phases to study this influence. See Figure 5.15.

  The ASIC AD9513BCPZ is used to distribute the clock in the test board. Moreover, it can add a delay between the sampling clock (SCLK) and the sampling clock delayed (ClkAux) for noise analysis purposes.

- **Power regulators**

  There are three power domains in the board: CSA, ADC analog and ADC digital/digital core/digital pads. The voltages shown in the Figure 6.1 come from the inputs 3.3V, 4V and 4V respectively.

  Linear voltage regulators have been used to define the power supplies. Voltage dividers were included to adjust with higher precision these values or even to modify as in the case of the digital core power supply. This flexibility in the power supplies allow, for example, testing the digital core below the nominal power supply. Moreover, the voltage regulator enables can be controlled by the board controller. This is necessary to test the power pulsing.

  Shunt resistors were added in each power domain to measure the power consumption per block.

- **Voltage divider**

  The voltage divider polarizes the feedback transistor of the CSA. Controlling the resistance in the feedback, we could control the time of discharge in the CSA. Therefore, we could modify the maximum pulse rate.

- **External ADC 12bits**

  The S-ALTRO prototype provides a test channel where the CSA has a direct output. This output is controlled by a switch. The analog CSA output is connected to an external ADC 12bits (AD9235) controlled by the board controller. This implementation was planned for debugging purposes.

- **Board controller**

  The board controller can be used for different functionalities.

  - Basic configuration of static parameters in the S-ALTRO.
  - Test of power pulsing changing dynamically the S-ALTRO configuration
  - Readout of raw data from the internal ADC, through the 40 bidirectional bus.

- Readout the external ADC 12bits connected to the CSA output.

- **Readout control unit**

  The Readout Control Unit (RCU) is in charge of sending the different commands and instructions to the S-ALTRO. It acts as master in acquisition mode and slave in readout mode. This unit is an evolution of the ALICE TPC RCU ([RCU]), which was adapted to the S-ALTRO modifications.

  The communication with the RCU can be a tedious task. To simplify the communication, a graphical user interface (GUI) was developed by Adams Szczepankiewicz. This GUI was implemented in Phyton ([PHYTON]).

  The RCU piles up the commands coming from the GUI and send them to the S-ALTRO prototype with the proper synchronization. In the case of a readout command, the RCU receives the data from the S-ALTRO, decodes the information and transfers the data to the computer. Finally, the GUI can plot or save the data in a file.

6.3 Test results

6.3.1 CSA + ADC + Digital interface

The objective in this test phase is to verify the CSA, ADC and digital interface functionality. The full chip is powered up, although the DSP functionality is bypassed at the moment. The digital interface is used to read the ADC data outputs stored in the memories. This test proves the communication and synchronization among the S-ALTRO prototype, the RCU board and the PC.

The input charge is generated from an external pulse generator connected to one of the lemo connectors (see Figure 6.3). The pulse charge depends on the generator voltage amplitude and the capacitor connected. During this test phase the input charge was constant, only the S-ALTRO analog configurations were modified.

It is important to mention that the input pulse charge can be delayed with respect to the acquisition window (level 1 trigger). In this way, more accurate pulse shape measurements are provided delaying the input charge pulse in steps of 5ns (keeping the sampling at 40MS/s).

Figure 6.4 shows the pulse shape for the minimum and the maximum peaking time and fixed gain. Figure 6.5 shows the pulse shape for the minimum and the maximum gain and fixed peaking time.

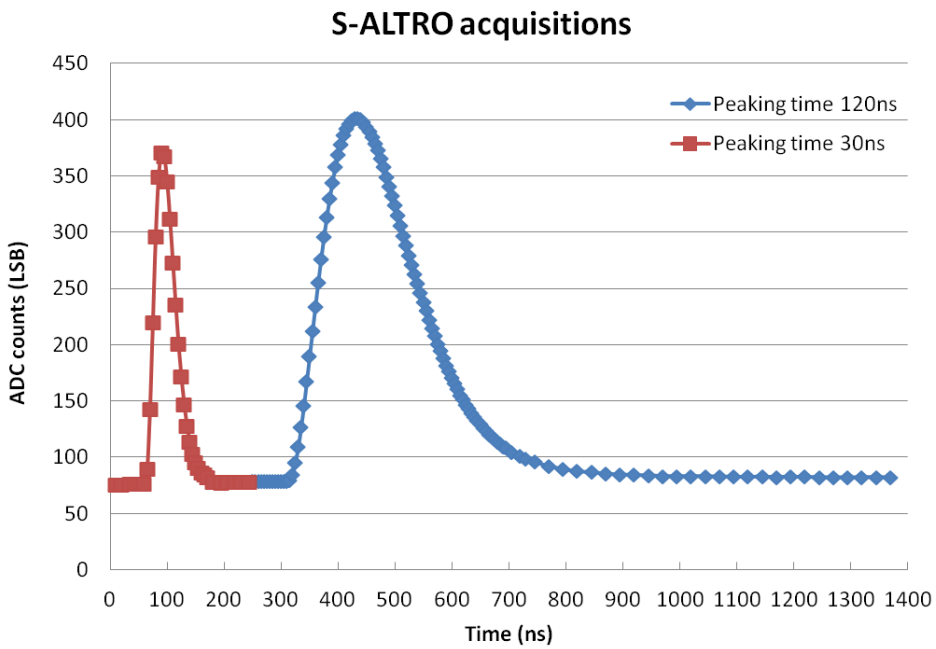


Figure 6.4 S-ALTRO acquisitions with different CSA peaking time configurations.

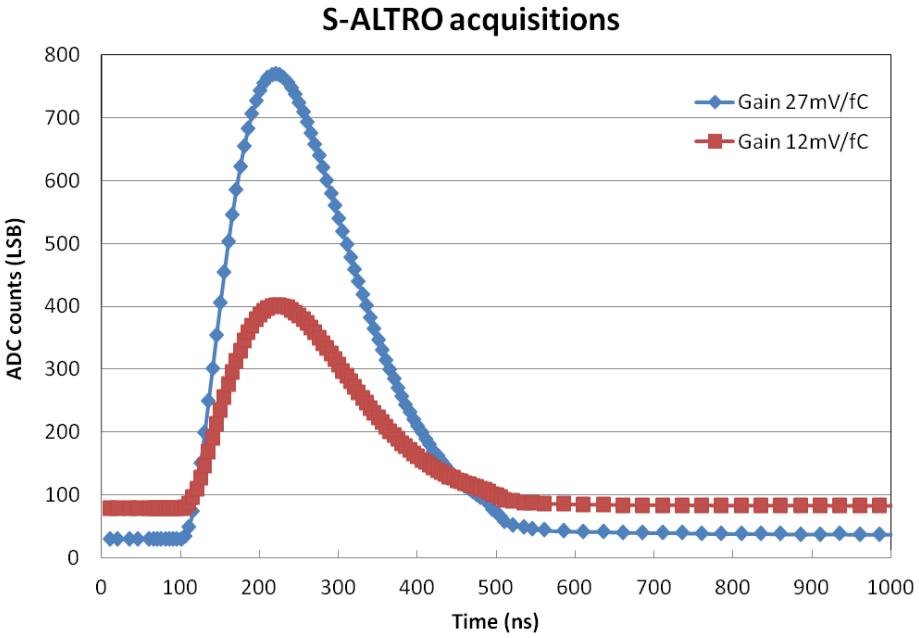


Figure 6.5 S-ALTRO acquisitions with different CSA gain configuration.

An important parameter to measure in the CSA is the gain variation with respect to the charge (linearity). Figure 6.6 shows the gain versus charge input for the CSA configured: gain 12mV/fC and peaking time 120ns. The measured gain is 10.6mV/fC with 1.9% variation.

While, Figure 6.7 shows the gain versus charge input for the CSA configured: gain 27mV/fC and peaking time 30ns. The measured gain is 22.56mV/fC with 0.9% variation in this case.

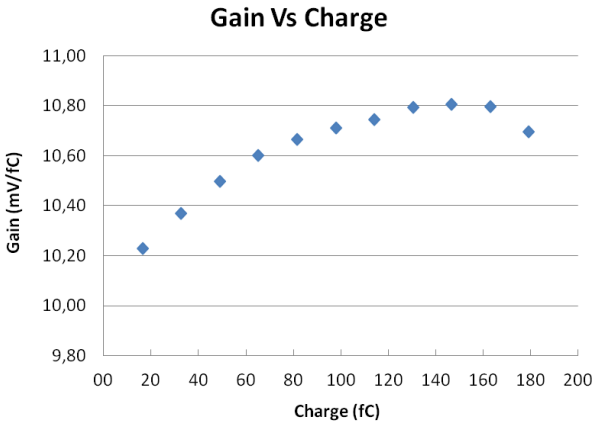


Figure 6.6 Gain Vs Charge
CSA configuration: 12mV/fC, 120ns,

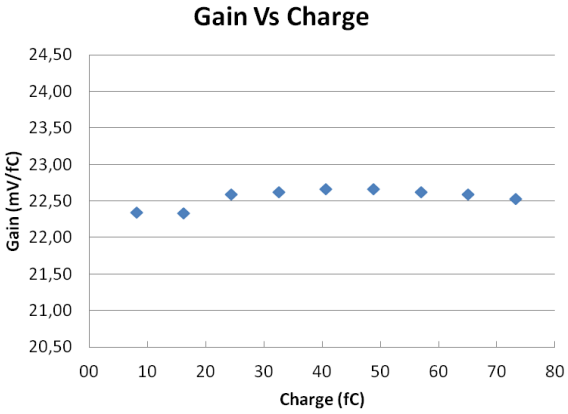


Figure 6.7 Gain Vs Charge
CSA configuration: 27mV/fC, 30ns,

6.3.2 DSP

In this test the analog circuitry is not powered. The input pattern is stored into the BC1 baseline memory and used later as input generator. Same patterns than the ones used to test the filters in simulation were used to test the filters in the lab.

Two different approaches are used to test the filters functionality:

- Store the DSP output with the filters bypassed and enabled. Afterward, both outputs are plotted and compared.
- Process a known pattern with a defined filter configuration in a simulation and in the lab. Later, both outputs are compared automatically by numerical computing software. Same test was repeated for different configurations. These tests prove that the digital filters behave as expected.

Figure 6.8 shows the behavior of the digital shaper. To calculate the filter parameters to correct the tails see ([ROSSEG]). Figure 6.9 presents the effect of the BC2. Finally, Figure 6.10 and Figure 6.11 show the combine effect of both filters. In this case, after the processing the output is ready for an efficient zero suppression.

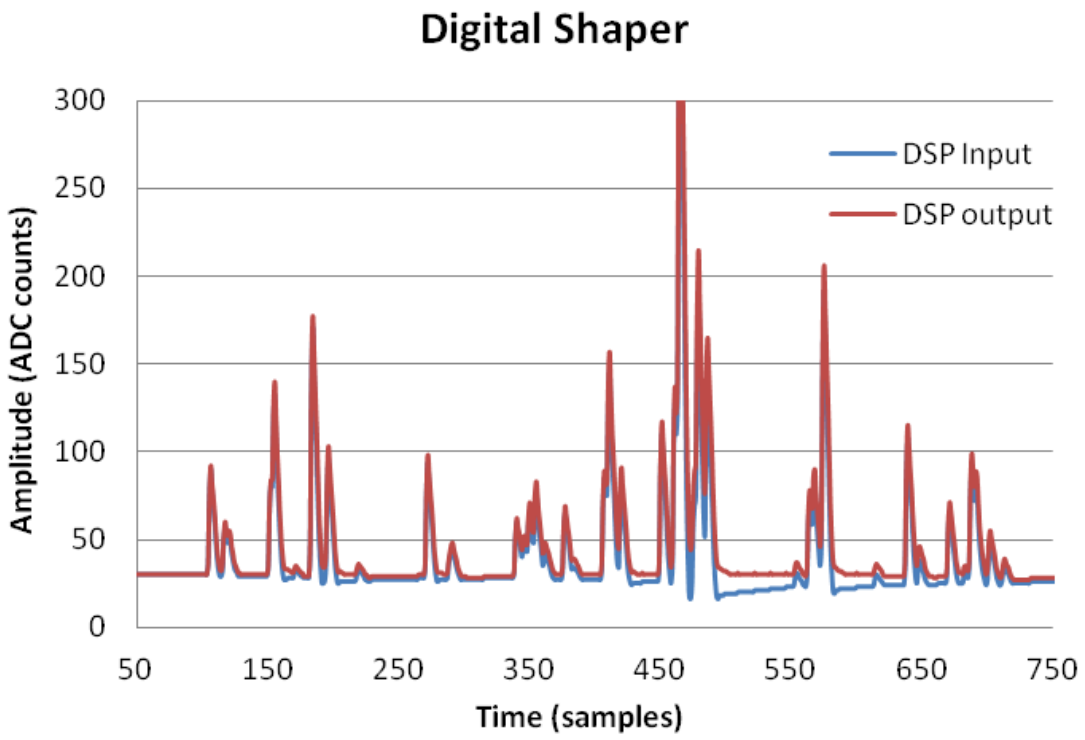


Figure 6.8 Digital Shaper

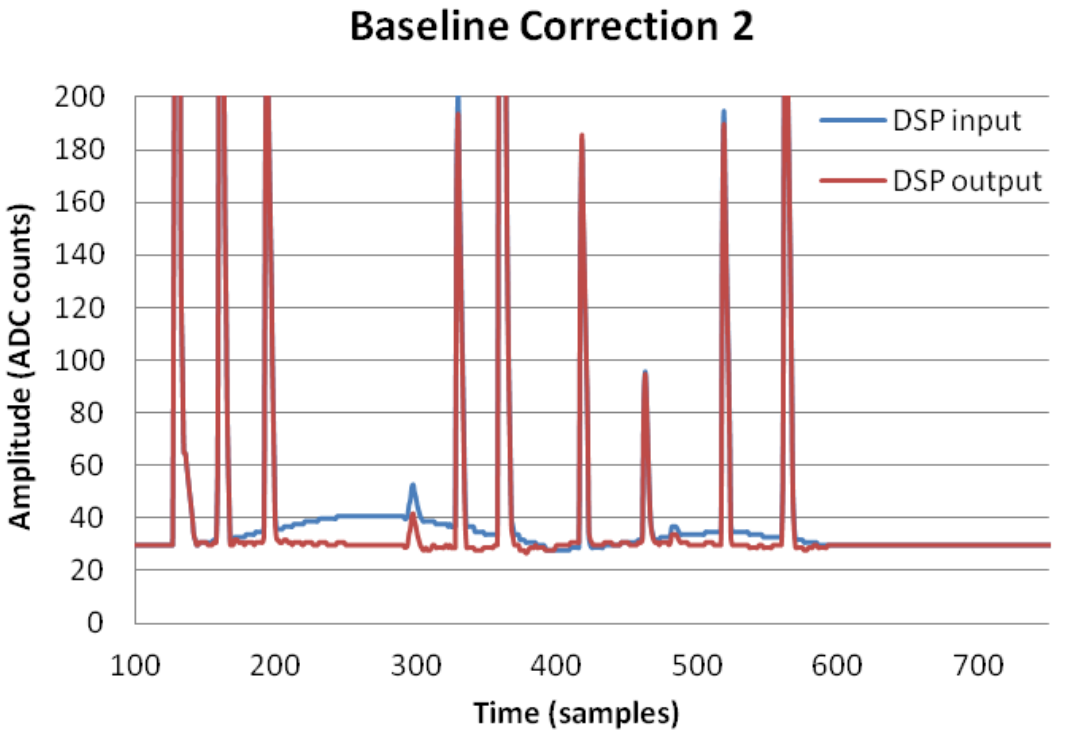


Figure 6.9 Baseline correction 2

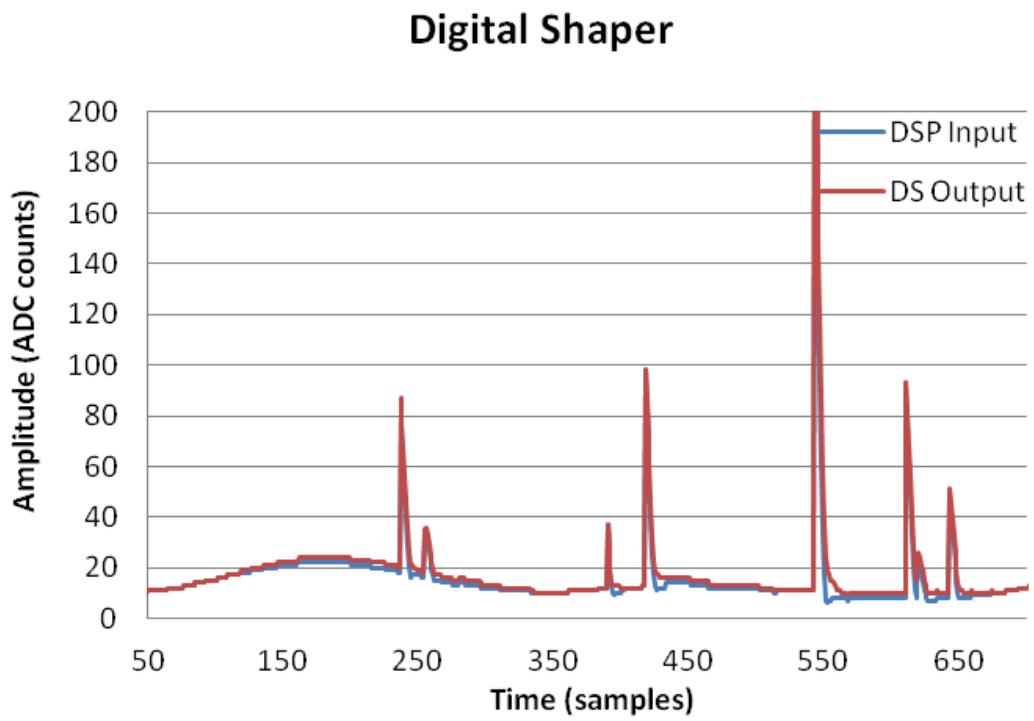


Figure 6.10 Digital Shaper

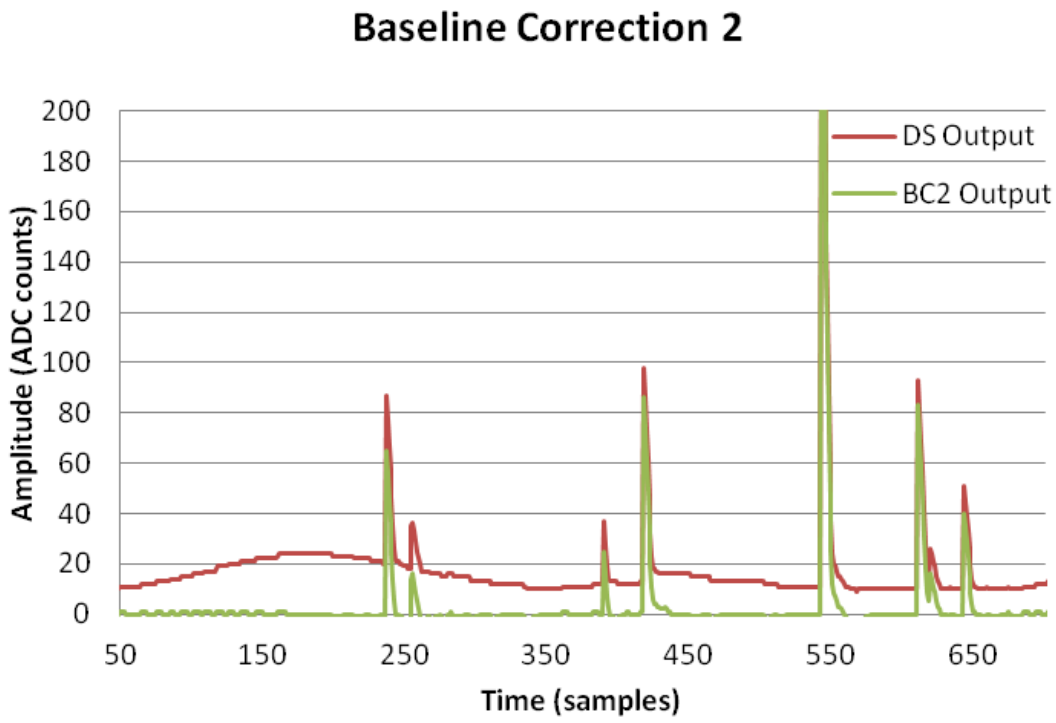


Figure 6.11 Baseline correction 2

6.3.3 Full chain

The full chain test consists on using all blocks (CSA, ADC and DSP) to process the input charge generated in the test board. This test proves that the data pass through all the blocks, measures the quality of the integration and power consumption of the different blocks.

The CSA shapes the analog input signal. The ADC converts to digital the shaped charge. The DSP processes the digital signals and stores them in the Multi-Event Memories (MEB). Posteriorly, the RCU reads the data from the MEB and decodes the information. Finally, the PC receives the decoded data and plots or saves the result.

Only if the full chain works properly, a pulse consistent with the analog and digital configuration will be plotted in the PC. Figure 6.12 shows the S-ALTRO output for the configuration defined in TABLE 6-1. This proves the S-ALTRO integration success.

To quantify the quality of the integration, next sections provide measurements of the crosstalk and signal to noise ratio.

TABLE 6-1 Full chain test configuration

Block	Configuration
Input charge	Pulse generator voltage: 300mV Capacitor on the test board: 1.8pF Attenuator: by 10
CSA	Peaking time: 120ns Gain: 12mV/fC
ADC	Sampling frequency: 40MHz
DSP	BC1: No DS: No BC2: Yes ZS: No

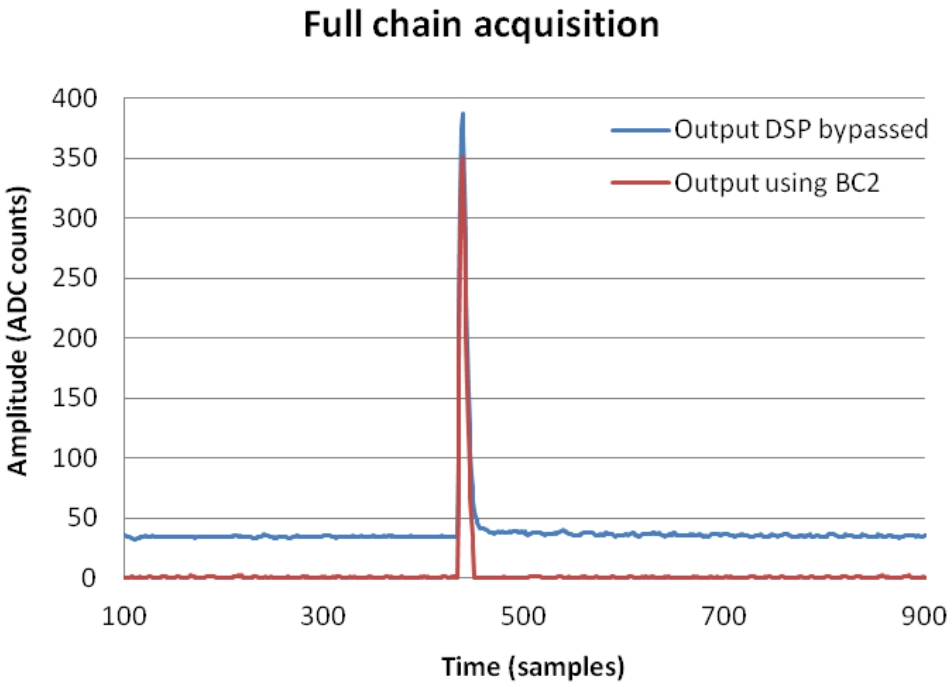


Figure 6.12 S-ALTRO prototype acquisition

6.3.3.1 Crosstalk

An important aspect of the full integration is the crosstalk between adjacent channels. To measure the crosstalk between channels a charge is introduced in one channel (aggressor). None of the adjacent channels (victims) are connected to an input charge.

In the ideal case, only the aggressor channel should measure data different than the baseline. However, in a real system a small part of the charge is detected in the adjacent channels. This can be caused by undesired capacitive, inductive or conductive coupling.

If the system is well isolated, the crosstalk and noise can have the same order of magnitude. Therefore, an average of at least five acquisitions was made to avoid measuring the noise. A full range signal is introduced in the S-ALTRO channel 15 (aggressor). Figure 6.13 and Figure 6.14 show the average of five acquisition readout of channels 15 and 14.

The crosstalk depends on the channel and the features of the aggressor. This section presents one of the worst cases measured. In particular, an aggressor of max amplitude at any channel would have as maximum influence of 0.3% in the victim.

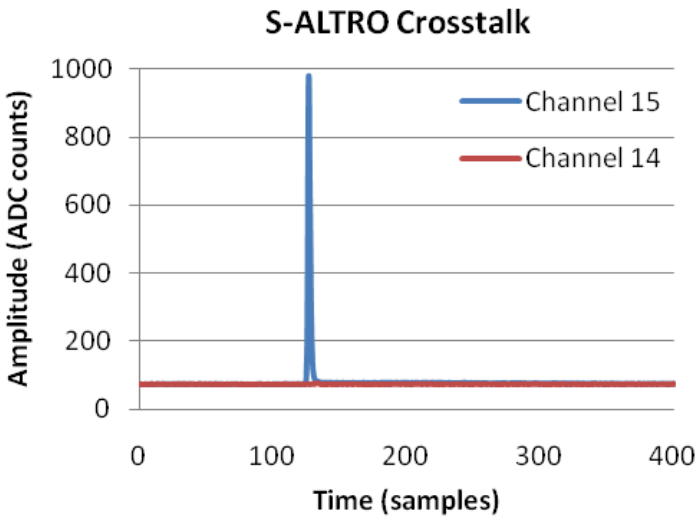


Figure 6.13 Crosstalk test. Channels 15 and 14 readout.

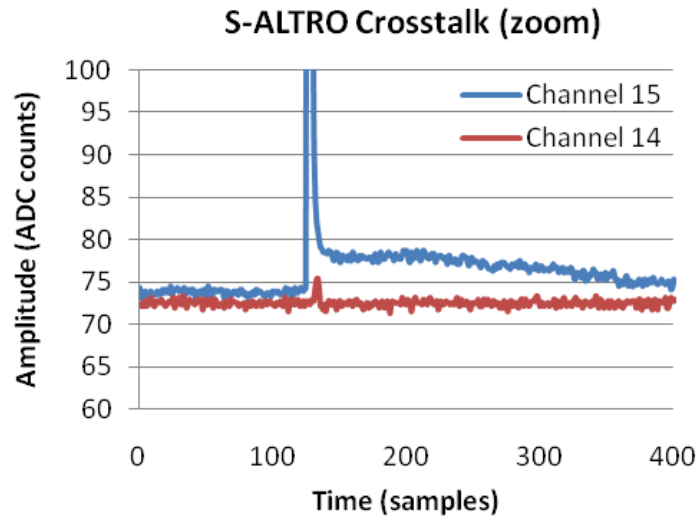


Figure 6.14 Crosstalk test. Zoom of the channels 15 and 14 readout.

6.3.3.2 Noise

The baseline noise is measured as the root mean square of thousand acquisitions. Same procedure was followed to measure the noise at peak of the pulse. Both results are similar. Low noise guarantees success integration with low distortions caused by the different clock domains.

The noise in the S-ALTRO prototype is approximately 0.5 LSB rms. This is an excellent result considering the complexity of the integration.

Figure 6.15 shows the noise distribution per channel for two CSA configurations. Both cases have shown a very constant noise per channel. This noise is measured in a dedicated package were the analog inputs were not bound to isolate the noise coming from the board.

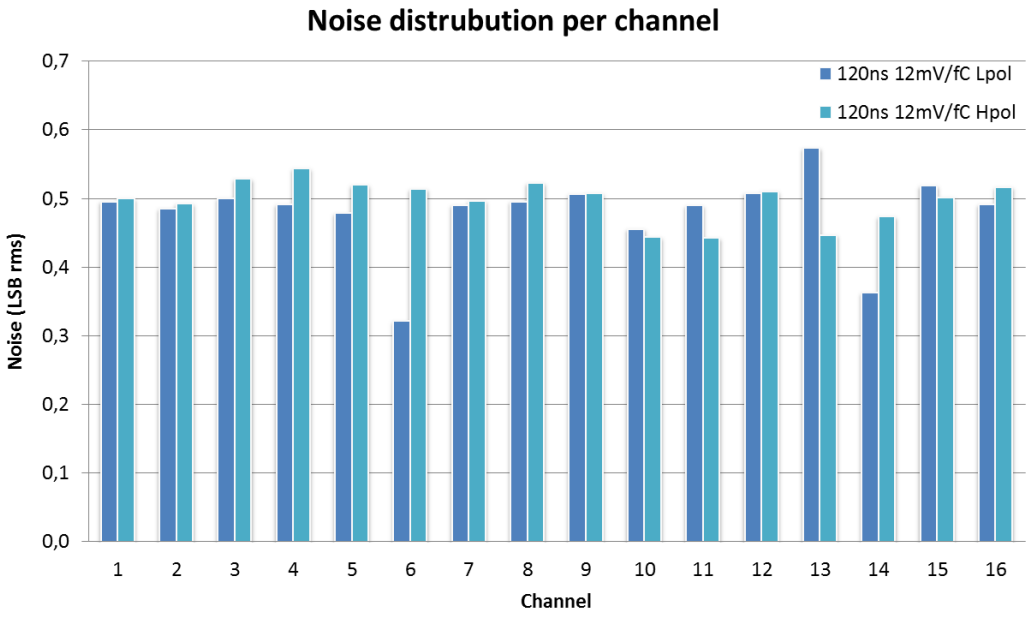


Figure 6.15 Noise distribution per channel

As explained in the previous chapter, the sampling clock phase was design to minimize the noise introduced in the analog sensitive blocks. The S-ALTRO prototype gives the possibility of using an external sampling clock to study the influence of this clock phase in the system noise. Using the clock distributor installed in the test board were tested several clock phase configurations. Figure 6.16 shows the noise results with respect to the sampling clock phase.

It is concluded that there is not a significant noise variation depending on the clock phase. This fact proves that the isolations presented in chapter 5 were enough to avoid the digital noise in the ADC sensitive blocks.

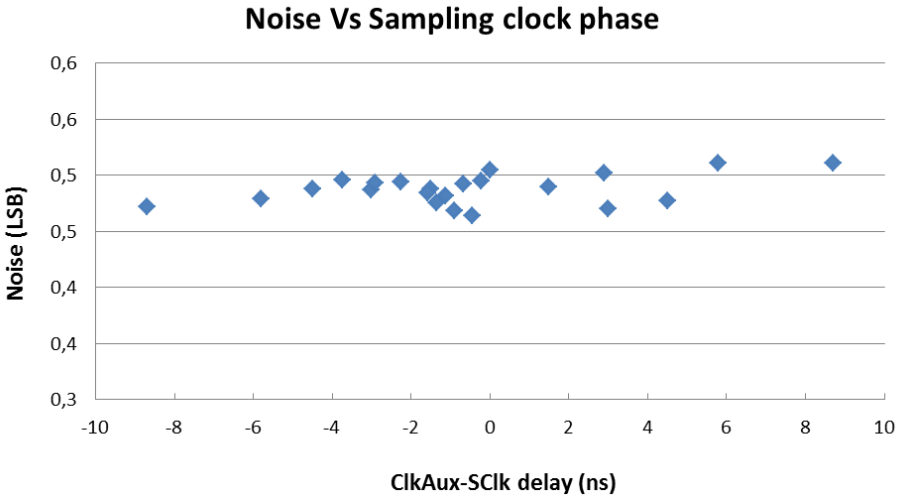


Figure 6.16 Digital noise depending on the sampling clock phase

6.3.3.3 Power consumption

The power consumption is measured using the shunt resistor per power domain installed in the test board. Figure 6.17 shows the power consumption distribution at 40MHz sampling frequency of the three S-ALTRO main blocks: CSA, ADC and DSP. The S-ALTRO consumes 756mW in continuous running at nominal power supply and 40MHz of sampling frequency.

As shown in the next figures, the digital power increase considerably during acquisition and readout window. Therefore, the total digital power depends on the trigger rate and the trigger rate depends on the detector.

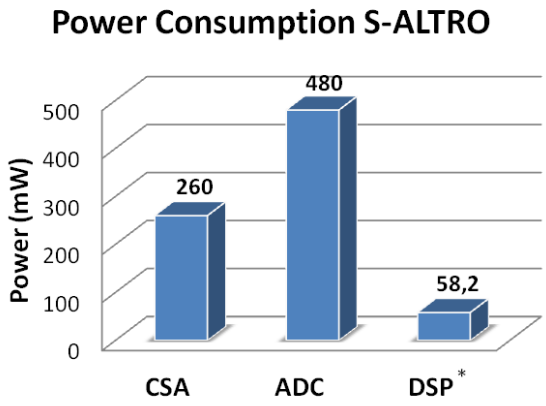


Figure 6.17 Power consumption distribution at 40MHz sampling frequency.
** considering trigger rate of 2%.*

Figure 6.18 shows the power consumption during an acquisition for different processing modes of operations at 40MHz sampling frequency:

- Orange line: all filters are bypassed.
- Blue line: the BC1 filter is active. This filter uses the baseline memory to subtract a known pattern. Most of the power is consumed in the readout of the baseline memory.
- Red line: BC1 and DS filters are active. The DS consumes most of the power of the processing chain.
- Green line: BC1, DS and BC2 are active. There is no significant difference in power.
- Purple line: full processing chain + zero suppression active. The significant power reduction is due to the reduction in the amount of data to be written in the MEB.

Figure 6.19 shows the readout power consumption at 40MHz readout frequency of 16,000 samples (1,000 samples per channel) stored in the S-ALTRO memories. This power corresponds to the memory read accesses and it is considerably higher than the acquisition power consumption. This power can be significantly reduced using the zero suppression.

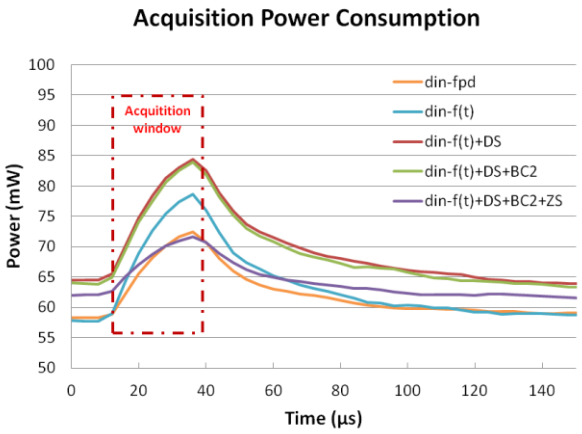


Figure 6.18 Acquisition power consumption for different modes of operation at 40MHz

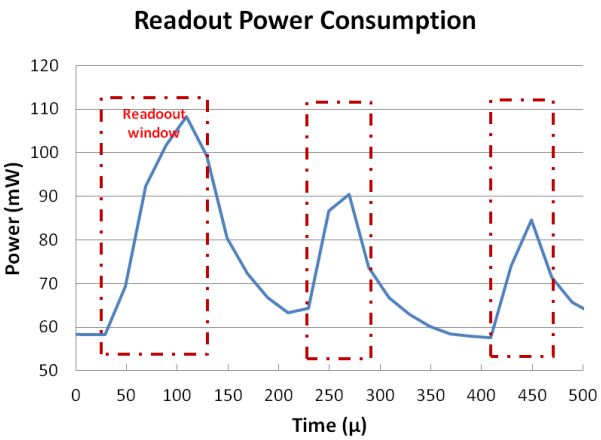


Figure 6.19 Readout power consumption (max acquisition size of the 16 channels at 40MHz)

As shown in eq. 4.39, the dynamic power consumption of a CMOS logic circuit can be reduced decreasing the frequency and power supply. Figure 6.20 shows the relation of the digital power with the sampling frequency. The power is reduced to less than one third at 10MHz sampling frequency.

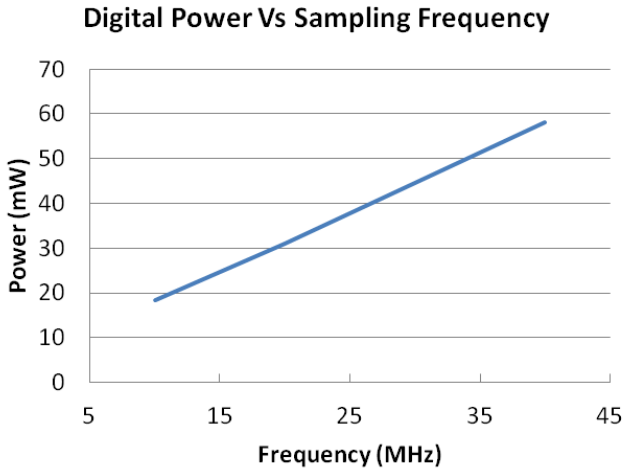


Figure 6.20 Digital power versus sampling frequency

Another parameter that has significant influence in the digital power is the supply voltage. Last results were measured at nominal power supply, V_{DD}=1.5V. Figure 6.21 shows the relation of the power supply with the digital power. Unfortunately, the test system has some synchronization problems with power supplies below 1.1V. In that case, the RCU is not able to read all the channels. In any case, it is concluded that the digital power would be reduced to 25% using V_{DD}=0.8V.

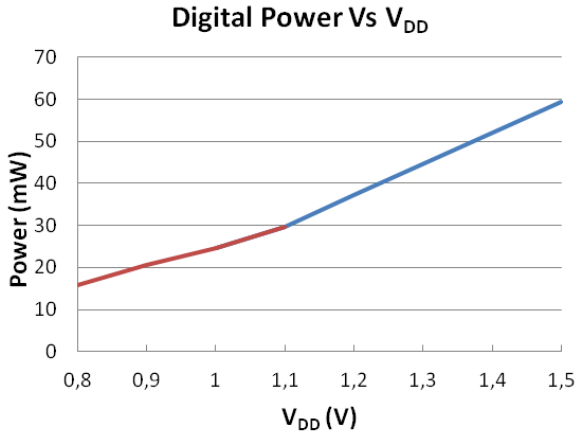


Figure 6.21 Digital power versus power supply

Finally, some tests at 10MHz sampling frequency were performed to compare the results with its predecessor. Figure 6.22 shows the instantaneous digital power during acquisition reported in ([BOSCH2]). Figure 6.23 shows the S-ALTRO digital power at the same conditions. New design and technology has reduced to 28% the digital power consumption.

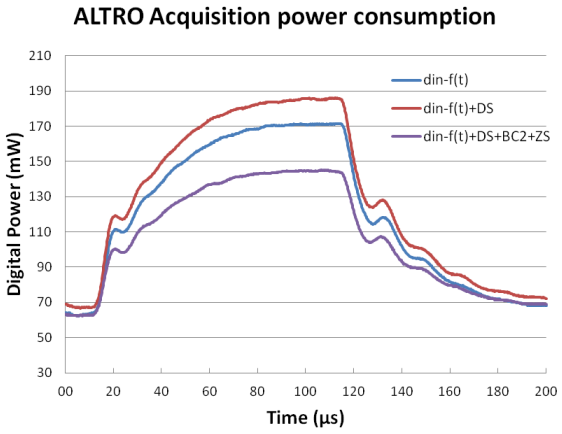


Figure 6.22 ALTRO power consumption during acquisition at 10MHz

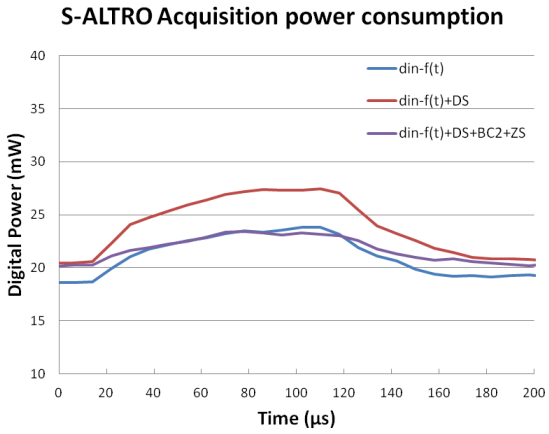


Figure 6.23 ALTRO prototype power consumption during acquisition at 10MHz

6.3.3.4 Power pulsing test

The power consumption presented until now considers the system running continuously. The S-ALTRO prototype includes a shut-down and power-up system which allows to the system to work with reduced duty cycle.

The CSA offers a shut-down mode configurable by one of the pins. This mode switches off the bias current sources of the full circuit bringing the system to a standby mode. Similar circuit is

implemented in the ADC. The ADC also provides a resistor outside of the chip to set the current source. Therefore, the approach of disabling the current sources is removing the external resistor. Finally, the DSP is brought to a stand-by state disabling the sampling and readout clocks. The power supplies remain enabled to keep all the configuration and memory data information.

The main parameter to determine in the power pulsing is the recovery time after a power-up. Figure 6.24 shows the amplitude of the pulse charge depending on the power-up delay. In this test, the input pulse amplitude is constant. However, the delay between the power-up instruction and the acquisition level 1 trigger has been varied to measure the limits. The pulse amplitude is distorting below 60µs delay. It is concluded that a power-up recovery time of 100µs is a safe margin to consider for the S-ALTRO prototype power pulsing.

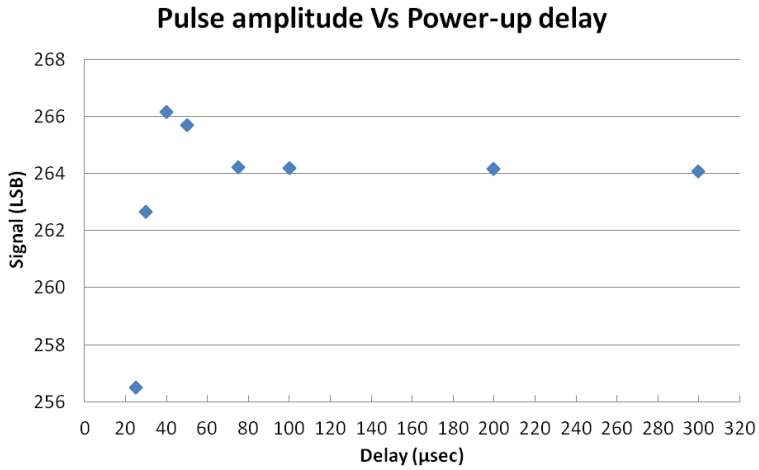


Figure 6.24 Pulse amplitude versus power-up delay

Figure 6.25 shows the time profile of the power evolution during an acquisition using the power pulsing technique. In this example the readout time is consuming most of the time and power. There are two considerations to be made:

- This example shows the worst readout case, where no zero suppression is applied. The readout corresponds to 16 channels with the maximum buffer size. Moreover the readout is made at 40MHz (limited by the RCU), while the S-ALTRO chip was designed to read data at 80MHz.

- The power pulsing could be improved disabling the analog blocks (CSA and ADC) after the acquisition. These blocks are not necessary for the readout and consume most of the power. Unfortunately, the RCU does not allow doing this.

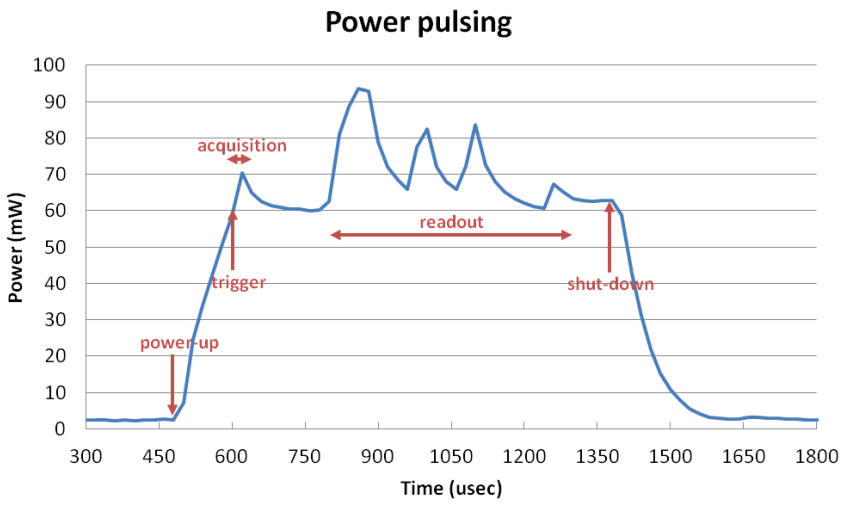


Figure 6.25 Power pulsing

In any case, the results are very promising. Figure 6.26 shows the power consumption on running mode and power pulsing (ILC and CLIC). For the ILC (5Hz rate) the power consumption has been reduced by factor 60, while for the CLIC (50Hz rate) has been reduced by factor 18.

	CSA	ADC	DSP	TOTAL
Running	164	527	65	756
ILC Power pulsing	2.85	9.1	0.5	12.45
CLIC Power pulsing	9.4	29	3.4	41.8

Figure 6.26 S-ALTRO prototype power consumption

6.4 Conclusions

This chapter has presented the test results of the S-ALTRO prototype. The measurements have shown very satisfactory results. The main objectives of full integration feasibility, power pulsing technique viability and power consumption reduction in the digital block have been proven.

The analog and digital functionality was tested and behaved satisfactorily. Some examples of digital processing were presented. Digital filters have been compared with respect to simulations by numerical computing software.

The crosstalk measured was of 0.3% and the baseline noise 0.5 LSB rms. These are excellent results considering the complexity of the full integration with sensitivity analog filters, ADCs and DSP. No significant noise increase was measured using different clock phase between the ADC and the DPS clock. This proves the good isolation between the analog sensitive block and the digital noise.

The S-ALTRO prototype has a power consumption of 756mW at 40MHz sampling frequency and continuous running. This power is divided among the different blocks as follows: CSA 164mW, ADC 527mW and DSP 65mW. The main power consumption is concentrated in the ADC. Therefore, future designs will have to focus on improving the ADC power consumption.

Two possibilities of reducing the digital dynamic power consumption were tested. The power is reduced to less than one third at 10MHz sampling frequency. On the other hand, the power can be reduced to 25% keeping the sampling frequency to the nominal and reducing V_{DD} to 0.8V.

The digital power was compared to its predecessor, the ALTRO. Without considering the power pulsing, the S-ALTRO prototype digital power consumption was reduced to 28%.

Finally, the power pulsing technique was proved and reported great results. The system can power-up and shut-down with a duty cycle of 0.5%. This duty cycle has been defined in the future TPC as a main requirement to reduce the power consumption. In conclusion, for the ILC (5Hz rate) the power consumption has been reduced by factor 60, while for the CLIC (50Hz rate) has been reduced by factor 18.

Chapter 7 Conclusions

7.1 Presented work

This thesis has covered the design of a novel front-end electronics design for time projection chamber detectors, the S-ALTRO. The preceding chapters have explained the full process from the study of the future detector specifications and current readout system status to the conceptual description of the circuit, filter optimization, design and test of the S-ALTRO prototype.

The first chapter has studied the future detectors and their requirements. In general, future detectors aim at very high spatial resolution, requiring smaller pad sizes (in the order of few square millimeters) and higher sampling rates. These requirements call for highly integrated low-power front-end electronics. The key design aspect is, therefore, the minimization of the power consumption. Moreover, regarding the digital signal processing circuits, the most important design criteria is the digital noise performance, which will contribute to the detector spatial resolution, the physical size of the circuit and the versatility to cover a broad range of applications. These requirements are a significant challenge in the design of a novel front-end electronics.

The second chapter has presented several readout electronics designs and proven that none of the existing or in-development front-end electronics designs meet the requirements presented in the first chapter. A common limitation of all the readout systems studied is the scale of integration. For example, the ALICE TPC readout system implements the analog filters in a separate chip, which makes the system inadequate for future detectors due to the high integration requirement.

At the end of the chapter, a first outline of a possible front-end solution is presented. The novel front-end electronics for TPC detectors is an evolution of the ALICE TPC front-end electronics.

Although it inherits its main features, higher integration, lower power consumption, larger flexibility and further functionality are included. This architecture meets all the requirements presented in the first chapter.

The third chapter has detailed the concept of the novel front-end electronics for TPC detectors, the S-ALTRO. This ASIC provides the integration of multiple channels consisting of front-end preamplifier, shaper, analog-to-digital conversion and digital signal processor integrated in a single integrated circuit. Moreover, new concepts as the 3D zero suppression or novel chip interface are presented.

This ASIC integrates 64 channels in 130 nm CMOS technology with an estimated power consumption of 0.5mW/channels using power pulsing technique. The S-ALTRO is the first ASIC with such high integration ever developed for HEP applications.

The fourth chapter has studied several filter optimizations of the S-ALTRO processing chain and has compared them with respect to its predecessor the ALTRO chip. The processing chain includes the Baseline Correction 1 (BC1), Digital Shaper (DS) and Baseline Correction 2 (BC2).

- The BC1 was optimized on SNR and flexibility. The SNR has increased 1.5db due to a shifting in the subtraction from the baseline memory. Moreover, the IIR filter outside the processing windows is now configurable, following the signal more accurately. These improvements increased the hardware resources by only 7.9% with respect to the old design.

- The DS is the main filter of the processing chain by area and power consumption. Therefore, a great deal of effort was made to study the optimum configuration for HEP applications. Finally, it was concluded that the transposed direct form II IIR is the optimum filter architecture. This improvement has reduced the area to 2/3 and the power consumption to approximately half.

- The BC2 was optimized on SNR and flexibility too. The SNR was slightly increased by 0.34db with respect to the ALTRO design. However, greater flexibility was achieved configuring the number of taps used in the FIR filter.

Moreover, the interconnection of the filters was optimized with respect to its predecessor. A common 13-bits fixed-point arithmetic is kept in the full processing chain. Only at the end of the processing chain a round-off to 10-bits is performed.

Another aspect studied was the reduction of the power consumption by decreasing the power supply voltage. The optimization was made by reducing the V_{DD} (followed by longer time delays), to the minimum value that is still compatible with the working frequency of the system. The critical timing path of the digital block is the DS, namely the multipliers of the IIR filters feedback paths, this was studied in order to optimize the power consumption whilst ensuring the functionality remained unaffected. In simulation the supply voltage was reduced to 0.8V, reducing the power consumption in the digital circuit to 45% with respect to what it would be

obtained if the nominal supply voltage (1.2 V) was used, but without degrading the working frequency of the system.

In summary, the filter optimizations presented in the fourth chapter provide the following improvements: the power consumption of the digital block has decreased to 40%, the hardware resources have been reduced to 80% and the SNR has been increased 7.9 db.

The fifth chapter has presented the prototype design. The main differences with respect to the final S-ALTRO chip are the number of channels integrated and the use of the ALTRO interface. Both modifications are justified and do not deviate from the main objective, which is the proof of principle of the novel architecture. The reduction of the number of channels has a purely economic reason for prototype production. The manufacture of 16 channels is one fourth of the cost. The decision of using the previous interface (ALTRO) is based on reduction of the testing time. For instance, the compatibility with the old system allows re-using the back-end electronics to connect the system to a real detector. Nevertheless, this prototype keeps the main high integration objective and the digital filters presented in Chapter 4. This chapter has also presented digital block layout process (floorplanning, placement, routing, timing calculation, power estimation and simulation) and mixed signal verifications of the whole chip.

Finally, the sixth chapter has presented the S-ALTRO prototype measurements. Two of the parameters which quantify the feasibility of the full integration are the noise and the crosstalk. The crosstalk measured in the victim channel is 0.3% with respect to its aggressor channel, and the noise is 0.5 LSB rms. These are excellent results considering the complexity of the full integration. On the other hand, no significant noise increment was measured shifting the clock phase between the ADC and the DSP clock. This proves the good isolation between the sensitive analog comparators and the digital clock.

The analog and digital functionality corresponds exactly to the simulations provided in the different chapters. The digital processing chain has been compared with simulations by numerical computing software and proved that there is no difference.

The S-ALTRO prototype consumes 756 mW at 40 MHz sampling frequency and continuous running. This power is divided: CSA 164 mW, ADC 527 mW and DSP 65 mW. These numbers shows that the main power consumption is concentrated in the present ADC.

Moreover, the digital power was compared to its predecessor in comparable working conditions. The S-ALTRO prototype digital power consumption was reduced to 28 % of its predecessors consumption.

Finally, the power pulsing technique was shown to provide good results. The full system can power-up and shut-down with a duty cycle of 0.5% (the same as the future TPCs specifications). This can make the readout system to work at 0.5% duty cycle reducing its power consumption to 28.1 mW for 16 channels.

In conclusion, a solution for future TPC detectors has been presented and the main features of the architecture have been proven. For instance, the integration of the analog front-end, the

analog-to-digital conversion and the digital processing in single silicon chip is feasible. The digital filters behave as expected with reduced power consumption and the power pulsing technique has worked for a duty cycle of 0.5 %.

7.2 Future work

After the good results and performance of the S-ALTRO prototype, there are two different lines of work:

a) Use of the S-ALTRO prototype in real detectors:

The work presented in this thesis was part of the framework EUDET which aims at supporting the detector R&D in Europe for the future International Linear Collider. The S-ALTRO chip has provided a readout solution to the community working on the detector R&D.

The University of Lund, which is one of the members of the EUDET collaboration, has been studying and designing the integration of multiple S-ALTRO chips in a Front-End card ([FEC-MCM]). The positive results of the S-ALTRO prototype allow continuing the multi-chip integration.

For this purpose, the remaining naked silicon chips will be packaged using PQFP208 package. At that moment, the yield analysis will be provided. This package was not used for the first test due to its high price for low number pieces.

Together with integration of multiple chips, another important objective is the characterization of the system using a real detector connected by GEMs and MicroMegas. This task will be carried out by the EUDET collaboration.

b) Next phase of the S-ALTRO design project:

The feasibility of the architecture has been proven with this prototype. However, the final integration of 64 channels requires a major improvement in the power consumption of the analog blocks.

The CSA and ADC power consumption must be reduced. The CSA will be re-designed. There are three different approaches for the ADC block: improve the current design, investigate other ADC architectures (e.g. asynchronous successive approximation) or procure a low power ADC IPs from industry.

On the digital side, the DSP has been proven and satisfies the requirements. However, the MEB controller needs to be re-designed to support continuous write and read operation. In this case, the use of dual port memories is highly recommended.

This new controller should write continuously into the memory in a programmable ring address space. Two configuration registers define the ring address space: the start address and the

memory depth. Moreover, the maximum number of samples after the trigger (post trigger samples) is also defined in a register. In conclusion, the memory depth defines the number of samples to store, and the post trigger sample register defines the offset with respect to the trigger.

Finally, as mentioned in chapter 5, this prototype has kept its predecessors interface for connectivity with the existing back-end electronics. Nevertheless, it is planned that this interface will be removed in the final S-ALTRO chip. This thesis has proposed another interface based on 16 address/data lines (CMOS) and 4 control lines. Moreover, the possibility of using a serial interface is being considered.

References

[ALICEDAQ]. "The ALICE DAQ: current status and future challenges." By M. Arregui. CHEP2000 International Conference on Computing in High-Energy and Nuclear Physics, 2000.

[ALICERCU]. "The ALICE TPC Readout Control Unit." By R. Campagnolo, A. Junique, L.Musa et al. C. González Gutiérrez. Puerto Rico: Proceeding of the 2005 IEEE Nuclear Science Symposium and Medical Imaging Conference, October 23 - 29, 2005.

[ALICETPC]. *"Technical Design Report of the Time Projection Chamber".* ALICE Collaboration, ISBN 92-9083-155-3, 2000.

[ALTRO]. "ALICE TPC Readout Chip User Manual." CERN, 2002.

[BARON]. "AFTER, and ASIC for the Readout of the Large T2K Time Projection Chambers." By E. Delagnes, D. Calvet, X. de la Broise, A. Delbart, F. Druillole, J-F Fallou, E. Mazzucato, E. Monmarthe, F. Pierre, A. Sarrat, E. Zonca, M. Zito P.Baron, 1865 - 1872 . Nuclear Science Symposium Conference Record, 2007.

[BLUM]. "Particle Detection with Drift Chambers." By W. Riegler, L. Rolandi W. Blum. Springer, 2008.

[BOKHARI]. "The ASDQ ASIC for the Front End electronics of the COT." By W. Bokhari et al. CDF Note 4515, 1999.

[BOSCH1]. "The ALTRO chip: a 16-channel A/D converter and digital processor for gas detectors." By R.E., de Parga, A.J., Mota, B., Musa, L., Bosch. Nuclear Science Symposium Conference Record, 2002 IEEE, pp. 566 - 570 vol.1, 10-16 Nov. 2002.

[BOSCH2]. "Study and Design of the ALICE TPC Front-End and Readout Electronics for the CERN LHC." By Raul Esteve Bosch. 2003.

[CERN]. "CERN (European Organization for Nuclear Research)." *http://www.cern.ch.*

[CHRIST]. "32-channel TDC with on-chip buffering and trigger matching." By J. Christiansen. London: 3rd Workshop on Electronics for LHC Experiments, 1997.

[CLIC]. "The Compact Linear Collider Study." *http://clic-study.web.cern.ch/CLIC-Study/intro.html.*

[Detectors]. *http://public-old.web.cern.ch/public-old/Content/Chapters/AskAnExpert/Experiments-en.html.*

[FEC-MCM]. *http://www.eudet.org/e26/e28/e86887/e105928/EUDET-Memo-2010-30.pdf.*

[FRANCA]. "A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process." By Hugo França-Santos. Geneva, 2009.

[GERACI]. "Adaptative Digital Spectroscopy in Programable Logic." By A. Di Odoardo, S. Riboldi, and G. Ripamonti A. Geraci, 2765 - 2772. TRANSATIONS ON NUCLEAR SCIENCE, 2000.

[GERD]. "Design and characterization of an Analogue Amplifier for the Readout of Micro-Pattern Gaseous Detectors." By Gerd Trampitsch. Doctoral thesis, 2007.

[GERD]. "Design and Characterization of an Analogue Amplifier for the Readout of Micro-Pattern Gaseous Detectors." By Gerd Trampitsch. Geneva, 2007.

[GIOMAT]. "MICROMEGAS: a high-granularity position-sensitive gaseous detector for high particle-flux environments." By Ph. Rebourgeard, J.P. Robert, G. Charpak Y. Giomataris, 29-35. NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, 1996.

[ILC]. *ILC (International Linear Collider).* http://www.linearcollider.org.

[KAUKHER]. "A Study of the Readout Electronics Based on TDC for the International Linear Collider TPC Detector." By O. Schafer, H. Schroder, R. Wurth A. Kaukher. 14th IEEE-NPSS Real Time Conference, 2005.

[KNOLL]. "Radiation Detection and Measurement." By Glenn F. Knoll. John Wiley & Sons, Inc, 2000.

[LArTPC]. *Liquid Argon Time Projection chambers.* http://www-lartpc.fnal.gov.

[LHC]. *LHC (Large Hadron Collider).* http://lhc.web.cern.ch/lhc/.

[LLOP02]. "Medipix2: a 64-k Pixel Readout Chip With 55-um Square Elements Working in Single Photon Counting Mode." By M. Campbell, R. Dinapoli, D. San Segundo, and E. Pernigotti X. Llopart, VOL. 49. TRANSATIONS ON NUCLEAR SCIENCE, 2002.

[LLOP07]. "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements." By R. Ballabriga, M. Campbell, L. Tlustos, W. Wong X. Llopart. Vienna Conference on Instrumentation, 2007.

[MOTA]. "Time-Domain Signal Processing Algorithms and their Implementation in the ALTRO chip for hte ALICE TPC." By Bernardo Miguel Lopes Leitao Mota. CERN-THESIS-2003-023, 2003.

[NA49]. "The NA49 Large Acceptance Hadron Detector." By NA49 Collaboration. CERN-EP/99–001, January 1999.

[OED]. "Position-sensitive detector with microstrip anode for electron multiplication with gases." By A. Oed, 351-359. NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, 1988.

[OPPEN]. "Discrete-Time Signal Processing." By Ronald W. Schafer Alan V. Oppenheim. Prentice hall, Second edition, 1999.

[PANDA]. "The PANDA GEM-based TPC prototype." By L. Fabbietti et al. NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, 2010.

[PELLEG]. "A high energy proton-electron-positron colliding beam system." By J. Rees, B. Richter, M. Schwartz, D. Mohl and A. Sessler C. Pellegrini. September, 1971.

[PHYTON]. *http://www.python.org/about/.*

[RCU]. "The ALICE TPC Readout Control Unit." By R. Campagnolo, A. Junique, L.Musa C. González Gutiérrez. Puerto Rico: Proceeding of the 2005 IEEE Nuclear Science Symposium and Medical Imaging Conference, 2005.

[ROSSEG]. "Simulation & Calibration of the ALICE TPC including innovative Space Charge Calculations." By Stefan Rossegger. CERN-THESIS-2009-124, 2009.

[S-ALTRO]. *S-ALTRO User Manual.* Geneva: CERN, 2010.

[SAULI]. "GEM: A new concept for electron amplification in gas detectors." By F. Sauli, 531-534. NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, 1996.

[SPIELER]. "Semiconductor Detector Systems." By H. Spieler. Great Britain: Oxford Science Publications, 2005.

[SPILLER]. "The FAIR accelerator project at GSI." By G. Franchetti P. Spiller, 306-309. Darmstadt, Germany: NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH, 2006.

[SYNOP]. *Synopsys web page.* http://www.synopsys.com.

[TK2]. *T2K (from Tokai To Kamioka).* http://jnusrv01.kek.jp/public/t2k/.