Preliminary Results of the Radiation Hardness Tests of the SVX IIE Silicon Readout IC

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Abstract

This note presents the results of the first radiation hardness test performed on the new SVX IIE. The SVX IIE was exposed at the Fermilab Irradiation Facility, with 8 GeV protons, up to a fluence of 4.9×10^{13} protons/cm^2 and its gain, linearity, pedestals and power consumption compared to those before irradiation. Everything indicates that the performance of the chip is very little affected by radiation. The gain and pedestals did not change, within errors, while the power consumption appeared to increase by 2%. The increase in power may very well be caused by environmental changes and not by radiation.

1. INTRODUCTION

The SVX II integrated circuit will be used for readout and digitization of the very small charge signals produced by the silicon detectors comprising the Silicon Tracker that is part of the DØ Upgrade. This chip has 128 input channels, each with a programmable analog pipeline delay of up to 4 μs, digitization to 8 bits of resolution, data sparsification (zero suppression) and many other features. The latest version of this chip, referred to as SVX IIE, is fabricated by United Technology Microelectronics Center with their 1.2 μm-drawn UTER radiation hard CMOS process, using 5" wafers and double level metallization. A detailed description of the chip can be found in Ref. [1].

The SVX II chips will be mounted (in bare die form) right next to the individual silicon detectors, located inside the tracking cavity of the DØ detector [2]. This means that the SVX II, as well as the silicon detectors, will be exposed to damaging radiation produced by the $p\bar{p}$ collisions. The two main effects of radiation in a semiconductor are ionization (creation of electron-hole pairs) and crystal lattice damage, referred to as "displacement damage" (displacement of the atoms in the lattice). Displacement damage causes the introduction of unwanted energy levels inside the forbidden gap of the semiconductor, modifying its electrical behavior. The most important consequences of this are the increase in junction leakage currents (introduction of carrier generation-recombination centers) and changes in the effective doping concentration of the different regions of the semiconductor (creation of acceptor- and/or donor-like levels). All of these,

in turn, cause degradation of transistor gains and operating points. The introduced defects can also modify carrier lifetimes, mobilities and diffusion lengths. Since many of this displacement defects are somewhat mobile inside the lattice (specially at high temperatures) they can be partially removed by annealing, thus recovering some of the damage. On the other hand, some defects will evolve over time in such a way as to make the damage worse; this has been called "reverse annealing" and is particularly severe in lightly doped (high resistivity) silicon. Displacement damage is also responsible for an increase in noise levels, which is, in some cases, the first symptom of the damage that becomes noticeable, specially in CMOS structures. In general, ionization of bulk silicon is a transitory disturbance which quickly disappears after the electrons and holes recombine, but it can have long term effects when some of the charge is trapped inside the SiO_2 layers used for insulation and passivation. Since the SiO_2 is an insulator, the charge generated in it cannot be easily removed and will remain trapped almost indefinitely. This kind of damage is specially detrimental to CMOS structures, since it modifies the field beneath the gate, causing changes in the threshold voltage and even dielectric breakdowns when the amount of trapped charge becomes too large. For more information on radiation damage in semiconductors see Refs. [3, 4, 5].

Since the charged particle flux inside the DØ tracking cavity decreases as $1/r^2$, the inner layers of the Silicon Tracker (silicon detectors and SVX II readout chips) will be the most heavily irradiated. According to Ref. [6], the inner layer (at 2.78 cm from the beam) is expected to receive a charged particle flux of 1.54×10^{10} cm^{-2}/pb^{-1} and a neutron flux of 1.8×10^{9} cm^{-2}/pb^{-1}. With the Tevatron running at 2000 pb^{-1}/year, the charged particle fluence will be 3.1×10^{13} cm^{-2}/year, wile the neutron fluence will be 3.6×10^{12} cm^{-2}/year. It becomes evident that radiation hardness is a very important and vital feature of the SVX IIE. The whole Silicon Tracker Upgrade project will be jeopardized by a failure of the SVX IIE to operate within specifications, when subjected to these levels of radiation.

In this note we present the first results of radiation hardness testing done on one of the irradiated SVX IIE, where the gain, linearity, pedestals and power consumption were measured before and after irradiation with 8 GeV protons at the Fermilab Irradiation Facility.

2. IRRADIATION PROCEDURES

This irradiation was performed at the Fermilab Irradiation Facility, located in one of the Booster's beam dump lines (identified as the AP-4 line). This line provided a pulsed beam of 8 GeV protons with intensities between 7×10^{8} and 1.5×10^{9} protons per pulse and pulse intervals from 2.9 s to 6 s, resulting in an average dose rate of 10^{8} protons/s. Dose monitoring was accomplished on-line by a toroid and off-line by the analysis of the activation of Al foils placed in front or behind the chips. The total dose delivered to the samples was $(4.91 \pm 0.70)\times10^{13}$ protons/cm^2.

The proton fluences quoted here are not normalized to 1 MeV neutron fluences, as is customary for radiation damage studies, because the spectra and contamination of the proton beam are not known. Assuming a pure and mono-

energetic 8 GeV proton beam, the equivalent 1 MeV neutron fluence $\Phi_n(1\text{ MeV})$ can be calculated as the proton fluence $\Phi_p(8\text{ GeV})$ times the ratio of the displacement kerma cross sections for both particles at those energies:

Disp. Kerma Cross Section for 8 GeV protons (from [7]): $D_p(8\text{ GeV}) \cong 8.0\times10^4\ \text{eV}\cdot\text{barn}$

Disp. Kerma Cross Section for 1 MeV neutrons (from [8]): $D_n(1\text{ MeV}) \cong 9.5\times10^4\ \text{eV}\cdot\text{barn}$

$$\Phi_{ne}(1\text{ MeV}) = \frac{D_p(8\text{ GeV})}{D_n(1\text{ MeV})}\times\Phi_p(8\text{ GeV}) \cong 0.84\times\Phi_p(8\text{ GeV}) \quad (1)$$

The SVX IIE's were located in a gas- and light-tight G-10 box, whose temperature was controlled to 5 °C ± 1°C. Dry nitrogen was circulated through the box to keep the humidity as low as possible and avoid condensation over the bare silicon dies (the humidity was not measured). This box was mounted on an X-Y motorized table that enabled us to sweep the samples across the beam.

Two SVX IIE chips (identified as #2 and #4) were irradiated at the same time, both chips were mounted on PCBs that allowed us to connect them to the Silicon Acquisition and Readout Test Station (SAR-TS for short) for testing (the PCBs also contain several capacitors and resistors needed to bias and operate the chip). Chip #4 was bonded to 128 channels of a full single sided ladder of silicon detectors (two single sided detectors of 6 cm × 2.1 cm). During irradiation, the chips were powered with AV_{DD}, DV_{DD} and QV_{DD} at +5 V and AV_{DD2} at +3 V. It has been found [3] that the effects of radiation on a powered device are very different from those on a non-powered one. The reason for this is that the electric fields present in a powered device help drain the ionization charge, decreasing its rate of accumulation in the Si/SiO_2 interfaces, and the currents flowing through the material accelerate the annealing of certain displacement defects. After irradiation, chip #2 was stored at room temperature for 56 days, while chip #4 was kept below 0°C to minimize annealing (either beneficial or reverse).

3. EXPERIMENTAL RESULTS

For all the following tests, the SVX and SAR-TS were configured as the following table shows (see Ref. [1] for a description of the parameters):

Parameter	DEC/HEX Value	BIN Value
PA BW	2	000010
Ramp Trim.	$250	01001010000
Chip Current	4	100
Pipeline Depth	3	00011
Cal. Voltage	4	100
Threshold	10	00010000
Counter Modulo	81	10000001
ADC Pedestal	4	0100
Clock Frequency	53.1 MHz	
AV_{DD2}	+3 V	
AV_{DD}, DV_{DD} , QV_{DD}	+5 V	

Table 1: SVX IIE parameter configuration during tests.

3.1. Power Consumption

Power consumption of the SVX II is a critical issue since power distribution and heat removal in the tightly packed tracking cavity are not easy tasks. Since the SVX is in thermal contact (through the HDI) with the silicon detectors, it should dissipate as little heat as possible because the detectors must be kept at a low temperature in order to minimize their leakage current (and the noise it causes) and slow down the reverse annealing of the radiation damage.

The AV_{DD}+DV_{DD} +QV_{DD} current of one of the detectors was recorded during the whole irradiation to see if there was a clear increase or decrease as the dose accumulated. Unfortunately, because all the digital inputs of the chip were left unconnected, the gates of the CMOS transistors floated to a voltage very close to the threshold, making the transistors conduct and draw a large current. For the same reason, the current changed constantly because of noise pickup at the floating inputs. Worst of all, each time the chip was hit by the proton beam the current increased instantly to about 80 mA because of the very large ionization produced by the protons in the bulk silicon; after the beam pulse, the current decreased slowly to about 30 mA. In consequence, the recorded current varies almost at random between 30 and 80 mA and is not meaningful. Nevertheless, according to past experience with irradiated electronic devices, we expected the current draw to increase (as leakage currents increase due to displacement damage) at least in the short term, recovering with time thanks to beneficial annealing [4].

Table 2 shows the currents and power drawn by chip #2 from each supply before and after irradiation, measured after initialization followed by one cycle of acquisition and readout. It is clear that power consumption is very little affected by radiation up to the applied dose, increasing by just 2%. It is even possible that the 2% increase is not really caused by radiation but by environmental changes or differences in the setup.

Supply	Current Before Irrad. [mA]	Power Before Irrad. [mW]	Current After Irrad. [mA]	Power After Irrad. [mW]
AV_{DD}	48.60	243.0	48.80	244.0
AV_{DD2}	25.03	75.1	26.04	78.1
$DV_{DD} + QV_{DD}$	14.54	72.7	15.50	77.5
TOTAL:	-	*390.8*	-	*399.6*

Table 2: Current and power consumption of chip #2 before and after irradiation. Currents were measured after initialization followed by one cycle of acquisition and readout.

3.2. Gain, Linearity and Pedestals

Linearity tests were performed by injecting, for each point in the curve, 20 identical charge pulses into a single channel of the SVX and taking the average and standard deviation (σ) of the resulting digitized output. The amount of injected charge was controlled by changing the height of the pulses. The output was fitted to a straight line by a least squares method, resulting in the following transfer functions:

$$\text{Before irradiation: } SVX\ Out = (2.633 \pm 0.016)\cdot Q + (13.26 \pm 0.92), \qquad \text{(eBe)}$$

$$\text{After irradiation: } SVX\ Out = (2.626 \pm 0.007)\cdot Q + (13.55 \pm 0.39), \qquad \text{(eCe)}$$

where Q is the injected charge in fC. Table 3 shows the digital output of the SVX #2 for 16 points along its range, from 0 to 91 fC, the standard deviation (σ), the values of the fit and a measure of the deviation from linearity (difference between the fitted straight line and the actual output). Figure 1 shows the measured points and the straight line fit for chip #2 after irradiation, while Figure 2 presents the deviation from linearity as a function of the injected charge for chip #2, both before and after irradiation. It is clear the linearity after irradiation is excellent and it changes very little from that before irradiation; in fact, within uncertainties, the slope (gain) and pedestal did not change. This means the gains and operating points (threshold voltages and quiescent currents) of the CMOS transistors were very little affected by the applied radiation dose.

As can be seen in the table, the noise (σ) apparently went down after irradiation but at this point we are sure that noise is dominated by the setup. Non-irradiated chips tested at the same time as the irradiated one, exhibit the same behavior with respect to the noise. More detailed and precise measurements of the noise levels, before and after irradiation, will be performed in the near future.

Charge [fC]	BEFORE IRRADIATION				AFTER IRRADIATION			
	SVX Out [ADC Cts]	σ [ADC Cts]	Fit [ADC Cts]	(Fit-Out)/Fit	SVX Out [ADC Cts]	σ [ADC Cts]	Fit [ADC Cts]	(Fit-Out)/Fit
0.00	14.85	2.16	13.26	-11.99%	14.60	0.68	13.55	-7.77%
6.07	29.70	1.63	29.25	-1.55%	29.30	0.86	29.49	0.64%
12.14	44.95	2.28	45.23	0.62%	45.25	1.02	45.43	0.40%
18.21	61.05	1.82	61.22	0.27%	61.45	0.89	61.37	-0.12%
24.28	76.70	1.75	77.20	0.65%	77.40	0.99	77.32	-0.11%
30.35	92.40	2.52	93.19	0.84%	92.85	0.88	93.26	0.44%
36.42	108.30	2.79	109.17	0.80%	108.20	0.70	109.20	0.91%
42.49	123.80	2.09	125.16	1.08%	124.30	0.92	125.14	0.67%
48.56	141.10	2.81	141.14	0.03%	140.55	1.15	141.08	0.38%
54.63	156.35	2.32	157.13	0.49%	157.10	1.17	157.02	-0.05%
60.70	174.20	1.82	173.11	-0.63%	173.20	0.77	172.97	-0.13%
66.77	188.25	2.27	189.10	0.45%	189.00	0.97	188.91	-0.05%
72.84	205.35	2.30	205.08	-0.13%	205.10	0.91	204.85	-0.12%
78.91	221.05	2.19	221.07	0.01%	220.80	1.01	220.79	0.00%
84.98	237.60	2.52	237.05	-0.23%	237.15	0.81	236.73	-0.18%
91.05	253.25	1.16	253.04	-0.08%	252.95	0.76	252.68	-0.11%

Table 3: Transfer function measurements on chip #2.

4. CONCLUSIONS

It has been shown that the radiation hard version of the SVX II readout IC (SVX IIE) was very little affected by irradiation with 8 GeV protons up to a fluence of $(4.91 \pm 0.70)\times10^{13}$ protons/cm^2. Gain, linearity and pedestals remained unchanged, within uncertainties, while the power consumption increased by 2%. This increase in power can have other reasons besides radiation damage, and is negligible considering that current draw changes significantly depending on the operations being performed by the SVX II at the time of measurement.

It is expected that one of the first symptoms of radiation damage on the SVX II is an increase in the noise levels but, unfortunately, they cannot be accurately measured with the current setup. At this point the noise seems to be dominated by external sources, masking any increase caused by radiation (which will surely be small). More accurate noise measurements will be made in the near future.

After this preliminary tests, the SVX IIE appears to meet the radiation hardness specifications needed for a successful operation in the DØ Silicon Tracker. More detailed tests remain to be made but, given the results here presented, any degradation in performance is surely small.

5. REFERENCES

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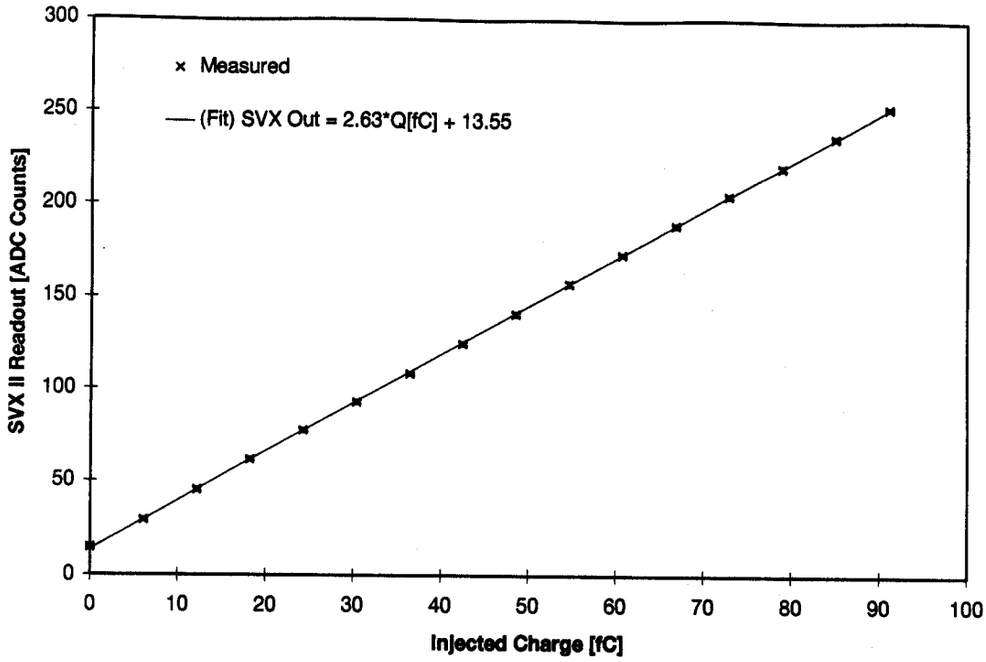

Figure 1: Transfer function measurements and a straight line fit for SVX IIE chip #2 after irradiation.

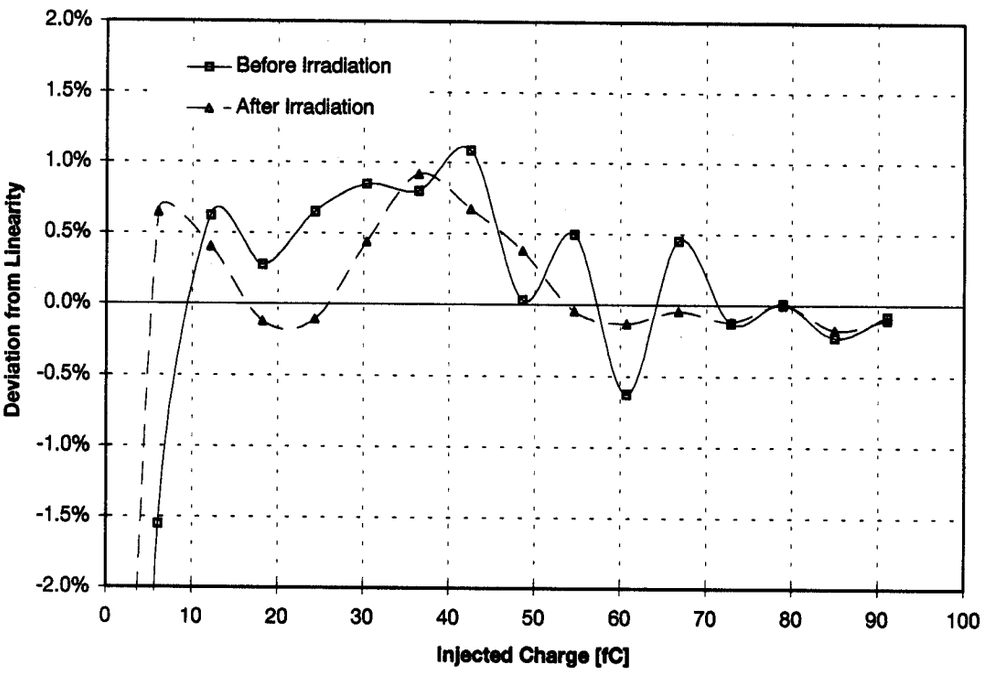

Figure 2: Deviation from linearity of SVX IIE chip #2, before and after irradiation. The smoothed lines connecting the points were added for legibility.