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SIMPLE, VERSATILE CAMAC CRATE CONTROLLER AND INTERRUPT PRIORITY ENCODING MODULE*

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Summary

A simple, versatile crate controller has been in use in CAMAC installations at SLAC for several years. Its design is based upon the criteria of minimum circuitry to connect seven CAMAC crates together on a "SLAC branch".

A priority encoding module to rapidly identify interrupt sources has been designed to work in conjunction with this crate controller for high rate interrupt environments. The concept is applicable to the standard branch as well.

Introduction

Prior to the availability of the Type A Crate Controller, a simple crate controller was designed at SLAC to be used in scanning-type scaler systems.[1] Although not as powerful as the Type A Controller, this crate controller has proven versatile enough to be used in all of the CAMAC systems now existing at SLAC that employ a "branch" concept. One limitation of this crate controller was that it had no capability to rapidly identify a module interrupt source (L).

Recently, however, the SLAC crate controller has been modified to provide independent outputs of the module L signals on the rear panel, as in the Type A Controller. This provides the capability of more sophisticated identification of the interrupt source. In particular, for a high rate, high volume interrupt system an interrupt priority encoding module is being built which encodes module interrupts into an 8-bit physical location code (3 bits for crate, 5 bits for module number) on a straightforward priority scheme, with crate number having the higher priority. The module also contains a 23-bit LAM mask register which permits rapid parallel control of interrupt activity. No patching or bit assignment is necessary and there is no limit on the number of modules with interrupt capability in the system.

In order to implement this interrupt system a separate link between the crates is necessary in addition to the usual branch connection.

Although this priority encoding module is designed specifically for the SLAC crate controller, the concepts are applicable to the standard branch as well, where the Graded-L cycle is used to identify interrupts.

Description of the SLAC Crate Controller

A block diagram of the crate controller is shown in Figure 1. It contains the minimum circuitry to connect 7 crates together on a branch; in other words, the crate controller is "transparent" to the Dataway signals. One of the primary benefits of this approach is that interfacing at the branch level is simplified, and knowledge of only the basic specification TID-25875 is required.

Many of the philosophies of the standard branch were retained, such as negative true TTL logic, the use of open collector drivers, the use of high impedance receivers, and the sharing of the 24 read-write lines on the branch. Significant differences include binary coding of the crate number, use of individual signal wires instead of twisted pairs on the branch, and coding of the first module position as N(0) instead of N(1).

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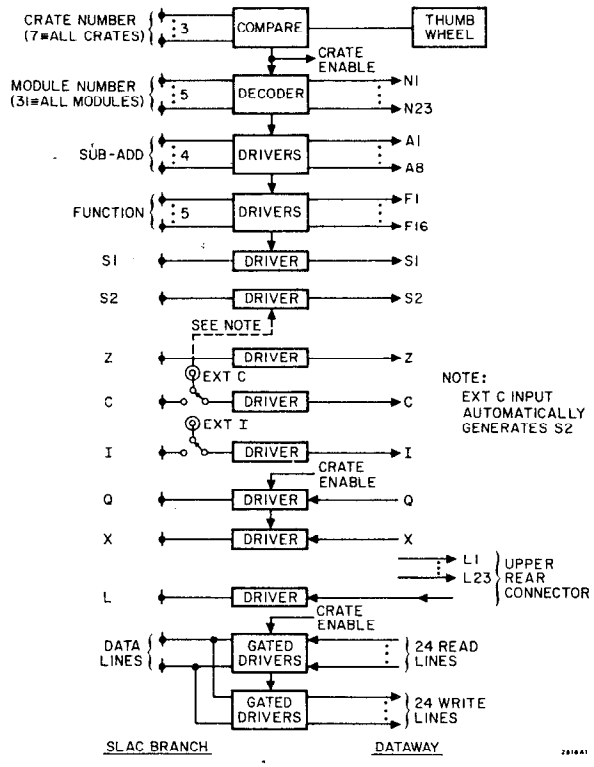

FIG. 1--Block diagram of SLAC crate controller.

Figure 1 indicates that the basic components of the crate controller are line drivers, the crate number comparison logic, and the N line decoder. Note that in general all Dataway signals are directly repeated on the branch, including S1 and S2. The timing of S1 and S2 is generated in the branch driver or interface based on speed requirements, cable lengths, etc. In fact, in one application this crate controller has been used over a 1000-foot twisted pair cable with a complete cycle of about 10 μsec.

Signals Z, C, and I appear on the branch and are common to all modules in the system. Separate inputs for clear (C) and gate (I) are provided on the front of the crate controller, which are switch-selected for independent clearing or gating if desired.

A special feature of the crate controller is that CR(7) addresses all crates, and N(31) addresses all modules in a crate.

Modifications to the unit since its inception are (1) addition of the X line; (2) routing of the 23 L lines to a rear connector for use in a separate LAM handling unit (an input to the branch L is provided on this same connector); (3) change of the branch connector due to reliability and availability problems.

A complete circuit diagram is shown in Figure 2. The unit contains 41 IC's on two boards. All signals are received from the branch in SP380A high impedance, high threshold receivers. All branch outputs are driven by MC858 or equivalent drivers capable of sinking at least 50 mA. Pullups at one end, usually in the branch driver or

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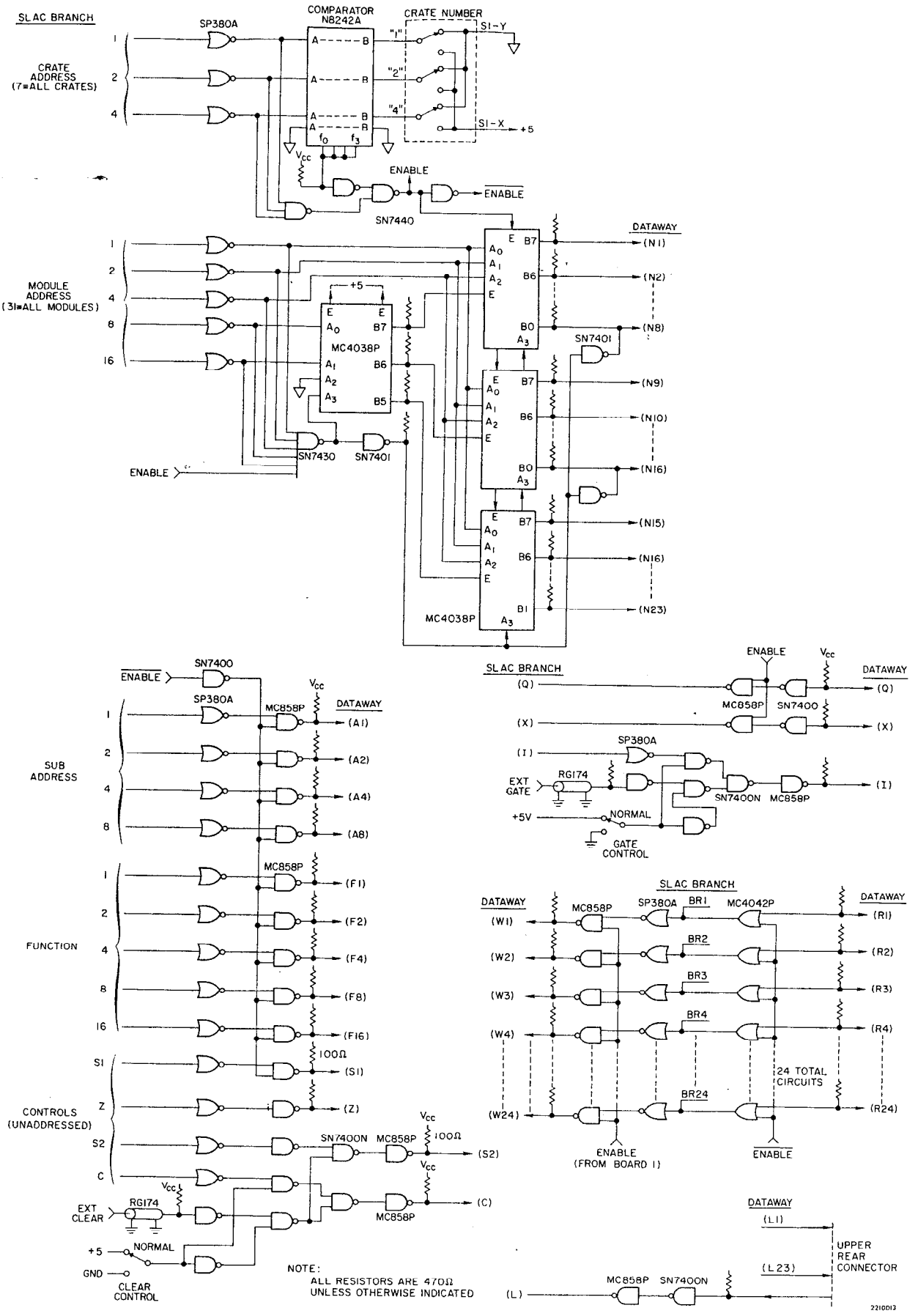

FIG. 2--Crate controller schematic.

interface, are required. In the special case of the 1000-foot branch mentioned previously, the cable was terminated at both ends.

Priority Encoding Module - General Concepts

Once the individual L outputs are available, interrupt handling can be treated in many ways depending upon the specific application and computer, but for high speed identification with a large number of interrupt sources a priority encoding scheme appears attractive both from the hardware (versatile, unlimited size, no patching) and the software standpoint (locations can vector to interrupt routines). A LAM handler based on this priority encoding concept has been designed. In order to establish crate priority and provide a direct, high speed path for encoded interrupts a separate connection between the priority encoding modules is used. In this way the computer can identify module interrupt locations directly without a CAMAC operation if an appropriate computer input register is available. As described later, this register is not a necessity, and encoded locations can be read via CAMAC operations if desired.

A diagram of system interconnection is shown in Figure 3. This figure shows both the normal connection between the

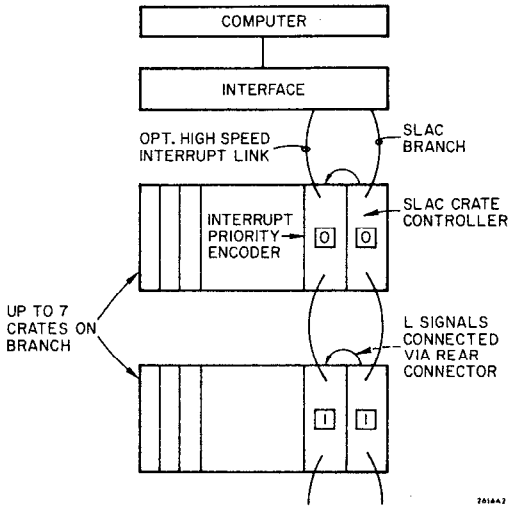

FIG. 3--System interconnection.

crate controllers and the additional link between the priority encoding modules. The interrupt link is obviously an additional burden, but does not limit crate distances any more than the existing limitations of the parallel SLAC branch. The link consists of 8 bits of coded information, a priority chain signal, and an interrupt response line from the computer. For programming convenience the priority encoding module is expected to be in the same station in each crate, but this is not a necessity.

Before going into any further description of the unit it is necessary to point out one important consideration in structuring a priority encoding system in which inputs can occur randomly and asynchronously as in the case of CAMAC L signals. In such a case, system inputs occurring during the reading of encoded information cause immediate readjustment of the data and may result in an invalid code as a transient condition. Although this effect may in some cases be negligible, or can be handled by software fixes, the goal in this design was to eliminate the possibility of false codes by staticizing (latching) all of the inputs to the priority encoding network during reading of the interrupt location. A considerable effort in the design went into the analysis and solution of the transient problem.

Priority Encoding Module - Description

A simplified block diagram of the unit is shown in Figure 4. The L signals from the Dataway are routed to the

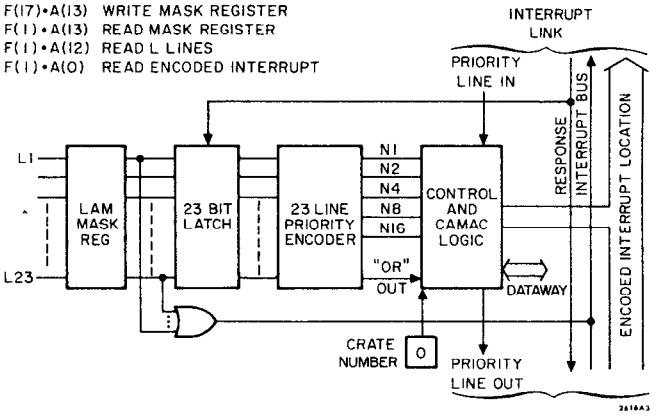

FIG. 4--Block diagram of interrupt priority encoder.

module via 26-conductor flat cable at the rear of the crate controller. Prior to masking or encoding, the state of all L signals can be read using F(1)·A(12). Each L signal is AND'ed with the appropriate bit of a mask register, which is parallel-loaded using F(17)·A(13). The 23 gate outputs are OR'ed and return to the SLAC branch via the crate controller, where the crate L's are OR'ed onto the single branch interrupt line, L. This single L signal then indicates whether any module requires service. Note that the parallel access to the mask register permits very rapid, convenient handling of interrupt activity. For example, the program can dynamically set interrupt priorities by disabling all modules of a lower priority while servicing an interrupt. Thus there is a potential of 23 levels that can be reassigned in a single CAMAC operation using CR(7)·N(i)·F(17)·A(13).

After activation of the branch L, identification of the interrupt source follows. The computer generates a response signal which latches the current states of all the gated L lines into a 23-bit register in each priority encoding module. One or more bits may be set. The priority encoding network in each crate, which is based on the use of Fairchild 9318 chips, encodes the highest priority bit set into a 5-bit module address. An overall OR in the priority network of each crate drives a crate priority bus daisy-chained between crates. The crate with the highest priority (closest to the computer) gates its module address onto the interrupt link along with a 3-bit code for the crate number. The speed of this activity is limited only by propagation delays of gates and cables. Following identification of the module the program identifies the particular L request within the module using conventional means.

Somewhere during the interrupt service routine the module LAM status flip-flop will be reset. This will reset the L signal in the SLAC branch, unless other interrupts are pending. If the L line indicates that an L request still exists in the system, then the response line is triggered again, the latches are loaded, and a new priority interrupt code is generated. In this manner the computer reads, and services, the highest priority interrupt that is currently active. As discussed previously, the actual priorities can be modified by reloading the mask register within the interrupt service routine.

In those cases where a separate input register is not available on the computer the priority encoded location can be read in a normal CAMAC operation using N(i)·F(1)·A(0) addressed to any crate in the system. This is possible since the interrupt link carrying the priority encoded information

connects all of the priority modules in the system. A further feature is that the priority encoded information in a particular crate can be read using N(i)· F(1)· A(1).

It is significant to point out that if the encoded information on the interrupt link is not read directly in a separate computer register, then in reality it is not necessary to transmit the 8-bit code along the interrupt link. Performing a read CR(7)·N(i)·F(1)·A(0) addressed to all crates will read the highest priority module L in the system. It is, however, necessary to connect the response line and the crate priority line between the priority encoding modules. At the present time a separate cable is required for this connection since extra wires in the SLAC branch were not available.

Conclusion

This paper describes a simple, versatile crate controller which has been in use at SLAC for several years in many different CAMAC systems. A recent modification makes possible an accompanying priority encoding module which provides rapid identification of an interrupting module in a branch. For the highest speed the encoded information is sent along a separate interrupt link, but it is also possible to read the same information using a CAMAC operation.

It is hoped that this development will inspire similar thoughts on LAM handling in the standard branch.

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