TWO 2-STAGE TRANSIMPEDANCE AMPLIFIERS FOR SILICON DRIFT DETECTORS READOUT

G. Mazza, INFN, Torino, Italy (email: mazza@to.infn.it)
A. Rivetti, Politecnico and INFN, Torino, Italy (email: rivetti@polgen1.polito.it)

Abstract

Two 2-stage transimpedance amplifiers have been developed which match the requirements of the front-end of the Silicon Drift Detectors (SDD) in the ALICE experiment. In this paper the architecture of the circuits is described and lab measurements are presented.

1. DESIGN SPECIFICATIONS

The requirements of the front-end electronics for the ALICE SDD are discussed in detail in [1] and [2] and can be summarised as following:

- Maximum input signal (charge): 10 mip
- Maximum input signal (current): 1.6μA
- Equivalent input noise charge (E.N.C.) < 500 e-
- Input current noise < 2nA r.m.s.
- Power consumption: < 1mW
- Input capacitance (detector capacitance + bonding wires and stray capacitances) < 2pF.
- Capability to work with power supplies down to 3.3 V

In addition, a fast peaking time (< 30ns) is a useful feature that can improve significantly the separation of close tracks.

The presented circuits have been designed to meet all of the previous constraints.

2. DESIGN ARCHITECTURE

When fast peaking times are desired, a transimpedance amplifier is a suitable configuration [3], [4].

Moreover, to decrease the power supplies to 3.3 V, we limited the maximum output signal to 1.5V. If this is the case, the transimpedance gain required can be calculated as:

$$\frac{V_{out(max)}}{I_{in(max)}} = \frac{1.5V}{1.6\mu A} = 940k\Omega$$

For the lowest signals of interest, which are in the nA range, this gain will give an output of few millivolts, thus requiring a waveform digitizer of high sensitivity (at least 10 bits on a scale of 1.5 V)

A possible alternative is to use a non linear amplifier. In CMOS technology a non linear transimpedance amplifier can be easily implemented using a MOS transistor as the feedback element [5]. We found the design proposed in [5] extremely interesting for our application because:

- The non linear transfer function relies on the behavior of a single MOS transistor, which is physically well understood and mathematically well modeled.
- With a proper design of the feedback element, the equivalent transimpedance can be quite high (hundreds of kΩ or more). The contribution of this resistor to the system noise is then very low.
- A second order transfer function is achieved in a single stage, saving area and power.
- The pulse shape can be optimised acting on a bias voltage, which makes the system very robust against variation of the input capacitance.

Our implementation of this scheme is reported in fig. 1.

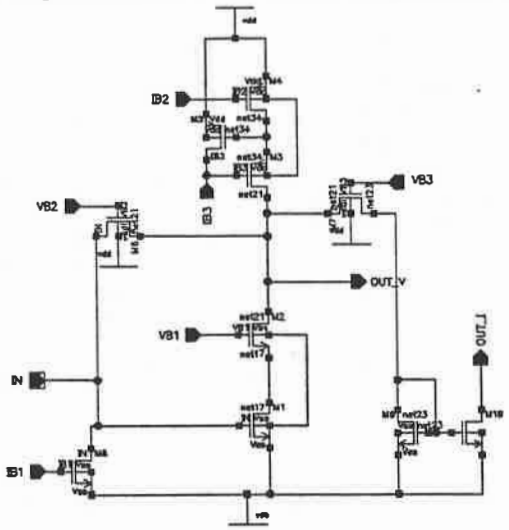


Fig. 1 Schematic of the transimpedance amplifier

Compared to previously reported designs which employ the same feedback topology, [5] [6], the main amplifier is loaded with a regulated cascode [7]. In this way, the output impedance of the main amplifier is improved and the bias voltage is more efficiently used.

For a peaking time of 25ns, the feedback branch could be optimised to give a small signal gain of 350.000 kΩ. This gain was not sufficient for our purposes, so a two stage configuration had to be used.

If we look at fig.1, we can notice that this configuration can provide two outputs: a voltage output at node OUT_V, which is proportional to the square root of the input current and a current output at the node OUT_I, which is proportional to the input current [5]. The second stage can be either a linear voltage amplifier connected to node OUT_V or a transimpedance amplifier connected to node OUT_I.

In the former case a square root signal compression is achieved in the input stage. In the latter, the square root compression can be achieved in the second stage if this has the same circuit topology of the input one.

3. DESIGN IMPLEMENTATION

Both solutions described above were implemented on silicon in a standard 0.8µm CMOS process, in a single chip containing eight channels of each type. Fig. 2 depicts the configuration which uses a voltage amplifier as the second stage. In the technology used, high value linear resistors were not available, so, to minimise power consumption, a differential pair with local feedback was the preferred solution. In this way, also a differential output is provided.

Design guidelines for this kind of amplifiers can be found, for instance, in [8].

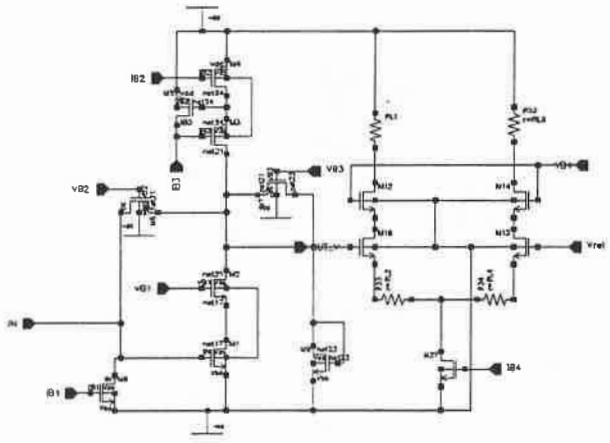


Fig2. Transimpedance amplifier with voltage gain stage

Fig. 3 depicts the alternative solution, in which the input stage works as a current amplifier. Compared to the previous one, this solution has the advantage that no passive component is required. If we look at fig.2, we see that there is the need to provide a reference voltage to the differential amplifier. On the other hand, in the circuit represented in fig. 3 the dc current flowing from the first into the second stage is to high and needs to be compensated. Both problems were addressed with the use of dummy structures. In this way, there is no ac coupling in the signal path. The amplifier is completely dc coupled to the detector and the detector leakage current can be measured.

The total small signal gain is adjusted to 2MΩ in both circuits for a peaking time of the pulse response of 25ns. The layout area is 100µm x 270µm for the circuit of fig. 2 and 100µm x 220µm for the circuit of fig. 3.

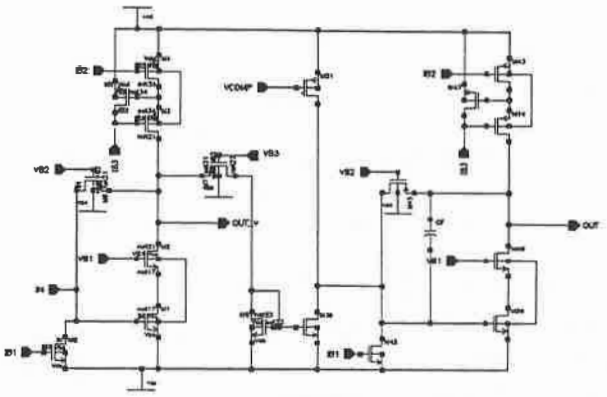


Fig. 3 Current amplifier with transimpedance gain stage

4. LAB MEASUREMENTS

The two circuits were first tested at the bench with a dedicated set-up and then connected to a silicon drift detector used in a test beam at the CERN SPS. The analysis of the beam test data is still very preliminary. We concentrate here on the tests at the bench. The main results are summarised in table 1 for the circuit of fig. 2 and table 2 for the circuit of fig.3, respectively.

Tab. 1 Measured parameters for circuit of fig. 2

Small signal gain	2MΩ (single ended) 4MΩ (differential)
Current input noise	< 2 nA r.m.s
Output voltage swing for 1.6uA input	0.75V(single ended) 1.50V(differential)
Power consumption	680 µW
Power supplies (Vdd - Vss)	3.3V

Tab. 2 Measured parameters for circuit of fig.3

Small signal gain	2MΩ
Current input noise	< 2 nA r.m.s
Output voltage swing for 1.6uA input	1V (Only single ended output available in this scheme)
Power consumption	800 µW
Power supplies (Vdd - Vss)	3.3V

The cross talk between channels was below 2% for both circuits.

The small signal gain variation was around 2% for channels on the same chip and 4% for channel on different chips for both circuits as well.

The chip were also tested in a large signal condition, with input signals up to 2μA, in order to study the non-linear behavior. As we have seen in sec. 2, in fact, this property could be used to compress the signal at the amplifier level, thus decreasing the resolution required for the waveform digitizer (i.e. analog memory + ADC) from 10 to 8 bits [1].

As an example, in fig. 4 we report the fits on the data measured on two channels which use the voltage amplifier as the second stage (see fig. 2).

The output voltage was chosen as the independent variable and the data were fitted by a simple parabolic law: $y = p1 \cdot x^2 + p2 \cdot x + p3$

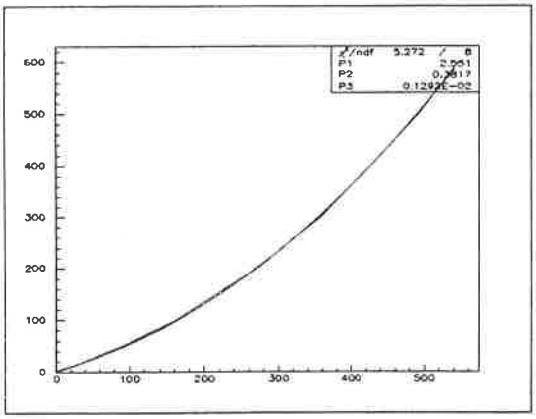
It can be seen that a parabolic fit is very good for input currents up to 700nA. In case of the Silicon Drift Detectors in ALICE, this value corresponds to an input charge of about 5 mip. The fact that the data follow a quadratic law is in good agreement with the fact that the nonlinear element is a MOS transistor working in the saturation region.

In fig. 5 is reported the behavior of the two channels for input currents up to 1.6μA, which correspond to a a charge of about 10 mip

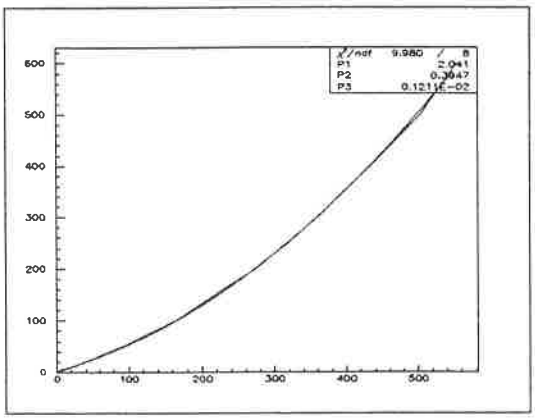
We notice that here the curves can be better approximated by a polynomial fit of the third order. This indicates that for higher levels of current the non linearities in the stages following the input transimpedance amplifier become important.

This effect is basically due to the differential voltage amplifier and results in a stronger compression for the largest input signals.

A more robust voltage amplifier with improved linearity for large signals is now under development. If the second stage is linear also for large swings, in fact, a very simple quadratic function can be used for the whole dynamic range. The homogeneity of the compression curve between different channels is improved as well.

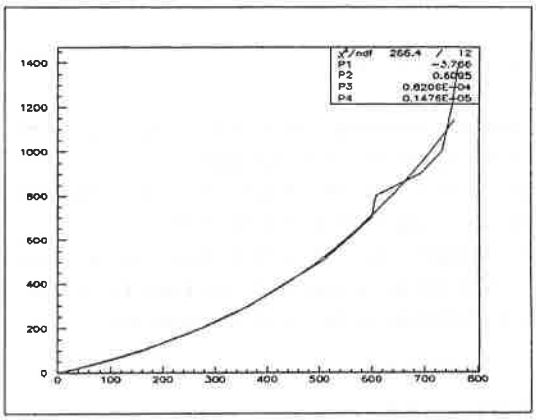


x-axis: mV y-axis: nA

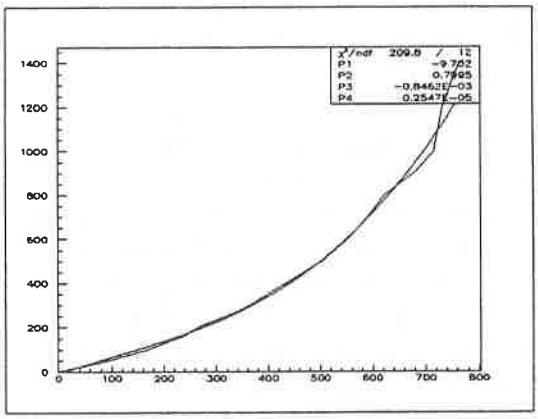


x-axis: mV y-axis: nA

Fig. 4 Fit of the non linear input-output relationship of t



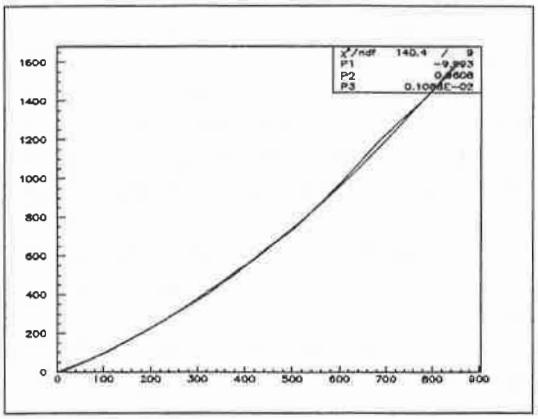
x-axis: mV y-axis: nA



x-axis: mV y-axis: nA

Fig. 5 Fit of the non linear input-output relationship of two different channels of the circuit of fig. 2. Compared to fig. 4 the input signal is extended to 1.6μA (10 mip)

In fig. 6 is reported the input-output curve for the circuit of fig. 3. Here the parabolic fit is a good approximation for the whole dynamic range.



x-axis: mV y-axis: nA

Fig. 6 Fit of the non linear input-output relationship of the circuit of fig. 3.

5. CONCLUSIONS

Two nonlinear transimpedance amplifiers have been designed in a 0.8μm CMOS technology.

The basic features of the circuits are a fast peaking time, a low noise and a low power consumption.

The lab measurements show that these circuits can meet the specifications required for the front-end of the Silicon Drift Detectors in the ALICE experiment.

6. REFERENCES

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