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From hybrid to CMOS pixels ... a possibility for LHC's pixel future?

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ABSTRACT: Hybrid pixel detectors have been invented for the LHC to make tracking and vertexing possible at all in LHC's radiation intense environment. The LHC pixel detectors have meanwhile very successfully fulfilled their promises and R&D for the planned HL-LHC upgrade is in full swing, targeting even higher ionising doses and non-ionising fluences. In terms of rate and radiation tolerance hybrid pixels are unrivaled. But they have disadvantages as well, most notably material thickness, production complexity, and cost. Meanwhile also active pixel sensors (DEPFET, MAPS) have become real pixel detectors but they would by far not stand the rates and radiation faced from HL-LHC. New MAPS developments, so-called DMAPS (depleted MAPS) which are full CMOS-pixel structures with charge collection in a depleted region have come in the R&D focus for pixels at high rate/radiation levels. This goal can perhaps be realised exploiting HV technologies, high ohmic substrates and/or SOI based technologies. The paper covers the main ideas and some encouraging results from prototyping R&D, not hiding the difficulties.

KEYWORDS: Solid state detectors; Particle tracking detectors (Solid-state detectors); Particle tracking detectors; Radiation-hard detectors

Contents

1 Introduction

Pixel detectors as large scale tracking devices have first been developed, built and have been used for the LHC detectors. They have had a very large impact on the physics performance of the LHC experiments, in the proton-proton collision experiments ATLAS [1] and CMS [2] operating at very high rates and in a very harsh radiation environment, as well as in ALICE [3], optimised for heavy ion collisions. They provide precise tracking and vertexing thus enabling the identification of long-lived heavy particles such as τ-leptons and mesons containing heavy quarks (τ-, b-, and c-tagging). The conceptual architecture of the LHC pixel detectors is that of so-called hybrid pixels [4], in which the pixellated sensor-diode and the R/O-chip are separate entities.

While hybrid pixels are so far the only viable concept to cope with the rate and radiation environment in LHC pp-experiments, other concepts combining some R/O elements or even full R/O circuitry within the sensing element (pixel diode) have been developed and brought to a state of maturity. Examples are DEPFET pixels [5] chosen for the pixel detector of the Belle II experiment, to be installed in 2017, and MAPS (Monolithic Active Pixel Sensors [6, 7]) used and operated since 2014 in the STAR experiment at RHIC [8]. MAPS pixels are also planned for the ALICE Inner Tracker upgrade [9]. Table 1 compares particle rates and radiation levels at different collider accelerators. It is evident that the demands in terms of particle rate and radiation are highest for LHC and HL-LHC, larger by several orders of magnitude than at other colliders. So far only hybrid pixel detectors can cope with these levels. At other colliders, however, the rate and radiation levels are much reduced such that the mentioned alternative pixel detectors are attractive, offering better spatial resolution and less material.

Table 1. Comparison of rate and radiation conditions at some particle colliders. The assumed lifetimes are 7 years, 10 years, 5 years for LHC/HL-LHC, ILC, and others, respectively. The rates and radiation levels are quoted at respective locations of pixel detectors positioned closest to the interaction point.

	Luminosity $cm^2 s^{-1}$	BX time ns	particle rate kHz/mm^2	NIEL fluence n_{eq}/cm^2/lifetime	ion. dose Mrad/lifetime
LHC	10^{34}	25	1000	2×10^{15}	79
HL-LHC	10^{35}	25	10 000	2×10^{15}	>500
LHC Heavy Ions	6×10^{27}	20 000	10	$> 10^{13}$	0.7
RHIC	8×10^{27}	110	3.8	few 10^{12}	0.2
SuperKEKB	10^{35}	2	400	$\sim 3 \times 10^{12}$	10
ILC	10^{34}	250	350	10^{12}	0.4

In this contribution, the most recent advances in hybrid pixel development are described in the next section. Then, in the third section, new monolithic pixel technologies aiming to cope with LHC-like radiation and rate levels are addressed, for which R&D has started only a few years ago.

2 Hybrid pixel detectors at LHC pp-expertiments

2.1 The signal and the noise

Figure 1 shows the typical situation faced by pixel detectors operation at LHC in pp-collisions. In a typical $250\,\mu$m thick silicon sensor close to $20000\,e/h$ pairs are produced by a minimum ionising particle. The discriminator threshold is typically set to $3500\,e^-$. The signal is broadened
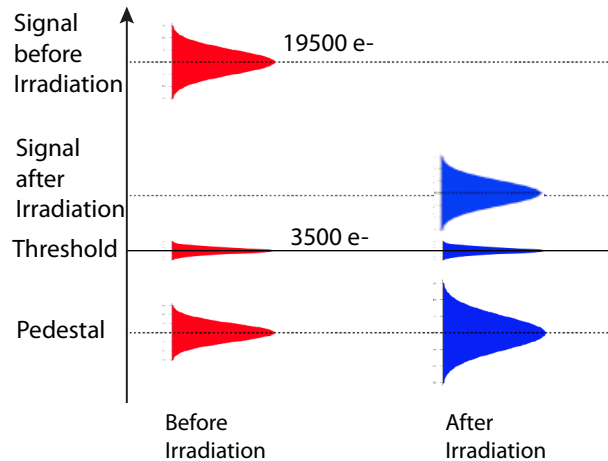

Figure 1. Signal and noise situation for a typical pixel detector.

(dominantly) by the electronics noise, the size of which can be measured by the width of the pedestal distribution. The probability of a fake hit, however, created when a noise hit crosses a channel's threshold, is governed by both the noise and the threshold spread (added in quadrature).

After irradiation (up to 2×10^{15} n_{eq}/cm^2) the S/N and signal-over-threshold situation become much tighter, because the signal is smaller due to bulk damage and the noise is larger due to increased leakage current. Fake hits thus become much more likely. In addition the chip electronics circuitry may fail due to ionising radiation, which is in the order of 80 Mrad at the projected end-life of the LHC, causing transistor threshold shifts. Note that these conditions become more severe by a factor of roughly 10 at the planned LHC upgrade HL-LHC (see table 1).

2.2 IBL — the first pixel upgrade in ATLAS

The so-called Insertable-B-Layer (IBL) is the first upgraded pixel detector added in 2014 as an additional innermost pixel layer in the ATLAS pixel system, now consisting of four layers (see figure 2). Compared to the existing 3-layer system of ATLAS, a large development step in terms
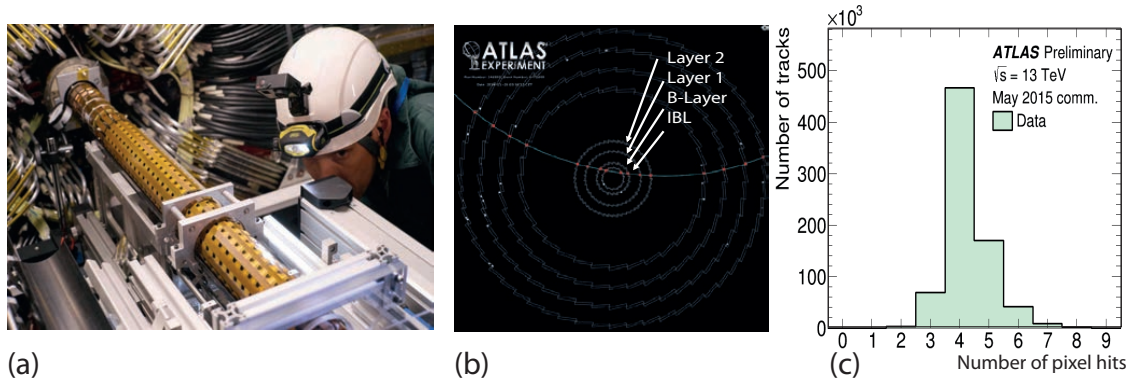
Figure 2. Insertable B-Layer of ATLAS, a first pixel detector upgrade. (a) IBL insertion into ATLAS, (b) cosmic ray event and (c) hit distribution in 13 TeV data, both demonstrating the capability of this new four-hit pixel system.

of sensors and electronics has been undertaken in the context of the design and building of the IBL. Facing a severe hit efficiency degradation with the existing readout chip (FE-I3 chip [10]) already at LHC luminosities three times as high as the nominal one, IBL uses a new R/O-chip (FE-I4 [11] in 130 nm technology), in which hits are stored locally in the pixels until triggered for readout, thus yielding a much higher efficiency. Additional SEU hardening measures have also been implemented. The pixel size is reduced to 50×250 μm^2. The FE-I4 chips can tolerate rates without too many hit losses up to several times the LHC design luminosity (10^{34} cm^{-2}s^{-1}), but it would yet be insufficient at rates as high as expected at the HL-LHC. IBL features two-chip pixel modules in size (~2×4 cm^2) almost as large as the 16-chip ATLAS pixel module using the FE-I3. In addition to the R/O chip, IBL has 75% planar silicon sensors with slimmed edges [13] and 25% 3D-Si sensors [14, 15], located at the end of the IBL-staves, which are operating for the first time in a large pixel detector.

The demands of HL-LHC in terms of rate and radiation are currently addressed by the R&D-Collaboration RD53 aiming for a pixel R/O chip in 65 nm CMOS technology [16]. This chip can be used in hybrid pixel concepts and will be capable of digesting a hit rate of 1 GHz/cm^2 and tolerate the ionising doses and fluences shown in table 1.

2.3 Advantages and limitations of hybrid pixels

Due to its split functionality (sensor and chip) the hybrid pixel technology has many advantages, especially in LHC-type environments, due to the fact that both parts can be tailored to the demands, i.e. the sensor especially to optimally stand irradiation and the readout chip to digest and process high rates ($\sim$ MHz/mm^2). Complex signal processing, even already in the pixel cell, is possible, including for example, zero suppression and temporary storage of hits during the trigger L1 latency. Hybrid pixels are proven radiation hard to 10^{15} n$_{eq}$/cm^2 and beyond. Spatial resolutions of the order of 10 μm have been achieved.

However, the hybrid choice also has some severe disadvantages. They constitute a relatively large material budget, typically more than 3% X$_0$ per layer in ATLAS and CMS. This is caused by the different components, sensor, R/O-chip, flex kapton, passive components, as well as support and cooling structures to operate at temperatures of (-10° C), as well as services. The module production including bump-bonding and flip-chipping is complex and laborious, leading to a large number of production steps. Consequently, hybrid pixel detectors are comparatively expensive.

Therefore, alternative pixel technologies have come into focus that aim to address the disadvantages mentioned above, while keeping the advantages to a large extent. This development runs under the label *Depleted CMOS Pixels* or DMAPS (Depleted Monolithic Active Pixel Sensors).

3 DMAPS — monolithic CMOS pixels for the HL-LHC upgrade

3.1 The goal

The goal of this new development is to employ commercial CMOS technology with some modifications to obtain sufficient signal and fast timing in monolithic CMOS designs, that merge sensor and R/O chip into one entity, while maintaining charge collection via charges drifting in an electric field inside the chip's substrate. In addition, the technology must survive the radiation environment at the HL-LHC, at least in the outer layers, far enough from the interaction point such that the radiation levels are similar to those presently encountered at the inner layers, i.e. 100 Mrad dose and $2 \times 10^{15} n_{eq}$/cm^2 particle fluence, respectively.

Simulations [17] have shown that these goals can be addressed by a) a high resistive ($>$1 kΩcm) substrate material in which the charge is collected, b) a sufficiently high bias voltage (typically 20–50 V) to supply the substrate with a high electric field and a reasonably large depletion volume according to

$$d \propto \sqrt{\rho V}$$

where ρ is the resistivity and V is the bias voltage, and by c) a large fill factor F (the ratio of the charge collection area to the illuminated pixel area). Typical numbers are $\rho = 2$ kΩcm, $V_{bias} =$ 20 V and $F = 75$%. In addition, one has to ensure that full CMOS circuitry (i.e. a balanced usage of PMOS and NMOS transistors in the electronics layer) is maintained by sufficient shielding of — e.g. in an n-substrate — the PMOS transistors in n-wells shielded by deep p-wells by use of triple/quadruple well technology as shown in figure 5.

Technologies that enable such designs are meanwhile available:

- *HV add ons:* Special processing add-ons (from automotive and power management applications) that increase the voltage handling capability and create a depletion layer in a well's pn-junction of the order of 10-15 μm.

- *high resistivity wafers:* 8 inch high/mid resistivity silicon wafers accepted and qualified by the foundry. A depletion layer develops due the high resistivity with only moderate bias voltages applied from the electronics side or a (specially processed) backside contact.

- *special technology features:* Radiation hard processes with multiple nested wells are needed and a foundry must accept some process or design rule changes in order to optimise the design for HEP-applications.

- *backside processing:* Wafer thinning from the backside and a backside implant allow the fabrication of a backside contact after CMOS processing thus yielding a strong electric field and uniform charge collection inside the sensor.

The interest in CMOS pixels for the HL-LHC has risen due to the potential of low cost, large area devices that can cover the outer layers of ATLAS or CMS. For the inner layers the possibility to achieve smaller pixels by in-pixel decoding [18] is attractive. Hence the goal for CMOS pixels suited for LHC pp-collisions is designing an intelligent CMOS pixel cell with some depletion depth (e.g. 40–80 μm) yielding a reasonably large signal ($\sim 4000\ e^-$) with fast and in-time efficient charge collection, while avoiding a long collection path on which charges can be trapped.

Three current development lines can be identified: (a) HV-CMOS pixels (high voltage), (b) HR-CMOS pixels (high resistivity), and (c) CMOS on SOI pixels. They will be described in some more detail below. An important aspect to take note of regarding all CMOS pixel developments, is the fact that the capacitance of a CMOS pixel cell seen at the input of the preamplifier has contributions from various boundary structures (figure 3). While for standard planar pixel structures the total capacitance is dominated by the interpixel capacitance, for CMOS pixels a large contribution comes from the capacitance C'_a between the collecting deep n-well and the p-well sitting above (see figure 3) [19]. Their close vicinity renders the capacitance contribution non negligible. Apart from increasing the total input capacitance, C'_a also acts as the capacitance through which any activity on the bias lines can couple via the electronics into the sensor.
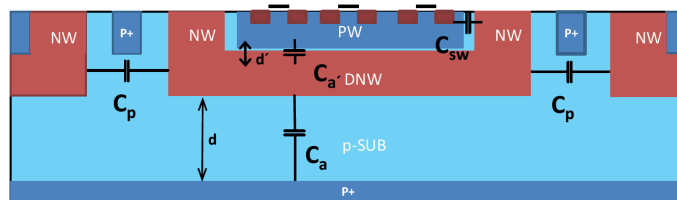
Figure 3. Capacitance contributions of a typical CMOS pixel cell to the amplification node. Apart from capacitances to the backside and between pixels a non-negligible contribution comes from the close by wells, deep n-well and p-well [19].

3.2 HV-CMOS pixels

CMOS pixels with some depletion depth have first been implemented by Peric [20] using a HV-technology with 350 nm and later 180 nm feature size. Both transistor flavours sit in a large deep n-well which at the same time acts as the charge collection node (figure 4(a)). The achievable depletion depth is expected around 10–20 μm, but measurement on prototypes suggest even larger values. The output is an already amplified signal. One, currently much discussed, possibility is to directly (via bump bonds) or capacitively (via glue bonds) couple the pixel cells to the ATLAS front-end chip FE-I4 [11] as a second amplifying and fast processing device: an active hybrid pixel detector called CCPD (capacitively coupled pixel detector). HVCMOS detectors have survived

(a) HV-CMOS principle

(b) Efficiency
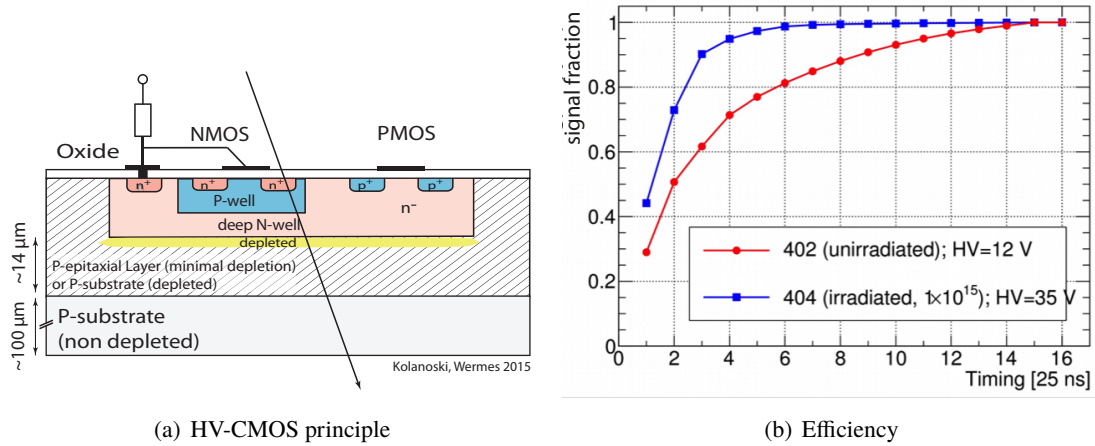
Figure 4. (a) Sketch of a generic HV-CMOS pixel structure (from [21]). Both transistor types are embedded in a large deep n-well. The process has HV-add-ons which allow bias voltages up to ∼100 V. (b) Time delay of the signal when crossing a threshold is shown in units of 25 ns for an unirradiated and an irradiated (1×10^{15} n_{eq}/cm^2) device. The HV-CMOS sensors was bonded with glue to a FE-I4 chip.

TIDs of as much as 1 Grad and fluences of 10^{15} n_{eq}/cm^2. The signal after 1 Grad is 1500 e$^-$ at a noise of about 60 e$^-$. The time-integrated efficiency drops from 99% (before irradiation) to 96% after proton irradiation to 10^{15} n_{eq}/cm^2. The signal rise time is typically 100 ns, still too slow to achieve the required high intime efficiency as shown in figure 4(b). It is observed that the timing performance improves after irradiation (blue curve in figure 4(b)), most likely due to acceptor removal such that the fraction of charge collected by drift rather than diffusion becomes larger.

By connecting three CMOS subpixels to one FE-I4-pixel one can achieve an effective pixel size of 33×125 μm via pulse shape decoding [18].

3.3 HR-CMOS pixels

Another approach uses high-resistive CMOS technologies with up to four well structures is shown in figure 5. In a >1 kΩ resistive substrate material several nested wells provide charge collection as well as individually shielded transistors. In figure 5(b) the charge collecting n-well is placed outside the electronics area providing a small capacitance at the expense of a long drift path. In figure 5(a) the collecting deep n-well also houses the electronics similar to the HV-CMOS approach, however an additional deep p-well is employed isolating the n-well which houses the PMOS transistors

from the collecting n-well. It is obvious that variant-B (figure 5(b)) will benefit from the small capacitance of the collecting node while it will likely be less tolerant against bulk damage than variant-A (figure 5(a)) due to the different path length.

(a) HR-CMOS principle: variant-A

(b) HR-CMOS priciple: variant-B
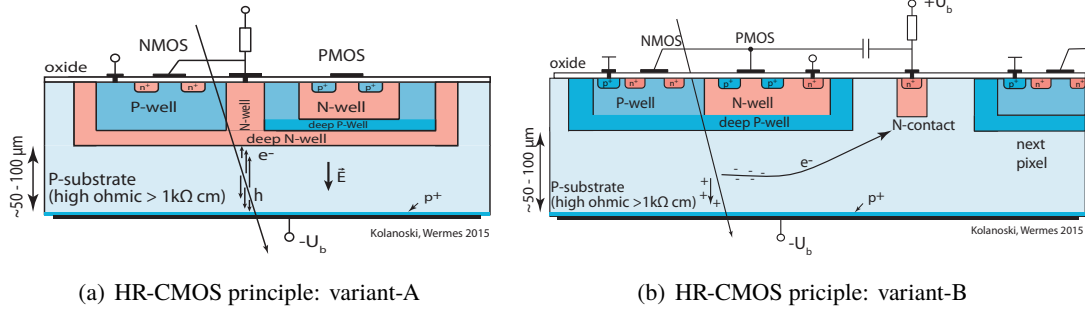
Figure 5. Structure of a HR-CMOS pixel cell. (a) Variant with a large collection n-well and short drift path; (b) Variant with a small collection n-well and a long drift path (from [21]).

HR-CMOS pixels in both variants of figure 5 have been realised [22, 24] in different technologies offering high resistive substrates, multiple wells and in some cases also a backside contact. The latter is important, although not mandatory, to provide an electric field inside the sensor which is directed from the back to the collecting nodes. Figure 6(a) shows the layout of a cell produced in 150 nm technology (LFoundry) on $2\,\text{k}\Omega\,\text{cm}$ substrate with a deep n-well structure aiming for smaller capacitance and faster rise time. A version of the cell with an n-well geometry encompassing the entire structure has also been realised.


(a) HR-CMOS pixel cell

(b) HR-CMOS priciple: variant-b
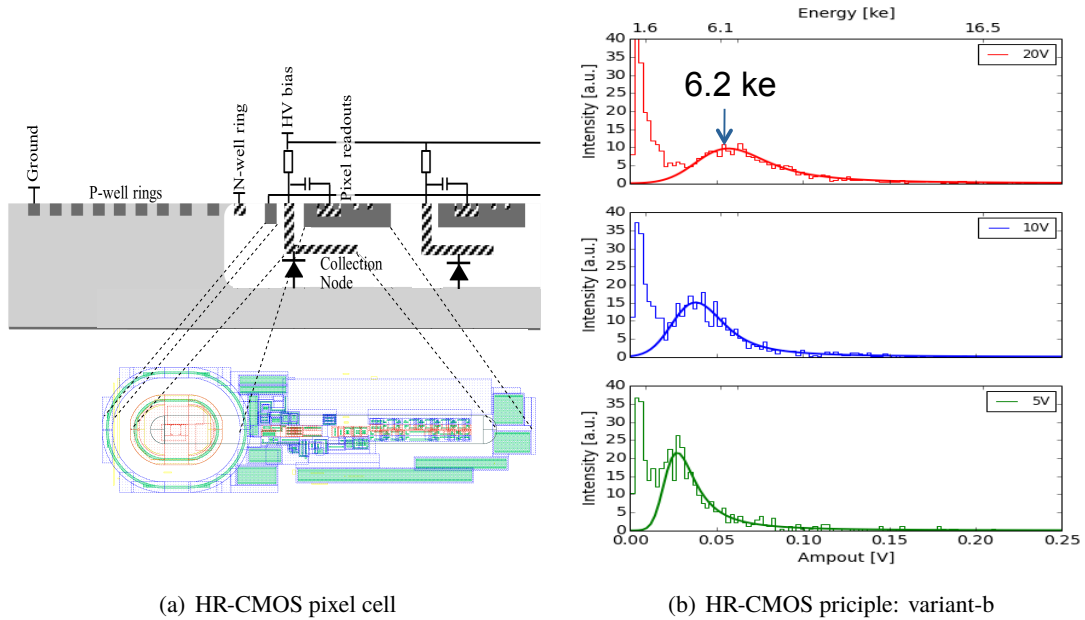
Figure 6. Variant of an HR-CMOS pixel cell with reduced capacitance. (a) cell layout in two cross sections, (b) spectrum from 3.2 GeV electrons at bias voltages of 5 V, 10 V, and 20 V. The corresponding scale of energy deposited in the detector is shown on the top.

In figure 6(b) the signal is shown after exposing the LF pixel array to a 3.2 GeV electron beam at the ELSA accelerator [23]. At a bias voltage of 20 V a mean charge of 6200 e^- is observed corresponding to about 60 μm depletion depth and confirming that the bulk resistivity is about 2 kΩ cm. In-beam timing measurements show that the fraction of in-time hits is 91% with a high threshold of 2600 e^-, a very low threshold of 190 e^- yields a fraction of 79% [23]. In another process (ESPROS, 150 nm) HR-structures including thinning and a backside implant have been prototyped (see [22, 24]).

3.4   CMOS-on-SOI pixels

The Silicon-on-Insulator technology provides a buried oxide layer (BOX) which separates the CMOS electronics from the substrate layer. Both parts are connected by vertical via structures reaching through the BOX and leading to an n-implant which acts as the charge collecting node. Monolithic SOI-based pixel structures have been developed for some time using the so-called fully depleted SOI technology [25], invented for high speed CMOS electronics with reduced (parasitic) capacitances. The CMOS electronics layer is embedded in depleted silicon. The pixel developments so far [25] suffered from effects inherent to the BOX oxide layer, most notably the so-called backgate effect and from radiation effects. There have been successful measures to overcome these drawbacks [26] for moderate radiation doses; FD-SOI pixels are nevertheless not suited for the conditions expected at the HL-LHC.

Thick film SOI, featuring trench isolation and doped, only partially depleted regions underneath CMOS transistors and thus shielding the transistors (cf. figure 7) are free of these difficulties and can also sustain mach larger radiation doses. SOI CMOS pixel detectors have been realised by [27]

| (a) SOI-MAPS-Structure | (b) Spectra | (c) Irradiation NMOS |
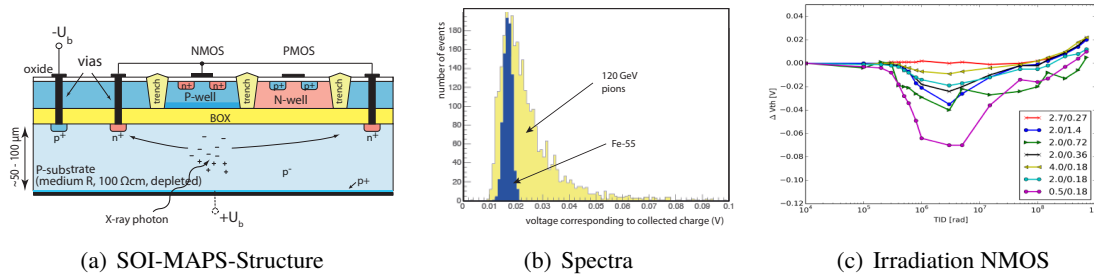
Figure 7. Depleted SOI MAPS: (a) Pixel structure on thick film partially depleted SOI. The depleted charge collection volume is separated from the electronic layer by the BOX. The transitors are isolated by tranches and shielded by doped silicon at the top part of the BOX. (b) Signal spectrum of (unirradiated) SOI pixel structures from ^{55}Fe (6 keV) and 120 GeV pions. (c) Threshold shifts of the NMOS transistor in SOI technology as a function of X-ray dose.

and characterised [28] in the lab and in test beams. Figure 7(b) shows the signals obtained with an SOI pixel matrix (XFAB, 180 nm) from ^{55}Fe as well as from a beam of 120 GeV pions. The signal peaks at about 1700 e^- corresponding to a depletion depth of 31 μm.

Figure 7(c) shows threshold shifts of the NMOS transistor of these SOI structures with X-ray radiation [29]. The maximum shift is 70 mV for NMOS transitors improving again towards higher doses because the damage at the Si-SiO$_2$ interface compensates the effect of the oxide damage.

PMOS transistors are not compensated; the shift after 1 Grad is about 100 mV. Both values are tolerable for CMOS circuitry when such threshold shifts are taken into account in the design.

4 Conclusions

Hybrid pixels have convincingly demonstrated their capability to cope with the high rate and high radiation environments at the LHC and even at the planned HL-LHC. A first upgrade of such devices is the ATLAS Insertable B-layer (IBL). However, hybrid pixels also have a number of drawbacks, among them is the material and the production costs. Intensive research and development of monolithic pixel detectors aiming to operate LHC-like environments is currently considered an attractive alternative direction. R&D profits from the rapid progress in micro electronics, meanwhile allowing a number of technology variants. CMOS pixels could offer is a low cost potential which is especially attractive for large areas needed at the outer layers of the LHC experiments, where also the radiation levels are less severe. For the inner layers, closer to the interaction point, the possibility to obtain smaller pixel sizes than with hybrid pixels is attractive.

Acknowledgments

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