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Design of a Signal Conditioner for the Fermilab Magnet Test Facility

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Dedicated to my family.

ABSTRACT

This thesis describes the design of a remotely-programmable signal conditioner for the harmonic measurement of accelerator magnets. A 10-channel signal conditioning circuit featuring bucking capabilities was designed from scratch and implemented to the level of the printed circuit board layout. Other system components were chosen from those available on the market. Software design was started with the definition of routine procedures.

This thesis is part of an upgrade project for replacing obsolescent automated test equipment belonging to the Fermilab Magnet Test Facility.

The design started with a given set of requirements. Using a top-down approach, all the circuits were designed and their expected performances were theoretically predicted and simulated. A limited prototyping phase followed.

The printed circuit boards were laid out and routed using a CAD software and focusing the design on maximum electromagnetic interference immunity.

An embedded board was selected for controlling and interfacing the signal conditioning circuitry with the instrumentation network. Basic low level routines for hardware access were defined.

This work covered the entire design process of the signal conditioner, resulting in a project ready for manufacturing. The expected performances are in line with the requirements and, in the cases where this was not possible, approval of trade-offs was sought and received from the end users.

Part I deals with the global structure of the signal conditioner and the subdivision in functional macro-blocks.

Part II treats the hardware design phase in detail, covering the analog and digital circuits, the printed circuit layouts, the embedded controller and the power supply selection.

Part III deals with the basic hardware-related routines to be implemented in the final software.

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INTRODUCTION

The Fermi National Accelerator Laboratory is an high-energy physics research facility operating under the U.S. Department of Energy, located in the outskirts of Chicago (Illinois), near the city of Batavia. Best known for hosting the Tevatron, a proton-antiproton particle collider (the biggest machine of its kind, before the Large Hadron Collider was completed at CERN in 2010), Fermilab's research fields range from physics at the micro-scale level to cosmology. International teams of scientists and engineers work at the laboratory, with several partnerships and collaborations around the world.

Fermilab is part of a collaboration with the European CERN concerning the research and development of the LHC (The U.S. LHC Accelerator Research Program). The laboratory also hosts a Remote Operations Center interconnected with both the LHC and one of its six experiments, the Compact Muon Solenoid (CMS) detector.

A Technical Division operates inside the laboratory with duties that range from experiment support, to the development and in-house manufacturing of accelerator and detector components. One of the main occupations of TD is the R&D and construction of accelerator magnets which requires, besides the manufacturing assets, proper testing facilities.

1 THE MAGNET TEST FACILITY AT FERMILAB AND THE CHISOX UPGRADE PROJECT

Fermilab's Magnet Test Facility (MTF), operated by the Technical Division (in particular, by the Test & Instrumentation Department) and located inside the Industrial Building 1, is where all magnets built by the TD are tested. This facility includes features and equipment aimed at the characterization of a vast range of magnets intended for high-energy physics experiments, both conventional and superconducting, and has been in operation since late 1970's.

The MTF houses warm and cryogenic test stands along with their supporting systems, such as: high-current power supplies, water and nitrogen cooling systems, helium liquefiers, vacuum systems and all the electronic test equipment.

During the years, the MTF was used to test magnets belonging to the Tevatron, to the LHC and several other particle accelerator experiments.

The Tevatron final shutdown, occurred at the end of September 2011, did not mean the end of the line for magnet development and manufacturing at Fermilab's Technical Division. In fact, magnets in development for new experiments at Fermilab, as well as planned LHC upgrades, still require testing at the MTF.

The integrated measurement system used to run all tests at the MTF is called the "CHISOX Measurement System" and owes its name to the Chicago White Sox baseball team.

The CHISOX is an apparatus composed of electronic test equipment and management software whose purpose is to ease and automate the testing procedures and maintain a database of all the results. Designed and built in the '90s, the CHISOX has now become obsolete and no longer supportable, a relevant limiting factor for MTF operations and improvements. An upgrade

Figure 0.1: LHC quadrupole production magnet installed at the Magnet Test Facility.

project was thus started to completely replace the system with new hardware and software.

The signal conditioner object of this thesis is part of this upgrade project and is intended to replace a number of electronic devices that were absorbed inside the "harmonic measurement" test equipment during its lifespan.

2 SIGNAL CONDITIONING REQUIREMENTS

The focus of this thesis project rests on a specific testing capability of the MTF, the harmonic measurements[1]. This kind of measurement is used to obtain an "harmonic description" of accelerator magnets field, that can later be used to characterize the magnetic field quality or for particle tracking purposes.

Harmonic measurements are performed by placing a rotating coil probe inside the field region of the magnet (the "aperture"), so that it intercepts the azimuthal flux of the generated field and is able to measure its variation while spinning on the same axis as the magnet's (illustrative set-up in figure 0.2). The data acquisition is synchronized using a precision angular encoder (placed on the probe shaft) as triggering source.

The harmonic coil transducers used at the MTF are several and vary in size, sensitivity and impedance, as well as physical construction. Most are made of wound copper wire, while other new designs come in the form of PCBs (Printed Circuit Boards) with etched coil-like tracks.

Those probes are used as voltage sources to measure the magnetic field intensity and its harmonics, in this case up to a frequency of approximately $1\,kHz$.

Field measurement for particle accelerator magnets usually requires an accuracy down to 10^{-4}. For this reason, one of the signal conditioner requirements was an accuracy of 0.025% for all gain/attenuation settings.

The most relevant characteristics of the probes, from the point of view of signal conditioning, are the expected output voltages, the maximum output

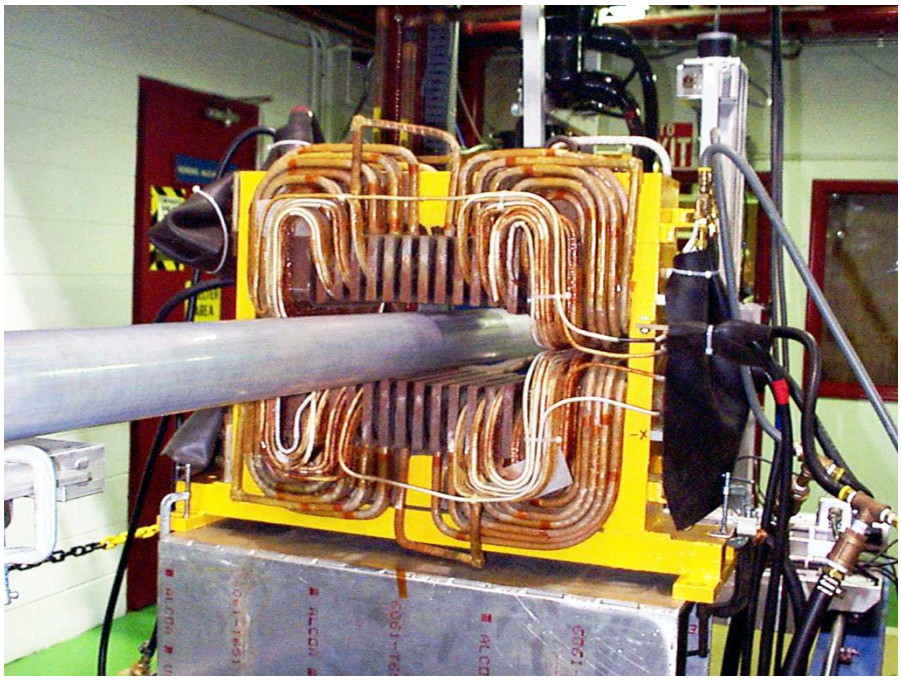


Figure 0.2: SMA magnet under test at the MTF. The gray cylinder is a rotating "Morgan" coil probe.

current (load constrains), their grounding configuration and the useful signal bandwidth.

The following list summarizes the relevant specifications addressed during the design process:

- signal voltage range: from $\pm 10\,mV$ up to $\pm 200\,V$;
- loading requirements: at least $100\,k\Omega$ towards ground;
- fully floating sources, with high common mode signal rejection;
- frequency bandwidth: from DC up to $\sim 1\,kHz$;

The signals originating from the probes are to be converted into digital form by an array of precision ADCs (Analog to Digital Converters), with resolutions of $18\,b$ (10^{-6}) and $24\,b$ (10^{-8}) over an input range of $\pm 10\,V$.

Since all the probes are configured as floating balanced sources, both the ADCs and the signal conditioner have a fully balanced configuration.

The purpose of the signal conditioning device, which springs from the previous statements, includes but it's not limited to:

- Being able to optimally fit the wide voltage range of the input signals to the fixed voltage range of the ADCs, thus allowing measurements with the highest possible resolution. In order to do this, the signal conditioner shall provide a way to amplify/attenuate those signals.
- Moreover, the gain of such a device shall be adjustable during operation, in order to track the amplitude fluctuations of the sources.
- Present the same loading impedance to the probes, regardless of the ADC used for sampling the data, so that it always be above the required value (i.e. buffering capabilities).

- This impedance shall remain as constant as possible under different experimental conditions, in order to guarantee consistent measurements .
- Preserve the differential nature of the signal, which also guarantees a superior immunity to common mode noise.
- Filter out the high frequency components picked up by the probes.

Aside from the previous list, other functionalities were requested by the end users. Those functionalities are generally related to usability and system integration and are listed below:

- The device shall provide a total of 10 cloned and independent measurement channels.
- The device shall integrate bucking capabilities (see 3.2), gain precision requirements do not apply to this function.
- The device shall be remotely programmable by the supervising measurement system, which is constituted by a network-oriented application framework and ultimately uses a LAN to control all the electronic test equipment.
- Calibration functionalities shall be remotely controllable and automatic.
- The signal conditioner shall be able to switch the gain settings during normal operation, and this shall take no more than $50ms$ ("hot-switching").
- Each channel shall provide a secondary route that bypasses the signal conditioner circuitry.
- The device shall withstand input signals up to $\pm 300\,V$ without deteriorating.
- The device shall provide an output saturation detector on each channel, triggering when the signal swings off the $\pm 10\,V$ rails. This event shall be notified on both the device's own front panel and to the aforementioned measurement system.
- A display interface shall be present on the front panel, which will show the current status of the device (including the gain settings for all the channels).
- The device shall implement diagnostic logging for several kind of events: saturation, over-voltage, brown-out, environmental parameters (temperature and humidity), user access and intervention, illegal operations and so on.

2.1 *Signal quality requirements*

The role of the signal conditioner within the measurement chain would require this device to only affect those signal properties that are considered non-ideal for the measurements' sake. In this particular case, as pointed out in the previous section, the conditioner shall provide precise amplification and frequency filtering.

On the other hand, any additional alteration inevitably caused by the device on the measured signal is considered a form of data corruption and needs to be kept within some bounds.

The unwanted effects are:

- The addition of noise to the signal.
- Non-linearities of the circuitry, that distort the waveform.
- Cross-talk between channels and interference from other parts of the signal conditioner.
- Signal offsetting and common mode gain.
- Rippling of the gain factor over the frequency bandwidth.

The signal conditioner was designed for compromise, that is, the original requirements were deliberately overspecified and the device was developed as a balanced trade-off between them.

As a matter of fact, since this signal conditioner is not going to be manufactured in series but probably in less the 5 copies, the price per unit would have become unbearably high if those requirements were to be strictly respected.

Below are listed the target specifications for each channel:

- Noise power spectral density $\leq 2\,\frac{nV}{\sqrt{Hz}}$.
- Total harmonic distortion $\leq -100\,dB$ @ $1\,kHz$, $-1\,dBFS$ output.
- Crosstalk channel to channel: $\leq -130\,dB$.
- Input voltage offset $\leq 5\,\mu V$, $CMRR \geq 120\,dB$ @ unity gain.
- Pass-band flatness within $\pm 0.02\,dB$.

These requirements were discussed with the end users throughout the design phase and were given different priorities. Some ended up to be completely unobtainable by using commercially available electronic components.

2.2 *Analog bucking*

Profiling of the magnetic field high-order harmonics is a relevant topic in the field of testing and characterization of magnets intended for particle accelerators [2].

Rotating coil probes are designed and built with several independent loops that may be used to isolate high-order harmonics of the magnetic field by "bucking" the signals.

Bucking is the procedure that highlights an arbitrary harmonic by properly summing the signals generated by the individual coils of the probe, effectively canceling out the unwanted harmonic components.

Although several methods exist to perform the bucking of signals[3, p. 408], this project requirements explicitly limited the feasible solutions by stating that: a) bucking must be performed in an analog fashion; b) this functionality must work besides, and not preclude, the single channel signal conditioning.

All of the 10 signal conditioning channels were required to be clamped to a single analog bucking circuit with remotely controllable switches.

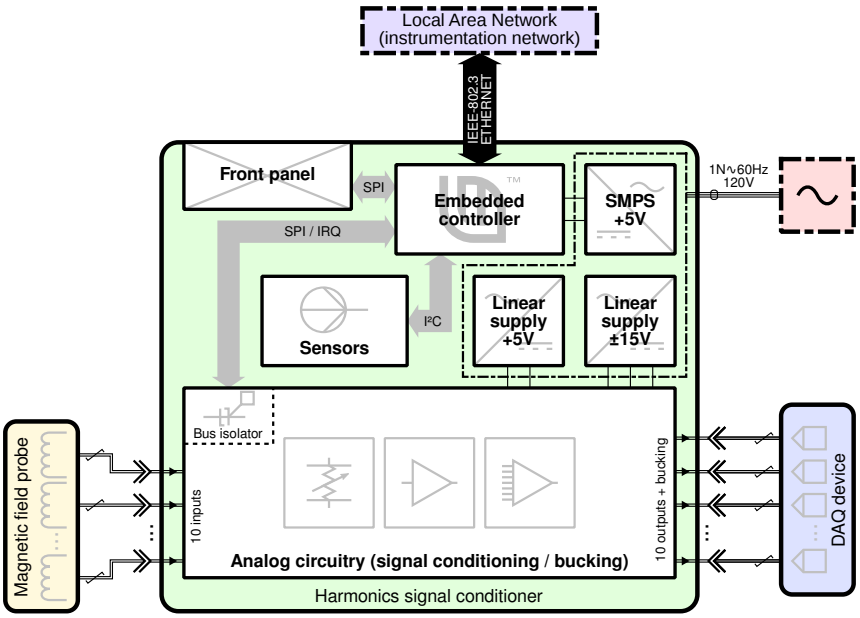


Figure 0.3: Signal conditioner high-level block scheme.

Controlled gain precision was not required for the bucking circuitry because the relevant information lies in the relative amplitudes of the harmonics. Moreover, technical personnel performing measurements are usually required to manually adjust the amplitude of single signals in order to obtain high bucking ratios. This feature was implemented as well.

3 A NOVEL HARMONICS SIGNAL CONDITIONER

The signal conditioner design was carried out with a top-down approach, starting from the logical subdivision of the target functionalities in macroblocks that were subsequently developed to match both specific and system-wide requirements.

The logical decomposition of the signal conditioner is better laid out in a graphical scheme (figure 0.3), in which the following components are identified:

1. The analog circuitry. The core of the device, where all the signal conditioning is performed.
2. The embedded controller. A full-fledged single board computer that works as an interface between the outside world and the inner circuitry.
3. Power supplies, three of them. Those used for powering the main analog circuitry are linear, a choice made to avoid feeding switching noise to this sensitive part of the system.
4. The front panel interface, constituted by a small display and some buttons.
5. Sensors used for monitoring the device internal conditions (humidity and temperature).

The previous list only shows the physical components of the signal conditioning device. A remotely controllable device like this also needs a firmware and a virtual interface driver. This software has to be fully compatible with the system framework already used to operate the MTF [4, 5] and is thus under joint development with the interested persons.

An effort was put in the separation of the digital and analog electrical domains: the digital components present on the analog board were limited to the minimum necessary for configuring the signal conditioning behavior (gain switching, calibration, and a few diagnostics). No "live" digital components are present on the analog circuitry; that is, there are no on-board digital clock sources that might cause noise issues.

An isolated digital bus (Serial Peripheral Interface) interconnects the analog and digital boards. SPI was chosen due to its widespread adoption in the IC industry, its simplicity of use and the potential for high-speed communications. An additional hardware interrupt line was provided, due to SPI being a single-master bus that doesn't permit slave devices to initiate communication on their own.

The digital bus only remains active (digital signals and clock present) during the brief time lapses of configuration. The digital noise possibly fed-through to the analog circuits during this brief periods of activity, even when hot-switching the gain settings, is not going to be a problem, since valid measures are not expected then.

Galvanic isolation on this bus was added to preserve both the digital board and the devices attached to it in the event of a catastrophic failure of the analog part. Indeed, the signal conditioner is planned to be deployed inside an industrial environment - with all the related hazards involved.

All the parts listed above were bought from third-party manufacturers, except for the analog circuitry, since the requirements were matched by commercially-available devices.

The whole hardware development effort was thus placed on the main analog part, that was designed from scratch. The greatest challenges addressed during this phase were mainly related to the required gain precision, the analog bucking features and the required input impedance.

3.1 *Attaining the required precision for all gain settings*

Several factors influence the precision of the signal conditioner gain. Since the gain is defined at a circuital level by resistors (typically by ratios of resistor values - see chapter 4), it's plain that the performances of resistors represented one of the main concerns: precision, thermal drifts, aging and so on. Resistors thus had to be chosen for their precision and stability.

Moreover, the signal conditioner device had to be remotely programmable: this implies that some "electronic switches" were needed in order to change the gain settings. Ideally, switches should not disrupt the signals they're carrying but, as it is for the resistors, real electronic switches operate far from ideal. Consequently, good switches were another fundamental ingredient of the system, as explained in chapter 5.

Choosing the best components was, anyhow, never meant to be a solution for attaining the required gain precision.

In fact, using high-precision components was only a mean to keep drifts, circuit unbalances and other non-ideal effects to a minimum, while the gain accuracy was assured by the calibration circuitry.

The calibration circuits were designed as precision-adjustable resistive attenuators using digital potentiometers as trimming elements. All the amplifier/attenuator stages were thus designed with gains slightly higher than the nominal value, so that the calibration attenuator would be able to adjust the errors under any possible initial condition.

Digital potentiometers were adopted in order to provide the required functionalities of automatic and remote calibration but also had the side effect of reducing the complexity of the circuitry. By using a digital potentiometer, the calibration data of each gain setting can be stored in a memory and restored when needed. This way, a single potentiometer per channel is enough to trim all the gain settings (see section §5.3).

3.2 *Permitting analog bucking along with direct signal conditioning*

Several approaches exist for performing analog bucking, with the simplest being "coil stacking". Coil stacking means simply placing the coil terminals in series, thus obtaining the sum of the voltage signals.

This method, other than being potentially dangerous (extremely high voltages may develop at the coil terminals), is fundamentally unfit to be used alongside the direct channel conditioning. Common-mode voltages arising from the series of stacked coils would make the connection of amplifiers to single terminals a major problem.

Another common method is to pass the coil signals through pre-amplifiers / attenuators and then sum the voltages with another amplifier.

While this solution might appear fit for working together with direct channel conditioning, it's got a serious drawback: feeding the harmonic-rich voltage signals to the pre-amplifiers will result in phase shifts and added distortion, making a good bucking troublesome, if not utterly impossible.

The signal conditioner's final circuitry was thus based on a completely different approach: current-mode bucking.

This solution consists in drawing little currents (order of µA) from the probe signals and summing them together at the input node of a trans-impedance amplifier. The amplifier has the purpose of both providing a fixed summing node (virtual ground) and converting the resulting current back to a voltage.

Current pickup is performed by adjustable resistor networks (using digital potentiometers) clamped in parallel to the inputs of each direct channel signal conditioner. High resistance values are needed to keep the total shunt input impedance above the requirements.

3.3 *Keeping the input impedance high*

One of the main requirements of the signal conditioner was about the input impedance of the device. Providing an high input impedance over the specified input voltage range proved to be a challenge, in particular at both ends of the signals dynamic, for different reasons.

3.3.1 *The upper end of the input dynamic: signals above $\pm 10\,V$*

Signals exceeding $\pm 10\,V$ are those that swing off the signal conditioner output range and thus need to be attenuated. The resistive attenuator had forcibly to be placed at the input of the signal conditioner because the

gain/buffering stage can't handle high voltage signals. This attenuator, when enabled, is thus loading directly the source coil.

At the same time the bucking circuit might be active, which means that two shunted resistive loads are connected to the probe.

The trade-off that had to be done ended up being between the magnitude of the bucking current (which defines the intrinsic load of the bucking circuit) and the noise introduced by the attenuator (higher with increasing resistance values).

However, The reduction in bucking current was bounded by the gain-bandwidth product of the cascaded trans-impedance amplifier, as well as the noise floor. On the other hand, the added Johnson noise arising from the use of high-value resistors was a side effect barely relevant with ample signals. A third factor to consider was the actual availability of high-precision, high-value resistors, which are limited to $\sim 1\,M\Omega$ (higher values were available only with reduced performances).

The issue was settled by choosing a bucking current in the order of $10^{-6}\,A$ and keeping the attenuator loading in the range of $10^{6}\,\Omega$.

3.3.2 *The lower end of the input dynamic: signals below $\pm 100\,mV$*

The problem was somewhat different for tiny signals. Here, obtaining a bucking current of $\sim 1\,\mu A$ requires a load value of less than $10^{5}\,\Omega$, even though no attenuator is likely to be used (which means working with the single channel conditioner at maximum input impedance). The bucking circuit was thus either going to violate the requirements, or to provide an added buffering stage.

Feedback from end users pointed towards the reduction of the input impedance down to $10\,k\Omega$ (only under these conditions) and avoiding the introduction of active components.

Mid-range signals work with the highest input impedance, thanks to the design of the amplifier stage. The configuration chosen was that of a fully-differential instrumentation amplifier, whose inputs are directly attached to the coils and thus are truly high-impedance (see section §4.2).

The only limitation of this circuit was the need of biasing resistors for the amplifier inputs, due to the probe coils being isolated from ground. $10\,M\Omega$ resistors were selected for the purpose after choosing very-low input bias current amplifiers. Thus, the final input impedance obtained was slightly less than $10\,M\Omega$.

4 PROJECT ROAD-MAP AND CURRENT STATUS

Being a project with a medium-long lifespan, a sort of "technology road-map" was devised to keep track of the development status of this signal conditioner.

At the time of writing, the hardware development phase is finalized, while the firmware development is put on hold due to the lack of feedback required from the final hardware. Aside from this, a proof-of-concept software was developed to test the main digital components used in the device.

As both the software and the firmware are supposed to be compliant to an internal codebase, most of the development rests with the team of people dedicated to this task. Consequently, it is not easy to assess a completion time for this part of the project.

Regarding procurements and manufacturing, PCBs are currently in production at Sunstone Circuits, Portland, OR, while all the electronic components have already been ordered. Some components, in particular high precision resistors, are manufactured on-demand by the suppliers: this caused a long lead time for those components, up to 8 months.

The various development phases are here reported in retrospect, along with the amount of time used to complete them. An estimated time to completion is provided for the ongoing work.

1. Project specification and planning [1 month]
2. Hardware design [5 months]
3. Firmware and software design [ongoing, e.t.a. may 2012]
4. Procurements [almost over, took 8 months]
5. Device assembling [estimated 1 month, after PCBs manufacturing]
6. Testing and commissioning [estimated 2 weeks, after assembling]

Part I

SYSTEM DESIGN

1 INITIAL REQUIREMENTS

Below is reported an extended and ordered list of requirements, divided by topic.

The signal quality requirements, such as noise and linearity, were over-specified at the beginning of the project. They were thoroughly discussed with the end users during the design phase, and amended to what was reasonably attainable without requiring exotic and expensive solutions.

1.1 FUNCTIONALITIES

- Direct channel signal conditioning.
- Analog bucking, with each channel manually adjustable between 95% and 100% of the amplitude.
- Automatic calibration (using external devices).
- Remote control of all settings and calibrators.
- Diagnostics: output saturation, brown-out and surge of the supply voltage, temperature and humidity.

1.2 SIGNAL CONDITIONING REQUIREMENTS

- Balanced differential input/output.
- Input voltage range: $\pm 200\,V \rightarrow \pm 10\,mV$.
- Output voltage range: $\pm 10\,V$.
- Input impedance $\geq 100\,k\Omega$ (differential and single-ended), may be reduced down to $\sim 10\,k\Omega$ for the bucking of signals below $\pm 0.2\,mV$.
- Signal bandwidth: $DC \rightarrow 1\,kHz$.
- Input over-voltage protection to $\pm 300\,V$.
- Gain/attenuation accuracy $\leq 0.025\%$.
- Passband gain flatness $\leq \pm 0.02\,dB$.
- Input-referred voltage offset $\leq 5\,\mu V$.
- Total harmonic distortion $\leq -100\,dB$ @$1\,kHz$, $-1\,dBFS$.
- Common-Mode Rejection Ratio $> 120\,dB$ (at unity gain).
- Noise power spectral density $\leq 2\,\frac{nV}{\sqrt{Hz}}$.
- Crosstalk channel-to-channel $< -130\,dB$.

$-1\,dBFS \approx 8.9\,V$.

The Common-Mode Rejection Ratio (CMRR) is defined as the ratio of the differential gain to the common-mode gain of an amplifier.

1.3 INTERFACING

- Ethernet 100BASE-TX - 802.3 (24) interface (remote control).
- Front panel displaying configuration and output saturation diagnostics.

- 19-inch rack mount enclosure, maximum height 5 units.
- Input connectors on the front of the device.

2 TARGET SIGNAL CONDITIONER SCHEME

The design started with the definition of the core signal conditioning circuitry, stripped of all the parts that could be offloaded to other, readily available, devices. This step was taken to reduce the design effort and improve the ease of servicing.

The fundamental part that had to be designed was the analog circuitry, along with the minimum digital components sufficient to provide the required remote control capabilities. Other parts, such as power supplies and the embedded controller, were kept separated and bought from third party companies, since commercially available components fitted the specifications.

The analog circuitry was thus developed keeping the digital components to a minimum, so that digital signals would not interfere with the measurement signals during operation.

figure 2.1 illustrates the functional parts that were integrated within the analog circuitry, which represented the main design effort of the project. The following sections describe the solutions adopted for each part.

2.1 DIRECT CHANNEL CONDITIONER

The direct channel conditioner is the part of the device committed to fitting the input voltage signals to the dynamic range of the analog-to-digital converter that is attached at its outputs. This circuit needs to provide both gain and attenuation, given the wide range of the input signals.

Commercially available programmable gain amplifiers and attenuators were deemed unfit for this application due to their limited overall performances that, in the majority of cases, can't be externally trimmed due to the high level of integration of these devices.

Gain programmability was thus achieved by using high performance switches to select the correct high precision resistor, out of a set that provided a pool of predefined amplification/attenuation values.

The direct channel conditioner was designed as a two-stage circuit composed of an attenuator followed by a fully differential amplifier, both programmable. The attenuator stage is bypassed when the input signal requires amplification (voltage range $< \pm 10\,V$), while the amplifier converts to an unity-gain buffer when the attenuator is engaged. The whole chain may be bypassed, if necessary.

Gain and attenuation settings were provided covering each decade with three steps, using the 1-2-5 series:

- Attenuation: $\frac{1}{20}$, $\frac{1}{10}$, $\frac{1}{5}$, $\frac{1}{2}$.
- Gain: 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000.

The maximum attenuation will be used to scale $\pm 200\,V$ signals down to $\pm 10\,V$, while the maximum gain factor will similarly be used to amplify $\pm 10\,mV$ signals.

When the attenuator is bypassed, the gain stage, a fully differential amplifier (outlined in section §4.2), directly presents two integrated circuit input pins to the source probe. This represented a potential weakness of the circuit when considering that the input signals might reach amplitudes of $\pm 300\,V$.

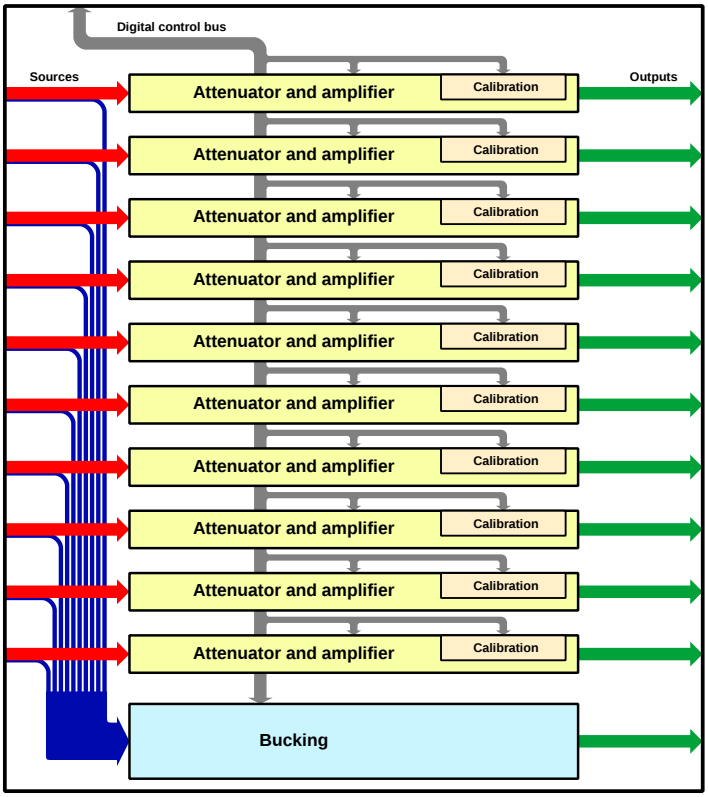


Figure 2.1: Functional blocks of the signal conditioner analog circuitry.

Therefore, a voltage clipper circuit was put before the amplifier inputs, protecting the integrated circuits by clamping the signals to the power supply rails.

The input attenuator did not need any form of protection, thanks to its high-impedance and the voltage rating of the components (see section §4.1).

2.2 BUCKING CHANNEL CONDITIONER

As pointed out in the introduction (page xxii), the main challenge of bucking was the ability to provide this functionality together with direct channel conditioning.

The basic approach to bucking is the "stacking" of the coils terminals, which means the coils are put in series, so that the output signals sum and/or subtract. This method is fundamentally unfit to be put side by side with direct channel conditioning because high common-mode voltages may develop at the coil terminals.

The solution was found by bucking currents, rather than voltages, while isolation between the channels was guaranteed by a (virtual) short circuit summing point.

Small currents are extracted from each input signal by means of high-impedance passive networks and then routed towards the inputs of a fully differential trans-impedance amplifier. This amplifier configuration ensures that its inputs are in "virtual short-circuit", thus making each source channel virtually transparent to the others.

All of the 10 channels where routed to the same trans-impedance amplifier, as per the requirements.

Detailed explanations of the voltage-to-current converters and the fully differential trans-impedance amplifier are provided in section §4.3 and section §4.4.

A secondary voltage amplifier had to be cascaded to the trans-impedance amplifier because, due to the limited gain-bandwidth product of the adopted operational amplifiers, the transresistance was not enough to output a full range signal in all cases. This amplifier was designed using the same configuration chosen for the direct channel signal conditioner, although the number of required gain presets was smaller.

A detailed block diagram of the analog part of the signal conditioner can be drawn using the information presented in this and in the previous sections. figure 2.2 shows the analog components along with their interconnections; the physical subdivision of the circuitry into two PCBs will be explained later, in chapter 7.

2.3 Remote control and calibration facilities

Complete remote control of the signal conditioner was requested in order to deploy the novel device as part of the fully-automated measurement system being developed at the MTF. Each single feature of the signal conditioner had to be made available to the instrumentation network.

Signal path selection and gain switching were implemented using electronic switches (relays and analog multiplexers) activated by logic signals. Because of the huge amount of controllable features present on the board, bringing out the whole control signals from the analog board would have required an unreasonable amount of wires. Therefore, the analog board was populated with glue logic having the purpose of reducing all the digital input/ouputs to a single bus. Serial Peripheral Interface (SPI) was the bus technology of choice because of its widespread adoption in the semiconductor industry, its ease of use and high performances.

Several GPIO (General Purpose Input/Output) integrated circuits were added to the analog circuitry in order to control all the programmable features with the embedded controller by means of SPI communication. This solution greatly reduced the amount of wires needed to control the signal conditioner but other factors, such as the physical extension of the circuitry and incompatibility of some SPI components (as explained in section §6.1), prevented the adoption of a single SPI bus from interconnecting all the digital components. In order to further reduce the interface connections, a custom SPI logic buffer/multiplexer was implemented that routes all the digital devices on a single 4-wire SPI bus (see section §6.3).

Other device features requiring a digital bus connection were diagnostics and calibrators.

Diagnostic functions were interfaced using an interrupt-driven paradigm: a chain of interrupt manager ICs receive the event triggers from all over the analog board and assert a single hardware interrupt line. This interrupt request is routed to the embedded controller, which will run an ISR (Interrupt Service Routine) to query the board status. Querying of the interrupt managers is performed via SPI, but these devices were not placed under the supervision of the SPI buffer in order to keep the ISR simple.

Calibrators were implemented as built-in additions to amplifiers and attenuators: as such they are not shown in figure 2.2 but represent inner workings of the circuits. The trimming elements of these calibrators are precision digital potentiometer used in rheostat mode, controlled via SPI.

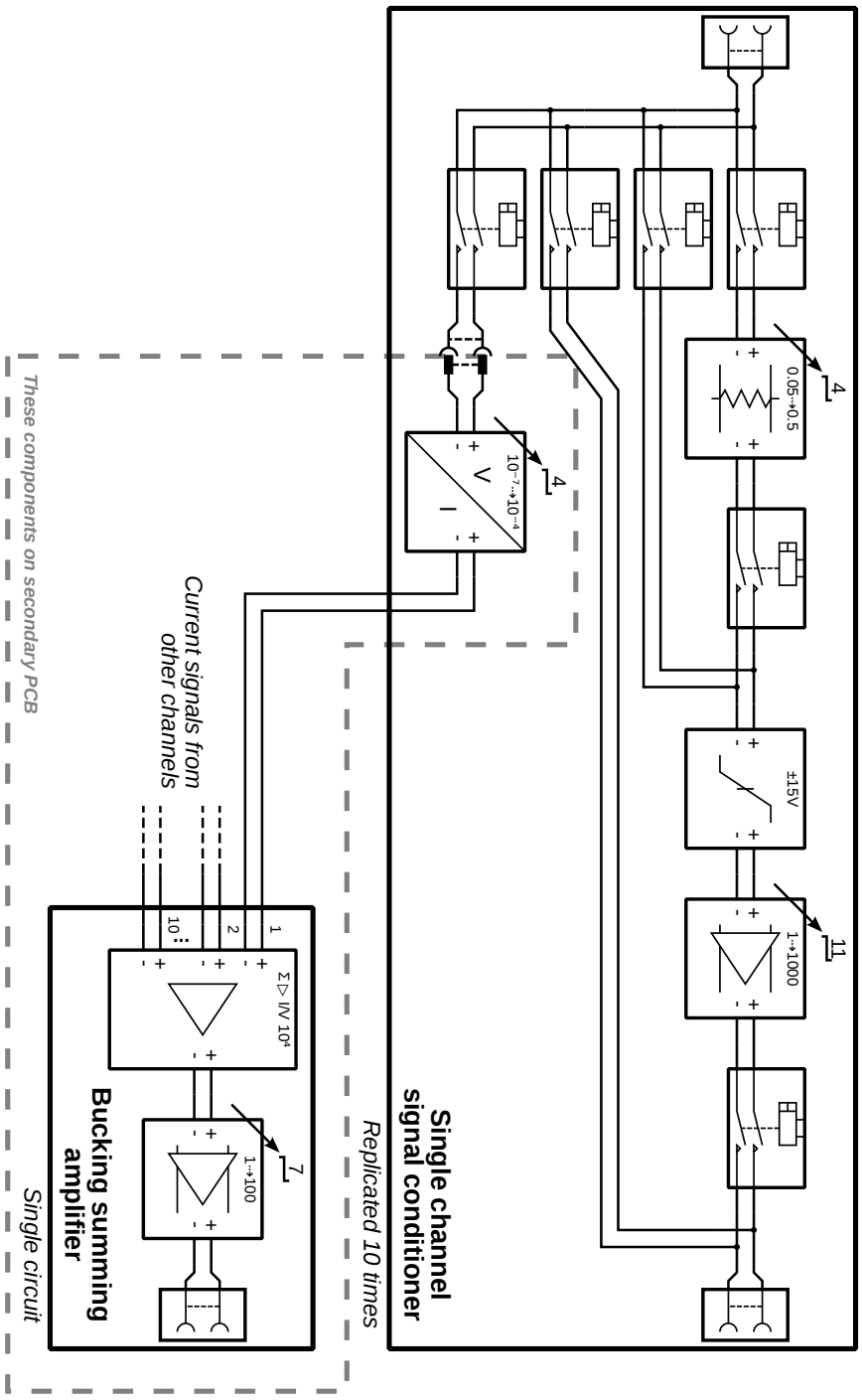


Figure 2.2: Detailed block scheme of the analog circuitry.

For a detailed explanation of how calibrator works, refer to section §5.3. The adoption of digital potentiometers permits the storage of their calibration setting for each gain preset, allowing a single potentiometer to trim all those presets. The calibration settings are saved in the memory of the embedded controller and restored during gain switching.

The calibration process involves the use of a stable source and a precision voltmeter to adjust the calibrators to the correct settings. The trimming has to be done for each gain/attenuation preset of every channel, making it a rather lengthy process. Since the calibration process requires the interaction of three different devices, it will be executed by an external software over the instrumentation LAN.

3 OVERALL DEVICE DESIGN

The blueprint emerging from the previous chapter needs to be completed with additional components, in order to obtain a fully functional device.

3.1 THE EMBEDDED CONTROLLER

The embedded controller, the device that has the duty of managing and interfacing the signal conditioner, had to be chosen starting with the following base requirements:

- Ability to store and execute code (firmware).
- SPI bus master (to control the signal conditioner).
- Ethernet 100BASE-TX - 802.3 (24) support (to interface with the instrumentation LAN).
- Graphical display (monitoring/diagnostics).
- Mass storage device (calibration storage and logging).

Given the present widespread use of advanced microcontroller units (MCUs) and Systems-on-Chip (SoCs) in multiple sectors of consumer, automotive and industrial electronics, and the availability of inexpensive, feature-rich evaluation kits from several semiconductor manufacturers, the choice of the embedded controller was oriented from the beginning towards this kind of solution.

Evaluation kits had on their side, also, the advantage of being designed for flexibility, since they are intended to fit the needs of a wide range of system developers.

The embedded controller ultimately chosen was the Stellaris® LM3S8962 evaluation board produced by Luminary Micro (now part of Texas Instruments). This board, based on an ARM® Cortex™-M3 MCU, fitted all the requirements and had some additional advantages: support of other buses (such as I²C) and, above all, being a LabVIEW Tier 1 device.

LabVIEW, the famous graphical development environment from National Instruments, is widely adopted in Fermilab's Technical Division and permits integration with the measurement system framework already running at the MTF [4, 6]. A Tier 1 device is an embedded device fully supported by the LabVIEW Embedded Module for ARM, that is, every functionality is programmable at a graphical level with the code already provided by the extension module and no low-level code has to be written.

A thorough description of the embedded controller is given in chapter 8, while the software is treated in Part iii.

3.2 POWER SUPPLIES

The adoption of excellent power supplies was implied in the tight performance requirements of the signal conditioner.

When selecting this part of the system, the main concerns regarded reliability, stability and noise. The analog circuitry was not designed to include any

power stage or power hungry device, which means that significant loading variations are unlikely to occur during normal operation. Moreover, relay coils were attached to a different supply than active analog components, effectively isolating the signal path from that kind of transients.

Linear regulated power supplies were chosen for the analog circuitry in order to obtain the stablest and cleanest supply voltages. A Dual $\pm 15\,V$ unit for powering the analog components and a $5\,V$ unit for the relays and digital ICs.

The embedded controller was designed to be bus-powered by an USB host, thus a small, switched-mode power supply was deemed sufficient to power it up.

All the three selected power supplies are produced by Acopian, a company with a history of product quality and reliability. More details about power systems are given in chapter 9.

3.3 Environmental monitoring

Environmental monitoring of the device was requested only for rough logging purposes. Therefore, temperature and humidity sensors could be chosen from the pool of low-end integrated devices having low prices.

Those sensors were placed on a small PCB attached to the signal conditioner chassis and directly wired to the embedded controller. Readout is performed using the I²C bus.

A brief explanation of this feature is provided in section §9.3.

3.4 External and internal interfacing

Aside from the already mentioned ethernet interface, two other external interfaces were integrated in the signal conditioner: a human interface (the front panel) and a firmware debugging interface.

The front panel consists of an OLED display with 5 push-buttons and a series of LEDs that light up whenever a channel is saturating. The display is used to shown the current configuration of the analog circuitry, with the buttons providing a mean to browse through the information.

The debugging interface is a USB guest provided by the embedded controller that can be used to access an on-board JTAG emulator (see section §8.2). This way, one can debug the MCU and upload a new firmware in-system, without the need to disassemble the device

The internal interfacing of the various parts was designed keeping in mind the failures that might occur in the circuitry, to prevent any faulty condition to affect other components through the electrical connections. From this point of view, the only interface deemed critical was the digital bus connecting the embedded controller to the analog board. Therefore, Galvanic isolation was added to this bus by using high-speed *i*Coupler® digital isolators from Analog Devices.

The selected transformer-coupled isolators can withstand voltages up to $2.5\,kV_{rms}$, providing sufficient equipment protection in case of catastrophic failure of either side of the bus, at the cost of slightly lowering the SPI bus clocking speed. For further information on this topic, see section §6.6.

Part II

HARDWARE DESIGN

4 AMPLIFIERS AND ATTENUATORS

Amplifiers and attenuators constitute the fundamental building blocks of the signal conditioner and their design influences the device quality and performances above any other factor.

As it is explained in the following sections, keeping the circuits as simple as possible was the key choice in reducing the amount of factors that could badly affect the behavior of the signal conditioner. This had the side effect of reducing the degrees of freedom of the design, but it ended up not affecting the development phase.

Initial considerations must be made about electronic components, regarding their performances and availability. Indeed, real components have performances limited by their manufacturing technology, calling for thorough estimation and correct addressing of the non-ideal effects they introduce inside electronic circuits.

The design process of the signal conditioner was challenging about the containment of such non-ideal behavior of components, given the tight requirements in signal quality (listed in chapter 1). A good start was to address the stability of the components with respect to environmental and operating conditions.

Gain and attenuation presets of the analog circuitry are set by the value of resistors and subsequently calibrated to reach the desired accuracy. It is clear that calibration would be completely futile if the values of resistors were to drift excessively because of, for instance, slight changes of the ambient temperature or even amplitude variations of the measured signal.

The first task was thus to investigate the availability of high-quality resistors showing good accuracy and excellent stability. The candidate resistor technologies with the best characteristics turned out to be Vishay's Bulk-Metal Foil and Z-Foil. Resistors belonging to these series can have absolute value tolerances down to 0.001% and temperature coefficients down to $\pm 0.05 \frac{ppm}{°C}$ (see [ref - appendix] for other specs).

Ultimately, the resistors used in the signal conditioner were chosen with a tolerance of 0.01% from the following series: RCK (through-hole, high-value, high-voltage), VSMP and VFCP (surface-mount). These resistors are manufactured on-demand with custom values, that is, their resistance needs not be part of a preferred numbers series.

Preferred number series for electronic components, called the E-series, are defined in IEC standard 60063.

Another ubiquitous component is the capacitor. Throughout the signal conditioner, capacitors are mainly used for supply decoupling and for tuning the frequency response of amplifiers. Both functions are fundamental, but capacitors used inside amplifier circuits directly affect the quality of the signal, giving them a critical importance.

Within this context, the most disrupting effects of a capacitor are capacitance drift and distortion. Obviously, these are not the only sources of worries, other non-ideal characteristics may be of concern in other scenarios.

Capacitance drift is typically due to temperature change and component aging. These drifts of capacitance will mostly impact the frequency response of the circuit and, in the specific case of symmetrical circuits, their balancing.

The major problem comes from capacitance variation with the applied voltage, an effect particularly evident in high-permittivity ceramics used

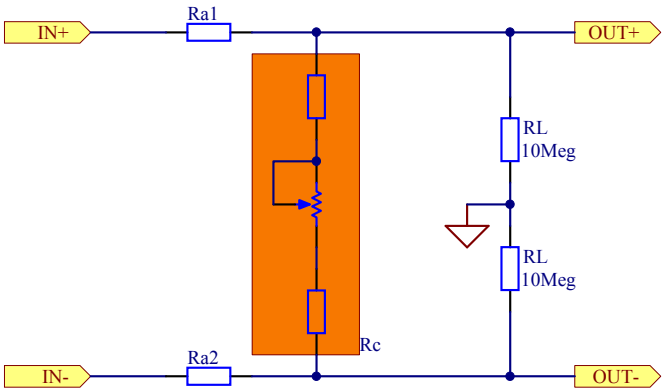


Figure 4.1: Differential attenuator circuit.

Dielectric classes are defined in the EIA standard 535.

as dielectric in small-sized chip capacitors. The best ceramics available for sensitive applications are those classified as EIA Class 1 dielectrics: the analog board was populated with $C0G$ (a.k.a. $NP0$) chip capacitors on the signal path, which represents the less-distorting ceramic of that class [7].

Other components that impacted the analog circuitry performances are treated extensively in the following sections.

4.1 ATTENUATOR

Attenuators designed for the signal conditioner are a balanced version of the common resistive voltage divider. As such, they maintain the utmost simplicity, while limiting the design issues to the trade-off between high input impedance and low thermal noise.

figure 4.1 shows the schematic of an attenuator, which includes the resistive loading of the subsequent amplifier stage. From this, the gain can be easily calculated:

$$G = \frac{2R_L \parallel R_c}{R_{a1} + R_{a2} + 2R_L \parallel R_c}$$

The loading resistance was fixed to $10\,M\Omega$ (see section §4.2), while $R_{a1} = R_{a2}$ in order to maintain the circuit balanced. Therefore, the design process of the attenuator had two degrees of freedom (R_a and R_c).

The calibrator was implemented within the center branch of the attenuator, that is the only part of the circuit that all the preset have in common. Thus, Rc is fixed across the presets (except for the small calibration trimming), while Ra changes when setting a different attenuation value.

The design constrains of this circuit were:

- Nominal gain values: $\frac{1}{20}$, $\frac{1}{10}$, $\frac{1}{5}$, $\frac{1}{2}$.
- Final accuracy obtainable by the calibrator: 0.025%.
- Electrical ratings of the calibrator (due to the digital potentiometer): maximum voltage: $\pm 15\,V$, maximum current: $\pm 2\,mA$.
- Minimum loading resistance dependent on the bucking V/I converter.

Selection of the actual values of resistance required the set up and minimization of a system of equations, whose purpose was to define the overall

Attenuation	$\frac{1}{20}$	$\frac{1}{10}$	$\frac{1}{5}$	$\frac{1}{2}$
R_a	$1.9\,M\Omega$	$900\,k\Omega$	$400\,k\Omega$	$100\,k\Omega$

Table 4.1: Resistor values of the attenuator.

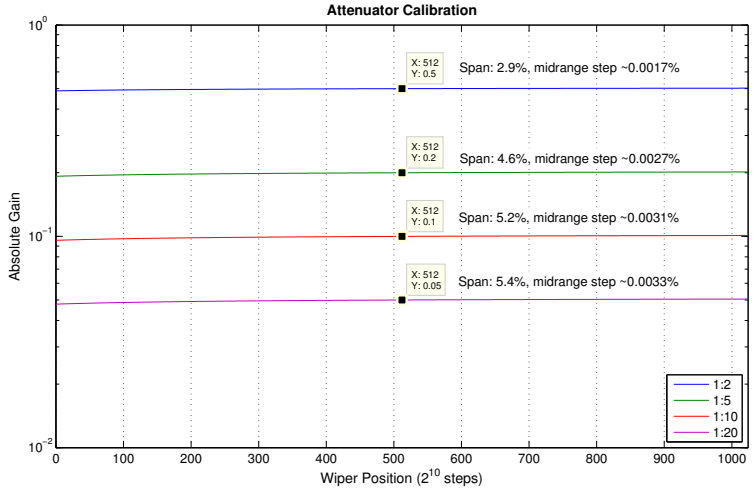


Figure 4.2: Calibration span of the attenuator.

calibration span of the attenuator. The total R_c was calculated to be $200\,k\Omega$, while the gain-specific resistor values are shown in table 4.1.

The calibration span realized with this values is shown in figure 4.2.

4.2 FULLY-DIFFERENTIAL INSTRUMENTATION AMPLIFIER

This amplifier serves two purposes in the direct channel conditioner: gain stage, when measuring small signals, and buffer in all other cases.

The configuration of this amplifier is a symmetrical variation of an instrumentation amplifier, from which it retains the main advantages, like high input impedance, high common-mode rejection and gain adjustable by changing one resistor. A common mode feedback loop was added at to further increase the common-mode rejection ratio.

The amplifiers selected for this circuit are:

- OPA2140, for its low input bias current, offset and noise.
- OPA1632, for its low distortion, noise and the high output driving current.
- LT1012, for its low voltage offset and high CMRR.

Two $10\,M\Omega$ resistors were placed between the input pins of the amplifier and ground, in order to provide a biasing current: no other connection to ground exists, since the magnetic field probes are floating sources. The input biasing current of the OPA2140 is small enough to avoid a noticeable offset.

figure 4.3 shows the circuit schematic, from which the expression of the amplifier gain is easily derived:

$$G = -\frac{R_{f2}}{R_2}\left(1 + 2\frac{R_{f1}}{R_G}\right)$$

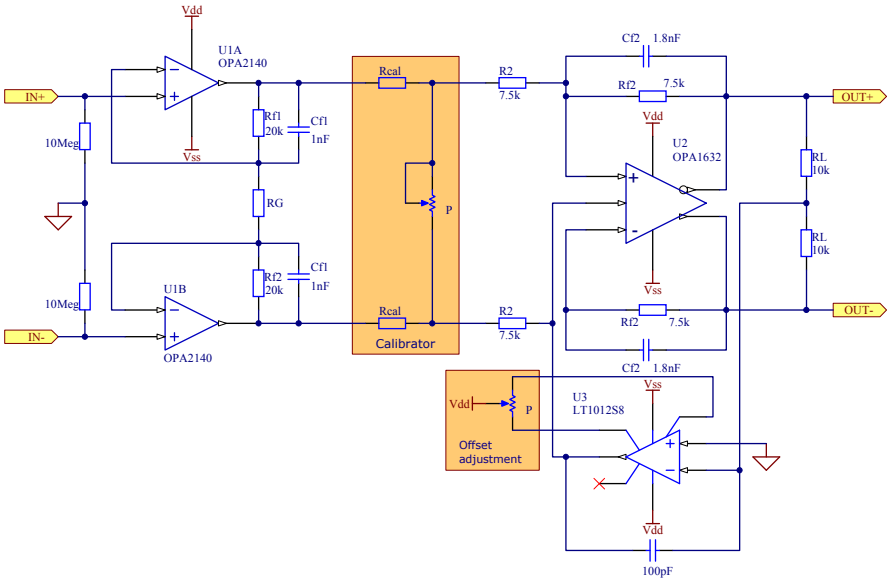


Figure 4.3: Fully-differential instrumentation amplifier circuit.

As it is clear from the previous equation, the gain may be set by changing the value of R_G alone, which is the only single resistor appearing in the formula. Gain programmability was thus attained by providing an array of resistors to select R_G from, using analog multiplexers.

The feedback capacitors at the output set the main low-frequency pole at:

$$f_{pL} = \frac{1}{2\pi \cdot R_{f2} \cdot C_{f2}} = 11.8\,kHz$$

The two other capacitors, C_{f1}, were placed to increase the gain roll-off at higher frequency to smooth an high-frequency resonance (@ $\sim 1\,MHz$) of the amplifier.

The circuit was simulated using SPICE, obtaining a total harmonic distortion of $THD = 0.05\%\,(-86\,dB)$ at unity gain with an output signal amplitude of $-1\,dBFS$ using a sine-wave input at $1\,kHz$. The input-referred noise power spectral density was 200 $\frac{nV}{\sqrt{Hz}}$.

This amplifier is calibrated by a programmable resistive divider placed between the OPA2140 and the OPA1632. This circuit has got a calibration span illustrated in figure 4.4.

In order for this kind of calibrator to work in any condition, the nominal gain value of the presets had to be increased by a small amount to ensure the the actual presets of the final device would never fall short of the target gain value: a voltage divider can only reduce the signal amplitude.

The programmable gain presets required for this amplifier were: 1, 2, 5, 10, 20, 50, 100, 200, 500 and 1000. The corresponding values of R_G, calculated taking into account the calibrator, are listed in table 4.2.

4.3 BUCKING VOLTAGE-TO-CURRENT CONVERTER

The voltage-to-current circuit used at the beginning of the bucking chain is the balanced version of a T-shaped resistor network (figure 4.5), with the differential current on the rightmost branch being the current output. In the figure, the resistors forming the output branch are seen connected

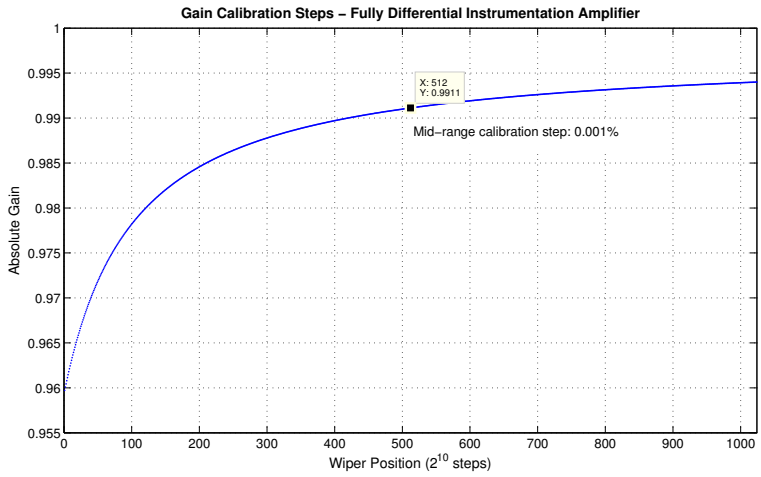


Figure 4.4: Calibration span of the fully-differential instrumentation amplifier.

Gain	1	2	5	10	20
R_G	∞	$39150\,\Omega$	$9870\,\Omega$	$4392\,\Omega$	$2081\,\Omega$

Gain	50	100	200	500	1000
R_G	$806\,\Omega$	$398\,\Omega$	$197.6\,\Omega$	$77.17\,\Omega$	$37.57\,\Omega$

Table 4.2: Resistor values of the fully-differential instrumentation amplifier.

together: that connection is due to a virtual short-circuit at the inputs of the the following amplifier stage (see section §4.4). All the voltage-to-current converters present on the board (ten, one for each channel) are physically connected together at the common node of the output branch, which means that, as long as the subsequent amplifier provides a good short-circuit, they will remain transparent to each other.

The conversion gain of the circuit in figure 4.5 is given by:

$$G = \frac{R_c \parallel 2R_b}{2R_a + R_c \parallel 2R_b} \cdot \frac{1}{2R_b} \left[\frac{A}{V}\right]$$

Because of the trade-off between input impedance and signal strength previously outlined on page xxiii, the conversion gain (transconductance) was defined so that the output current would, in any case, be around $10^{-6}\,A$. Therefore, four gain presets were provided, one for each decade of the signal conditioner input range; the transconductance was calculated starting from the maximum expected signal ($\pm 200\,V$):

- High voltage: $\pm 200\,V \rightarrow \pm 20\,V$ input, transconductance $5^{-9}\,\frac{A}{V}$.
- Medium Voltage: $\pm 20\,V \rightarrow \pm 2\,V$ input, transconductance $5^{-8}\,\frac{A}{V}$.
- Low Voltage: $\pm 2\,V \rightarrow \pm 0.2\,V$ input, transconductance $5^{-7}\,\frac{A}{V}$.
- Tiny Voltage: $\pm 0.2\,V \rightarrow \pm 0.01\,V$ input, transconductance $5^{-6}\,\frac{A}{V}$.

The resistor values used to provide these gain settings are listed in table 4.3.

Aside from these presets, the transconductance was made manually adjustable by 5% (95% $\leftrightarrow$ 100% of the nominal value) by adding a digital potentiometer to the common resistance R_c. This feature was implemented

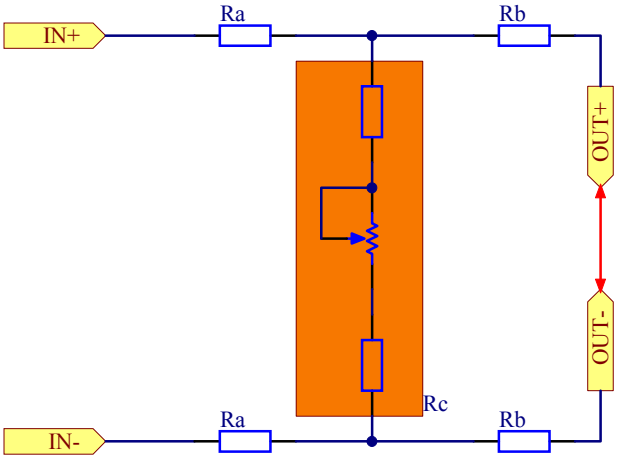


Figure 4.5: Voltage-to-current converter circuit.

Voltage range	$\pm 200\,V \rightarrow \pm 20\,V$	$\pm 20\,V \rightarrow \pm 2\,V$	$\pm 2\,V \rightarrow \pm 0.2\,V$	$\pm 0.2\,V \rightarrow \pm 0.01\,V$
R_a	$3.6\,M\Omega$	$348\,k\Omega$	$33.6\,k\Omega$	$4.53\,k\Omega$
R_b	$500\,k\Omega$	$250\,k\Omega$	$50\,k\Omega$	$5\,k\Omega$
R_c	$585\,k\Omega$	$411\,k\Omega$	$180.4\,k\Omega$	$70.2\,k\Omega$

Table 4.3: Resistor values of the voltage-to-current converter.

to allow the operators to trim the channel outputs and thus obtain a high bucking ratio.

4.4 BUCKING TRANS-IMPEDANCE AMPLIFIER

The amplifier used for summing the bucking current is a fully differential current-input, differential voltage-output stage, whose duties are to provide a short-circuit summing point for the bucking currents and then convert the resulting signal to a voltage.

The circuit was inspired by the well-known trans-impedance preamplifier, an operational amplifier circuit widely used to perform short-circuit measurements on current-output sensors (such as photodiodes). That design was extended to provide differential input/output capabilities.

figure 4.6 shows the schematic of this amplifier. A simple voltage gain stage (shown only as a load) follows at the output.

The conversion gain of this circuit is:

$$G = -2R_f \left[\frac{V}{A}\right]$$

A single gain value was provided for the trans-impedance amplifier: $G = -2 \cdot 10^4 \frac{V}{A}$ with $R_f = 10\,k\Omega$. The subsequent voltage amplifier was used for additional amplification, if required.

The bandwidth of the trans-impedance amplifier is limited by the pole at:

$$f_{pL} = \frac{1}{2\pi \cdot R_f \cdot C_f} = 10.6\,kHz$$

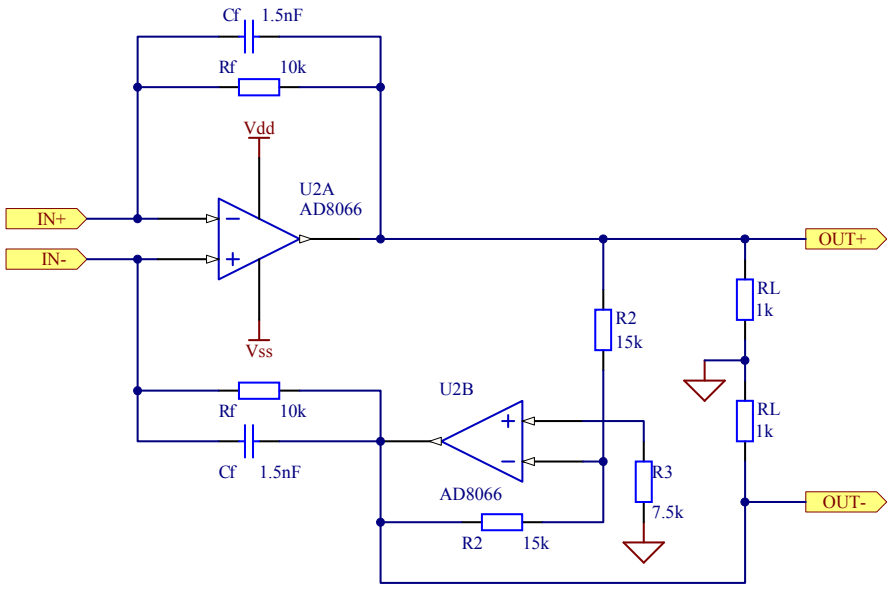


Figure 4.6: Trans-impedance amplifier circuit.

The linearity of this amplifier was estimated using SPICE, obtaining a $THD = 0.0011\%\,(-99\,dB)$ with an output signal amplitude of $-1\,dBFS$ using a sine-wave input at $1\,kHz$. It must be noted that this amplifier will never operate with such large signals, but it will be the following stage to degrade the total linearity.

The total input-referred noise, including the voltage-to-current converter, was in the range of 200 $\frac{nV}{\sqrt{Hz}}$.

4.5 PRELIMINARY PROTOTYPING AND TESTING

Prototypes of the amplifiers were built to asses the general functionality of the circuit, in particular to rule out instability and saturation problems.

Unfortunately, the precision components required for the circuits were not available, so that the prototypes ended up having performances not comparable with the project predictions.

The prototypes of the fully-differential instrumentation amplifier and the trans-impedance amplifier were fully functional, although their performances were limited by the unbalances caused by low-end resistors used.

Distortion measurements could not be done due to the lack of an high-purity voltage source and of a sharp low-pass filter. Testing was limited to checking that the amplifiers would not increase the harmonic components of a sine-wave produced by a common digital signal generator, with optimum results.

5 SIGNAL SWITCHING AND TUNING

Besides programmable gain, the flexibility of the signal conditioner comes from the possibility to thoroughly set up the analog circuitry. The actual path of the measured signal, from input to output, can be remotely configured for every channel with the following options:

- Completely bypass all the signal conditioning circuits.
- Activate/bypass the input attenuator.
- Attach/detach the channel to the bucking circuitry.

Since both signal path and gain selection are performed by operating some sort of switches, it was of utmost importance to carefully chose this components so that they would not nullify the effort put in the circuit design.

The two main classes of switches usable for analog signals are electromechanical relays (instrumentation-grade reed relays) and semiconductor switches (also known as analog multiplexers, when several are integrated together). Both have their pros and cons, but the properties that make them useful in different situations are:

A reed switch is an electrical switch made by ferromagnetic contacts enclosed in a sealed package. The switch engages when exposed to a magnetic field. Several reed switches can be integrated inside a reed relay and operated with the same coil.

- Relays are bulkier than semiconductor switches.
- Relays can handle high voltage signals, while integrated switches are typically limited to a fraction of the power supply rails.
- The on-resistance of relays is low and predictable, while semiconductor switches behave non-linearly over the signal voltage range. The same is conversely true for the isolation resistance: relays show negligible leakage currents while in the open state.
- Relays require higher power to operate than semiconductor switches. With non-latching relays, a significant continuous power consumption is required to hold the engaged status. Specific driving circuits are usually required.
- Because of the previous, relays will heat up during operation. This, in turn, amplifies the effects of their intrinsic thermal EMF. Such a problem doesn't exist with semiconductors.
- Relays have switching times many orders of magnitude higher than semiconductor switches.
- Relay switching transients are a potential source of EMC problems, when the issue is not properly addressed. Integrated switches are unlikely to cause disruptive EMI emissions.
- Instrumentation-grade relays are extremely expensive with respect to semiconductor switches.

From the previous list it stands to reason that some parts of the signal conditioner called for the adoption of relays, for instance where high-voltage signals might be present, while others were not going to be much impaired

by the use of analog multiplexers, like high-impedance nodes operating at low voltage.

Moreover, the unconstrained use of relays would have led to unreasonably large printed circuit boards and massive power consumption. The adoption of some semiconductor switches in place of relays was thus decided out of necessity.

A few manufacturers produce relays with truly outstanding performances, in term of signal quality. Among those, Coto Technology sells instrumentation-grade relays that were perfectly fit for the signal conditioner analog circuitry. Another company that manufactures good relays is Meder Electronic with its low-profile SMT relays, useful where high levels of integration are required.

On the other hand, semiconductor switches and analog multiplexer are available from the majority of semiconductor manufacturers, with characteristics tailored to cover a wide range of applications.

5.1 SIGNAL PATH SELECTION

The possible signal paths provided for each channel are, as shown in figure 2.2:

- Complete bypassing of the circuitry.
- Bypassing of the attenuator.
- Bucking.

The selection of signal paths had forcibly to be done with relays because of the high voltage range of the measurement signals. Coto technology manufactures reed relays with DPST (Double-Pole Single-Throw) contacts configuration that represent the ideal choice for differential signal switching: the 3600 series.

Model 3602 is a low-thermal EMF relay rated up to $250\,V$ on each contact (the maximum single-ended signal voltage is $150\,V$), with fast sub-millisecond operation and low contact resistance.

The magnetic field probes expected to be used with this signal conditioner are of inductive nature, which means that an abrupt load disconnection will likely result in a voltage spike at their terminals. This condition may happen every time the relays are switched to change the signal conditioner configuration, possibly causing arcing between the relay contacts and thus severely degrading their performances.

In order to prevent a voltage buildup during reconfiguration, each channel was equipped with a relay that shorts the source, thus permitting a safe switching procedure.

5.2 GAIN SWITCHING

Both amplifiers and attenuators have programmable gain presets activated by switches. The kind of switch used in each circuit was decided by predicting the final operating conditions of that particular section.

5.2.1 *Attenuator switches*

Attenuators are directly exposed to the full range of the input signals, thus forcing the adoption of relays over semiconductor switches.

Considering the high values of resistance appearing in these parts of the circuitry and the range of the expected signals, using the expensive Coto relays was deemed unnecessary. Instead, the choice fell on the SMT reed relays manufactured by Meder, model CRR.

Despite their small form-factor, these relays can withstand high-voltages and have outstanding performances, with the only drawback being the lack of a double-pole double-throw version: two different relays had to be used together to switch each attenuation preset.

It must be pointed out that the procedure of switching the attenuator configuration is affected by the same problem of voltage spiking highlighted in section §5.1, therefore requiring the adoption of the shorting relay.

5.2.2 *Amplifier switches*

Switching of the amplifier gain is performed by selecting the proper resistor out of a set of 10.

The nodes to which these resistors were connected are internal to the amplifier and operate within fixed bounds: in no case their voltage can exceed the supply rails and the loading seen on each branch is stable and high. For this reason, gain switching was designed using semiconductor switches, rather than relays. Moreover, the adoption of relays was discouraged by the amount of switches required.

The MAX4590 analog switches by Maxim were selected for their excellent linearity and low leakage current. The low on-resistance of $1.25\,\Omega$ maximum was negligible with respect to the resistor values connected to these switches, except for the highest gain settings (500 and 1000), that required the adoption of low resistor values ($< 100\,\Omega$). In this case several switches were put in parallel to reduce their influence.

5.2.3 *Bucking switches*

The bucking current-to-voltage converters are directly connected to the probes on one side and output tiny current signals on the other. Therefore, high-voltage switches were required at the inputs and high performance switches at the output.

Coto 3602 relays were used for switching the inputs, while Meder CRR05-1A were used at the outputs. This choice was made mainly for layout considerations, since both relays were suited for both ends of the circuit.

Again, these relays must be operated together with the input-shorting relay to prevent voltage spikes and arcing at the contacts.

5.2.4 *Relay driver circuit*

Operating a relay coil directly from the output pin of a logic integrated circuit is usually not a good idea, due to the limited load driving capabilities of most logic families. The relays used int this design require driving currents in of $13 \sim 29\,mA$ at the nominal coil voltage of $5\,V$, which is not a light burden for digital logic, considering also that some settings require the simultaneous operation of two relays.

A second issue that discouraged the direct connection of logic chips to the relays was the length of the electrical traces, and thus the increased losses caused by stray resistance.

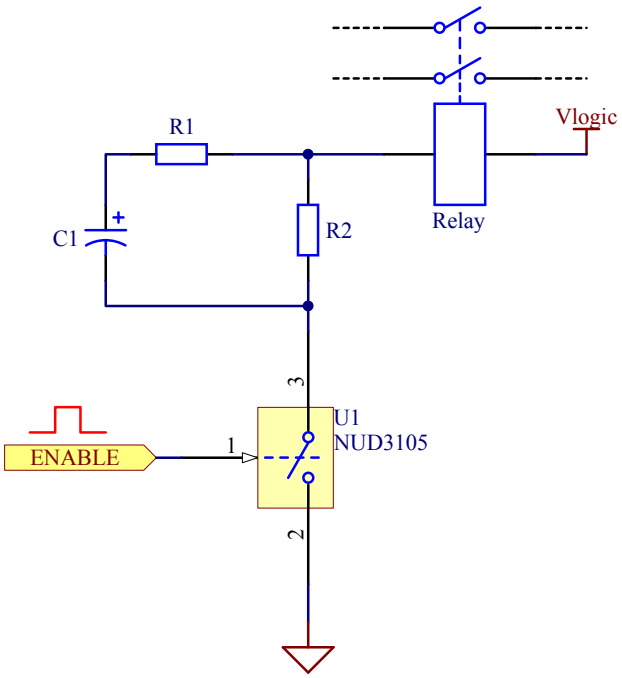


Figure 5.1: Relay driver circuit.

Due to the stated reasons, the implementation of proper relay drivers was mandatory.

Another issue that had to be addressed regarded the expected power consumption of the relays. With a total of ten channels, the number of relays present in the analog circuitry is 280: when considering the maximum amount of relays that could be simultaneously engaged (110 under normal measuring conditions), the gross power consumption would be of $\sim 12\,W$. Although this may seem a small amount, one has to observe that other sources of heat are present within the signal conditioner, and that thermal drift effects are detrimental in precision analog electronic circuits. A solution had to be sought to reduce relays consumption as much as possible.

The relays adopted in the signal conditioner have switching characteristics rated for actuation with a nominal coil voltage of $5\,V$. However, relays are guaranteed not disengage until the applied control signal falls down a different level, called the pull-in voltage.

A way to reduce the power consumption, without sacrificing the switching performances, is to initially operate the coil at the nominal voltage, then drop the signal down to the pull-in voltage. The initial $5\,V$ signal has to be kept only during the brief switching period ($< 1\,ms$).

A very simple circuit (figure 5.1) was designed to drive the relays according to the solution just explained. This circuit uses an RC network to maintain a full-scale operating signal for the required amount of time, after which the voltage drops down to the minimum safe value.

Different versions of the relay driver were made for the two models of relays, the values are listed in table 5.1.

	Coto 3602	Meder CRR05-1A
R_1	$22\,\Omega$	$22\,\Omega$
C_1	$33\,\mu F$	$22\,\mu F$
R_2	$1.2\,k\Omega$	$430\,\Omega$

Table 5.1: Component values for the relay drivers.

5.3 CALIBRATION CIRCUITRY

Three calibrators have been implemented within each signal conditioner channel. Two are used to calibrate the gain: one for the amplifier and the other for the attenuator. The third is used to trim the output DC offset. Circuits conceptually similar to the calibrators were placed in the bucking current-to-voltage converters, they were needed to permit manual fine-tuning of the bucking signals.

All these calibration circuits had to be remote controllable, a requirement that forced the adoption of digital potentiometer instead of mechanical ones.

Digital potentiometers have got a series of valuable advantages over mechanical trimmers that go beyond the simple programmability: they are more stable in the long run and they tend to be less affected by adverse environmental conditions, except for temperature. Unfortunately, due to their construction (they are manufactured with standard semiconductor IC processes), digital potentiometers share the non-negligible temperature coefficient of semiconductor resistors. To contain the effect of thermal drifts, the calibration circuits were designed to be less sensitive to the absolute value of potentiometers, this, in turn, required the adoption of high resolution potentiometers to obtain a calibration span suitable for successfully trimming all the gain settings.

The potentiometers selected for this design are those belonging to the AD5293 series, manufactured by Analog Devices. These potentiometers provide 10 bits of resolutions over a resistance of $100\,k\Omega$, $50\,k\Omega$ and $20\,k\Omega$, and are able to operate in "resistor performance" mode with 1% tolerance on the absolute value of resistance.

6 ANALOG BOARD CONTROL AND INTERFACING

A relevant part of the signal conditioner board was the digital circuitry that had to be implemented to allow controlling of all the features.

This digital part had to remain quiet during the measurements to avoid feeding noise to the analog channels. It was thus decided to avoid using any kind of clock generator, but rather rely on an external processing unit.

The solution pushed for the adoption of devices with combinational logic functioning, but also equipped with stateful communication interfaces. It was, indeed, impractical to provide the number of direct electrical links required to set up all the signal conditioner features using only combinational logic.

A number of digital components exist in which an internal register contains all the logic inputs (the status word) sufficient for operation. This status word may be accessed and written by using a serial communication protocol, the SPI, that carries a clocking signal temporarily limited to this precise function: the clock comes from the bus master and ceases as soon as the device has been programmed.

These components were ideal for this project, since a small clocking interference happening during configuration would not become a problem. The signal conditioner in no case is expected to provide meaningful outputs when changing its internal set up.

6.1 THE SPI BUS

The Serial Peripheral Interface is a 4-wire synchronous serial bus capable of full-duplex communication that supports single-master, multiple-slave topologies. The bus itself has never been standardized (it is a *de facto* standard) and different devices typically use different protocol rules.

The four wires used in the SPI bus are:

SCLK The serial clock provided by the master.

MOSI Master-Out Slave-In, which carries the data from master to slave.

MISO Master-In Slave-Out, which carries the data from slave to master.

SS Slave Select (also Chip Select), used by the master to start / end a transmission. Usually active-low.

The SPI bus operation is conceptually very simple. The master uses the proper chip select line to select a target slave device, then starts transmitting a clock along with serial data synchronous to it (the number of clock cycles equals the number of data bits transmitted). If the slave device supports an output channel, it will transmit data back to the master synchronized with the same clock. The transmitted data (word) is received by loading a shift register and then, upon release of the chip select line, the content of this register is processed by the receiving device.

SPI allows daisy-chaining, but support of this wiring scheme ultimately depends on the capabilities of the slave devices. It's mandatory to asses the specific characteristics of each slave before building a daisy-chain.

The main features of SPI, along with the common variants, are listed below:

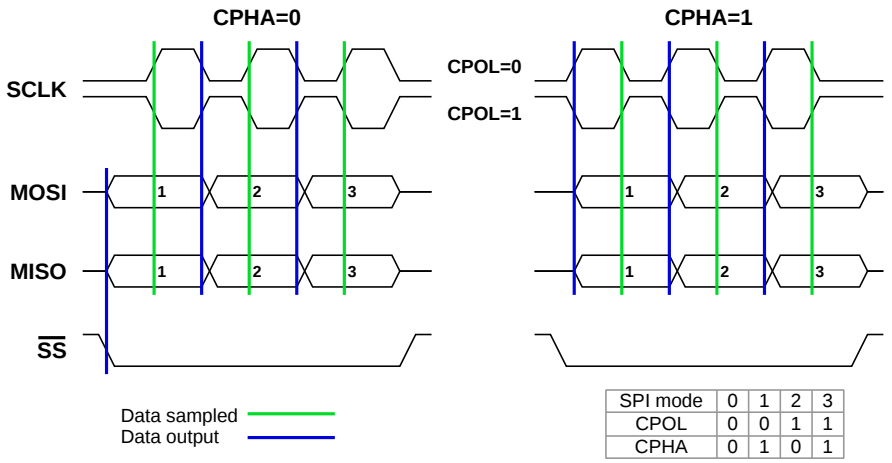


Figure 6.1: Timing diagram of the four SPI modes.

- Clock frequency (same as bit-rate): up to 70 MHz.
- Word size: usually 8 bits, may be any length.
- 4 possible clocking modes depending on polarity and phase (CPOL/CPHA)
- No protocol overhead in transmitted data.
- Transmission uses CMOS logic levels.

figure 6.1 illustrates the four possible clocking modes of the SPI bus. Complete support of these modes is uncommon in SPI devices.

6.2 General purpose output ICs

Except for those devices that come with an integrated SPI interface, such as digital potentiometers, setting up the signal conditioner requires the activation/deactivation of switches and relays by changing their logic inputs. The simplest way to perform this task was to use General Purpose Output (GPO) integrated circuits, also known as "output expanders". These devices have got a number of logic ports whose output level can be programmed (and read back) via SPI.

The following GPO chips were selected:

- Maxim MAX7301, in both its 20 and 28 ports versions.
- Microchip MCP23S08, having 8 outputs.

Whenever the embedded controller needs to change the gain settings, it simply has to overwrite the configuration register of the GPO chips.

6.3 SPI buffering and distribution

The large amounts of SPI slaves present on the signal conditioner boards prevented the direct connection of those devices to the embedded controller: the number of chip select lines required would have been too high (at least 3 per channel), the fan-out of the master excessive and the growing number of traces would have negatively impacted the PCB routing process.

A programmable SPI buffer was devised to reduce the complexity of the digital bus interconnections and the loading of the embedded controller. This device was designed as a hub to which all the SPI slaves are connected (except for the interrupt generators) and accessed only on-demand by the master.

Programmability of the SPI buffer output device was attained by making it a SPI slave. The master can set up the buffer by transmitting a word 6 bits long, that contains the encoded configuration requested. Upon termination of communication, the internal logic of the buffer decodes the data and virtually connects the proper target device to its input bus: from this point on, the SPI buffer becomes transparent to the master.

The SPI buffer was implemented inside a Complex Programmable Logic Device (CPLD) model XC95144 by Xilinx, the complete VHDL source code is transcribed in appendix C. This design was successfully synthesized and proof of concept verification was performed on a physical testing board.

Very-High-Speed Integrated Circuits Hardware Description Language, a language commonly used for describing logic systems. VHDL code can be processed by a synthesizer to obtain a physical implementation, which can be deployed into a programmable logic device.

The introduction of a buffer had two negative side effects:

- The added overhead of having to program the buffer.
- The limitation of clocking speed caused by the increased delay.

The XC95144 CPLD adopted in this design has a maximum propagation delay time, pin-to-pin, of $10\,ns$. In an SPI full-duplex communication, this delay time is doubled for the MISO data. Since the MISO signal needs to be valid within half period of the master serial clock, without considering any other source of delay, the buffer limits the maximum clocking speed to $25\,MHz$.

6.4 BOARD DIAGNOSTICS

Three classes of diagnostic circuits were implemented within the analog part:

- Detection of saturation at the outputs.

  Here "saturation" is not referred to the actual saturation of the output stage of the signal conditioner, but rather a condition when the output signals exceeds the input range of the subsequent analog-to-digital converter, that is $\pm 10\,V$ (or $\pm 5\,V$ single-ended, since the outputs are balanced). Indeed, even a signal double the rated output voltage is still well within the signal conditioner rails.
  Analog comparators were used at every output (including the bucking channel) to monitor the signal swing.

- Detection of input over-voltage conditions.

  The clipping circuits placed for protection at the inputs of the fully-differential instrumentation amplifiers trigger an interrupt whenever the input signals exceed the rails. Sensing of this over-voltage was done by detecting the flow of current in the protection diodes.
  A total of 10 over-voltage detectors were placed on the analog part, one for channel.

- Control of the power supply voltage.

  The performances of the integrated circuits adopted in the analog circuitry, mainly amplifiers and potentiometers, are strictly dependent on the voltage supply level and its stability over time. A change in the output of the $\pm 15\,V$ power supply will affect the behavior of the signal

Bit	Fault	Bit	Fault	Bit	Fault
47	*Unused*	31	Bucking output saturation	15	*Unused*
46	*Unused*	30	*Unused*	14	*Unused*
45	*Unused*	29	Channel 10 output saturation	13	Channel 5 output saturation
44	*Unused*	28	Channel 10 input over-voltage	12	Channel 5 input over-voltage
43	*Unused*	27	*Unused*	11	*Unused*
42	*Unused*	26	Channel 9 output saturation	10	Channel 4 output saturation
41	*Unused*	25	Channel 9 input over-voltage	9	Channel 4 input over-voltage
40	*Unused*	24	*Unused*	8	*Unused*
39	*Unused*	23	Channel 8 output saturation	7	Channel 3 output saturation
38	*Unused*	22	Channel 8 input over-voltage	6	Channel 3 input over-voltage
37	*Unused*	21	*Unused*	5	*Unused*
36	*Unused*	20	Channel 7 output saturation	4	Channel 2 output saturation
35	Positive supply over-voltage	19	Channel 7 input over-voltage	3	Channel 2 input over-voltage
34	Negative supply over-voltage	18	*Unused*	2	*Unused*
33	Positive supply under-voltage	17	Channel 6 output saturation	1	Channel 1 output saturation
32	Negative supply under-voltage	16	Channel 6 input over-voltage	0	Channel 1 input over-voltage

Table 6.1: Interrupt status word description.

conditioner.
The analog part was equipped with two voltage monitors (MC34161 from ON Semiconductor), which are used as voltage window detectors for both supply rails. Their tripping points are $\pm 14\,V$ for under-voltage detection and $\pm 16\,V$ for over-voltage detection.

6.5 HARDWARE INTERRUPT HANDLING

The diagnostic circuits signal the occurrence of a faulty condition by asserting a logic output. All these signals were routed to a series of interrupt generators ICs, whose duty is to catch these assertions and notify the embedded controller.

A single hardware interrupt line connects the analog part to the embedded controller. When this line is brought low, the embedded controller starts an interrupt service routine that queries the interrupt generators for their status via SPI. The status word thus read permits to know exactly which diagnostic circuit tripped, table 6.1 lists the meaning of each status bit. The interrupt is automatically cleared when reading the status word.

The PCA9703 integrated circuit (manufactured by NXP), a device with 16 input ports, was selected as hardware interrupt generator. Due to the amount of fault signals present, three such devices were required for simultaneous monitoring of all the diagnostic outputs. These ICs were organized in a SPI daisy-chain and their interrupt output pins were connected in wired-or (thanks to the open-collector outputs).

The SPI bus to which the interrupt generators were connected was not fed-through the SPI buffer for increased ease of access and simplification of the interrupt service routines.

All the wires connecting the analog part to the embedded controller were provided, for safety reasons, with galvanic isolation. This was accomplished by using a series of high-speed digital isolators mounted on a peripheral zone of the analog PCB.

The isolators had to respect some requirements in order to be able to transmit reliably fast SPI signals. A series of high-performance digital isolators manufactured by Analog Devices, the ADuM 3301, with their $2.5\,kV_{RMS}$ input-output isolation, were found to be well suited for the task.

Isolation rating of this component was assessed as per UL standard 1577.

The ADuM 3301 features 3 isolated channels (2 in one direction and 1 in the other) with a maximum propagation delay time, input-to-output, of $32\,ns$. Each channel has a guaranteed propagation delay matching of less than $2\,ns$ to the others. The maximum data rate is $90\,Mbps$.

A total of three isolators were needed to connect all the required input/output lines.

Obviously, the introduction of an isolator in the SPI bus will limit its speed. Using the previous data along with the delay figures provided in section §6.3, it is possible to estimate the theoretical clocking limit of the SPI bus that assures a working full-duplex communication.

The total delay between the MISO signal and the SCLK at the master's side will be:

$$T_{delay} = 32\,ns + 10\,ns + 10\,ns + 32\,ns = 84\,ns$$

T_{delay} must be smaller than half the serial clock period, which then has to be slower than $6\,MHz$. This result does not keep into account eventual delays of the SPI slaves.

7 ANALOG BOARDS PHYSICAL DESIGN

The printed circuit board design process involved the physical organization of the components and the routing of the tracks. This lengthy process was performed with the Altium Designer CAD/CAM program suite, which helped in producing a final layout that respected the proper electrical and design rules.

Most of the routing was done by hand but, fortunately, the presence of ten identical channels allowed to replicate the majority of the circuits, reducing the actual design effort.

7.1 DESIGN CONSTRAINTS

The PCBs had to fit within a 19-inch rack module, a kind of enclosure that has got an usable width of 17″ (43.18 cm). Therefore, the PCB width was limited to 16.8″ (42.67 cm) to allow some clearance between the enclosure walls and the board.

Rack units are based on the EIA standard 310.

On the other hand, the depth of a rack module may vary: depths of 20″ (50.8 cm) are common for rack cabinets. The final board depth was thus defined at the end of the routing.

Besides the space constraints, some components had specific board placement requirements.

The input signal connectors had to be positioned in line on the side of the board facing the front panel. This, in turn, forced all the channels to align side-by-side on the shortest side of the board. Shortly after starting the routing procedure, it was clear that the circuitry was not going to fit within only one board: the circuitry was thus split into two boards, as explained in section §7.3.

7.2 LAYOUT AND EMC CONSIDERATIONS

The PCB layer stack was designed for minimum EMI emissions and susceptibility.

The two PCB sides were initially assigned to different domains: one reserved to the analog components and the other to the digital circuits. After this subdivision, the PCB layers were assigned.

A total of eight layers were adopted for both PCBs: two layers dedicated to the analog signals fully surrounded by analog ground planes, a single analog power plane split between $+15\,V$ and $-15\,V$, a digital ground plane, a digital signal layer and a digital power plane (also used for digital tracks crossover). The layer stack is shown in figure 7.1.

Unfortunately, the printed circuit board manufacturer did not support blind and buried vias, thus reducing the actual isolation between the analog and digital domains.

An most important issue in an EMC-aware design is proper grounding. In order to avoid ground loops and ground coupling, a single-point grounding scheme was adopted for the ground planes of the PCBs.

All the ground pins of the devices present on the boards were independently connected to their relative ground planes. Moreover, to prevent ground

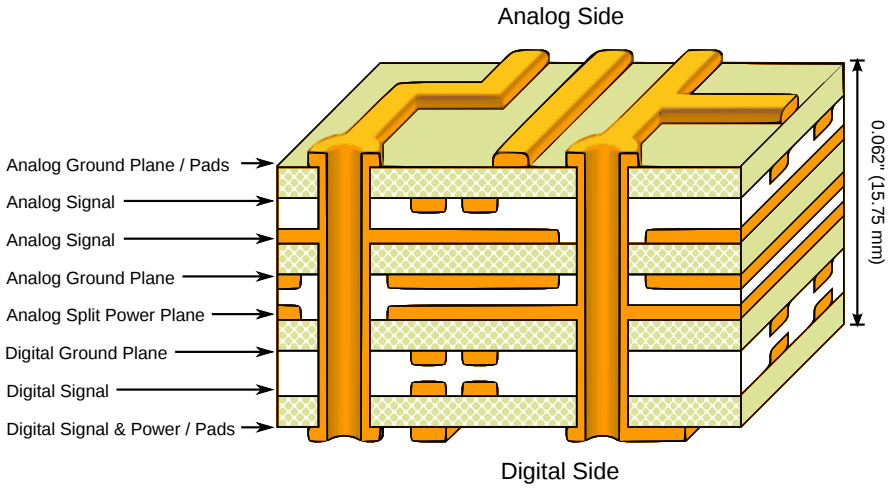


Figure 7.1: PCB layer stack.

return currents from coupling across different channels (which would have caused cross-talk), the analog ground planes were split into stripes, so that all ground currents would be forced to flow on the peripheral regions of the board.

The analog and digital grounds are not connected together on the PCBs, but rather at the power supplies. Two diodes were placed on the board to prevent the two ground potentials from drifting away in case of a ground fault.

7.3 STACKED-BOARD DESIGN AND CONNECTIONS

As previously pointed out, the extension of the circuits and the dimension of some components (relays in particular) prevented all the circuitry to be fitted within a single PCB. The design had to be split over two boards.

Since the direct channel conditioning circuits and the bucking circuits were basically independent from each other, it was decided to offload all the bucking circuitry to the second board. Anyway, this second board had to maintain some connections with the other, specifically:

- Signal sources.
- Power supply.
- Digital control lines.

In order to make these connections without using a large amount of wires, the boards were designed to be stacked using board-to-board connectors.

Sabritec manufactures two types of connectors that were well suited for this application. The QMS/QFS board connector pair provided 104 high-speed contacts used for digital signals, plus 8 power pins that were adopted for power supplies and grounding. Analog signals from the probes were brought to the bucking board by using ten IJ5/IP5 connector pairs, which are coaxial shielded connectors with controlled impedance.

The mating height of these connectors was 10 mm. Because of the Coto relay height (12 mm), the analog component sides of the two boards had to be placed facing outwards from the stack, while the digital sides faced inwards.

This also simplified the routing of the digital tracks for the QMS/QFS pins, that are surface mount connectors.

The PCBs needed to have several connectors for interfacing other parts of the signal conditioner and the external apparatuses: the embedded controller, the power supplies, the magnetic field probes and the ADC. The analog signal connectors were the most critical.

Having to attach a differential source, the choice was oriented towards twinax connectors from the beginning. Series-E by Lemo includes a PCB-mounted twinax connector that fitted the requirements, the EXG.0B.302.

Twinax, or Twin-Axial connectors, are similar to coaxial connectors but have two cores instead of one, surrounded by a shield.

At the time of writing this thesis, the output connectors were still to be decided. Therefore, generic miniature SMA twinax connectors were placed on the boards for internal use (that is, to attach the final output connector once it is chosen), these connectors are manufactured by Sabritec.

The digital isolators and the embedded controller bus connector were placed on an isolated corner of the main PCB, separating the copper pours as well (ground and power planes).

7.4 PCBs fabrication and assembly guidelines

PCBs were sent to Sunstone Circuits for production. The required RS274X GERBER files were generated from the final printed circuit board layouts using the Altium integrated CAM processor, along with Excellon Drill files. The manufacturer provided a set of design rules that were used at the beginning of the PCB design process.

The final board sizes were:

- Main board: $16.8'' \times 14''$ $(42.67\,cm \times 35.56\,cm)$
- Bucking board: $16.8'' \times 9''$ $(42.67\,cm \times 22.86\,cm)$

Both PCBs were provided with aligned mounting slot and holes isolated from the ground and power planes.

A small set of guidelines were given for mounting the electronic components one the boards:

- Precision SMT components must not be soldered by hand with an iron. Their performances are only guaranteed for reflow soldering.
- Precision through-hole components may be soldered by hand only with a low-temperature iron.
- Coto relays, that are through-hole components, are to be soldered by hand at the last step, for their dimension will impair the positioning of other, smaller components.

8 DIGITAL CONTROL BOARD

The signal conditioner project required an interfacing board capable of controlling and monitoring the analog circuitry, as well as providing a network interface.

Due to the ever expanding business of embedded systems, large amounts of embedded development kits were released on the market by the major semiconductor manufacturers. In particular, the ARM architecture has become a common denominator of high-end microcontrollers and Systems-on-Chip.

Although this development kits are intended for device evaluation, and thus are not guaranteed to be suitable for any specific application, their wide diffusion ensures a constant feedback between the manufacturer and the developers. This means that evaluation kits are usually improved over time and a sound support base is always available.

Before thinking about a custom digital design, evaluation kit catalogs were searched for an embedded controller suitable for the signal conditioner.

8.1 DESIGN REQUIREMENTS

The final list of the required features is here reported:

- Ethernet 100BASE-TX interface.
- SPI and I²C bus mastering support.
- Hardware interrupt support.
- Availability of GPIO lines.
- Mass storage device support.
- Integrated display.

The contents of this list are actually very common capabilities for high-end microcontroller development kits. Therefore, the choice of an embedded controller was pointed towards the containment of superfluous features and price, as well as the limitation of size.

8.2 THE STELLARIS® LM3S8962 EVALUATION BOARD

The Luminary Micro LM3S8962 evaluation board was found to be a suitable embedded system: it respected all the requirements at a limited cost. A picture of the board is shown in figure 8.1.

This development board mounts a LM3S8962 MCU powered by an ARM Cortex-M3 processor core, clocked at 50 MHz. External connectivity is ensured by two 30-pin expansion headers that expose all the main buses. The OLED graphical backlit display can be detached from the board with limited effort.

Mass storage is provided by means of a microSD slot, while the MCU itself hosts a small flash memory of 256 kB where the firmware is stored.

Other interesting board features were put to use during the design phase:

Figure 8.1: The LM3S8962 evaluation board.

- A 32 *bit* Real Time Clock, that was used to add time stamps to the event log.
- An FTDI FT2232D USB-to-UART interface, that provides USB-to-JTAG capabilities, making it possible to program and debug the microcontroller via USB without the need of an external JTAG adapter.

The LM3S8962 evaluation kit comes with a number of different software development tools and it is fully supported by the LabVIEW for ARM module (Tier 1 device).

figure 8.2 shows a block scheme of the embedded controller and its peripheral connections.

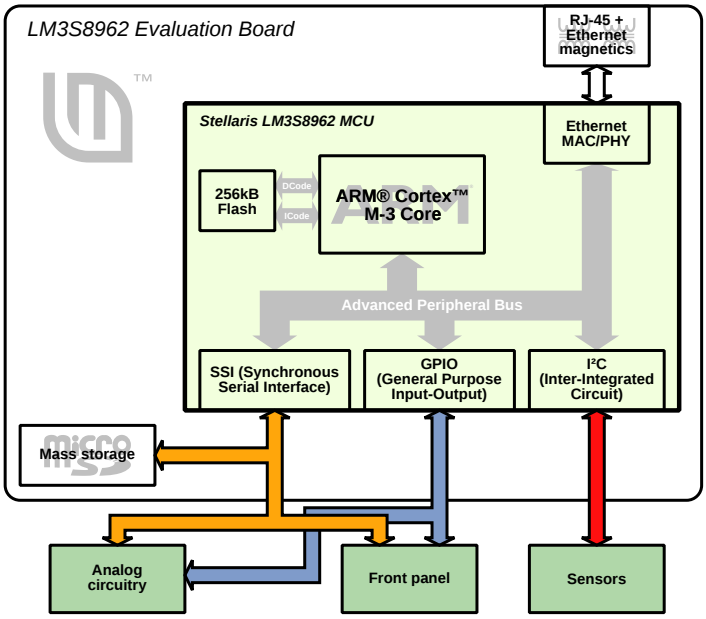


Figure 8.2: Embedded controller block scheme.

9 POWER SUPPLIES AND OTHER PERIPHERALS

The remaining components of the signal conditioner were not designed but chosen from those readily available on the market.

The selection was based not only on the base of technical requirements, but also on the expected reliability of the part. In particular, power supplies were chosen from the catalog of Acopian, a company that has proven to manufacture extremely reliable products.

9.1 ANALOG POWER SUPPLY

The analog circuitry were designed to operate from a dual $\pm 15\,V$ supply. A linear supply was selected to limit the noise introduced by the power section.

A rough power consumption estimate was calculated using the figures taken from the datasheets of the analog components, leading to a total quiescent current of:

$$I_{q-analog} = 0.24\,A$$

The current consumption of the amplifiers is going to rise during operation, so a power supply rated $1\,A$ was selected: the Acopian TD15-100 Gold Box.

9.2 DIGITAL POWER SUPPLY

The digital circuits ran on $5\,V$ supply. The power supplies intended for the embedded controller and the digital elements present on the analog boards were to be kept separated for safety reasons.

While a low-power switching regulated supply was enough for the embedded controller (which was designed to be powered by USB), a linear supply was preferred for the analog board.

As for the analog power supply, an expect power consumption was calculated basing on the component ratings. This time the calculations had to account for the relays consumption. The quiescent current absorbed when all the relays are active at the same time was:

$$I_{q-relays} = 1.92\,A$$

While the quiescent current of the digital components was:

$$I_{q-digital} = 0.2\,A$$

Together, these gave a worst-case quiescent consumption of:

$$P_q = (I_{q-relays} + I_{q-digital})5\,V = (1.92\,A + 0.2\,A)5\,V = 10.6\,W$$

This result needed to be scaled up because both digital components and relays were designed to be in their highest consumption state at the same time (during reconfiguration). For instance, considering the peak current consumption of all the 280 relays switching together, one obtains:

$$I_{p-relays} = 6.7\,A$$

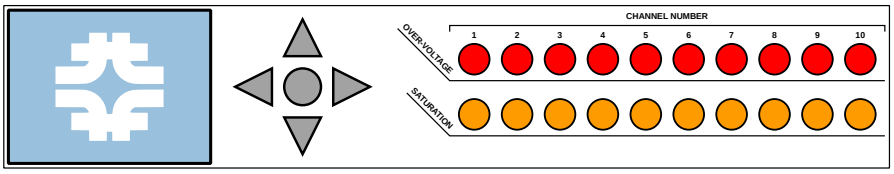


Figure 9.1: Outline of the front panel.

This figure is well beyond the real peak supply current, but allowed to settle for a power supply rated 5 A of maximum current output. The device ultimately chosen was an Acopian B5G500 Series-A Gold Box.

For what concerns the switching regulated power supply, an Acopian 5WB600 was chosen.

9.3 ADDITIONAL SENSORS

Two sensors were added to the signal conditioner design to keep track of temperature and humidity. Since they were not required to have no critical duty within the system, but only supposed to detect major environmental condition changes, cheap integrated sensors were adopted.

The Honeywell HIH6130 integrated circuit was selected, which provides both relative humidity and temperature sensors in the same package. The deivce was placed on a small printed circuit board and its I²C interface was connected to the microcontroller.

9.4 FRONT PANEL

The front panel was designed as a direct extension of the embedded controller.

The OLED display, as well as the buttons, were those provided by the Luminary evaluation board. Two series of 10 LEDs each, controlled by the remaining GPIO lines, were added to signal the occurrence of input over-voltage and output saturation conditions on each channel. A graphical representation of this front panel is shown in figure 9.1.

Part III

SOFTWARE DESIGN

10 FUNCTIONAL ROUTINES OF THE EMBEDDED CONTROLLER

All the software used for measure automation at the Magnet Test Facility has to be assembled starting from a component-based framework, the Extensible Measurement System (EMS) [4, 8]. This approach promotes code reuse and simplifies software maintenance, while easing and speeding up the development.

The firmware running on the embedded controller, however, must include a series of low level routines for setting up the signal conditioner configuration, that are new to the EMS. Therefore, they are to be implemented from scratch.

The LM3S8962 MCU uses a dedicated hardware to provide the SPI interface, so that the firmware is lifted from having to perform bit-banging for communicating with SPI slaves. The only limitation regards the presence of a single slave select output, which forces the adoption of additional GPIO lines to access all the devices connected to the controller.

Bit-banging is a common technique for executing serial communications when missing the dedicated hardware. The software directly reads and sets the input and output pins with proper synchronization.

The low level routines described in this chapter will be combined with other generic code, already developed, to obtain the final firmware. These other pieces of code will take care of maintaining a network connection to receive/process remote commands, perform logging and permit user interaction with the front panel.

The current plan is to code all the firmware using LabVIEW, to speed up the development process. Most of the reusable code written for the MTF automated measurement framework has already been ported this platform.

All the SPI configuration commands relevant to this project are reported in appendix D, divided for each digital device.

10.1 SPI BUFFER ACCESS COMMANDS

All the SPI slaves used on the analog circuitry, except for the interrupt generators, are not connected directly to the embedded controller SPI bus, but rather stand behind the SPI buffer. Every time the controller needs to access a digital device belonging to a channel, the SPI buffer must be programmed accordingly.

The slave select signal that controls the SPI buffer has got two opposite functions: when it is brought low, the buffer works as an SPI slave, allowing to program its internal status register (configuration stage); when it is high, the buffer becomes transparent and simply repeats the full-duplex communication with the selected output port.

The 6 bit status register contains encoded instructions about the target channel to access, listed in table 10.1.

The two least significant bits are used to access a specific device within the selected channel, as reported in table 10.2.

10.2 CHANNEL CONFIGURATION AND GAIN SETTING

Both the signal path and all the gain / attenuation settings (bucking included) are configured by changing the relative outputs of the GPIO port expanders.

Status word bit						
5	**4**	**3**	**2**	**1**	**0**	**Function**
0	0	0	0	X	X	Select Channel 1
0	0	0	1	X	X	Select Channel 2
0	0	1	0	X	X	Select Channel 3
0	0	1	1	X	X	Select Channel 4
0	1	0	0	X	X	Select Channel 5
0	1	0	1	X	X	Select Channel 6
0	1	1	0	X	X	Select Channel 7
0	1	1	1	X	X	Select Channel 8
1	0	0	0	X	X	Select Channel 9
1	0	0	1	X	X	Select Channel 10
1	0	1	0	X	X	Select trans-impedance amplifier
1	0	1	1	X	X	Select trans-impedance amplifier offset control
1	1	1	1	1	1	Shutdown

Table 10.1: SPI buffer status word encoding.

Status word bit						
5	**4**	**3**	**2**	**1**	**0**	**Target device**
X	X	X	X	0	0	Direct channel GPIO port expanders
X	X	X	X	0	1	Direct channel calibrators
X	X	X	X	1	0	Bucking amplitude adjustment
X	X	X	X	1	1	Bucking GPIO port expanders

Table 10.2: SPI buffer slave device selection.

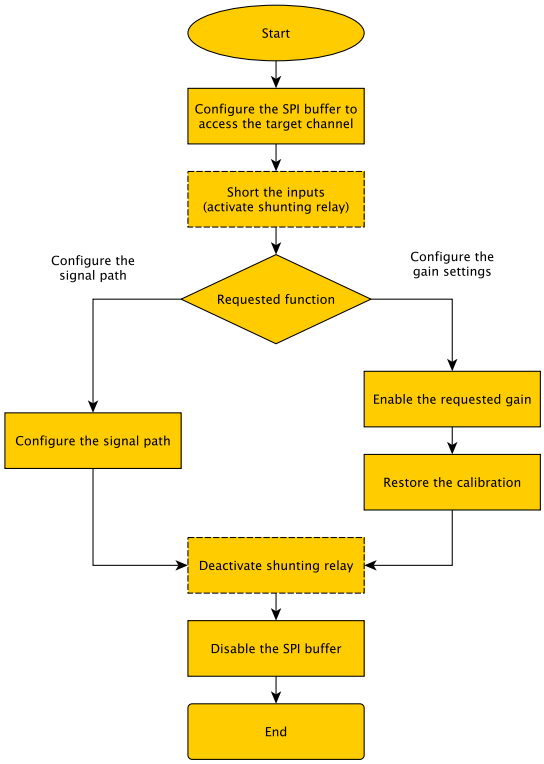


Figure 10.1: Channel configuration flow chart.

Since the firmware is keeping track of all the channel statuses (because they are to be displayed on the front panel), no reading back is really necessary, if not for diagnostic purposes.

The flow chart in figure 10.1 shows the procedure of channel configuration without read-back.

10.3 DIGITAL POTENTIOMETERS ADJUSTMENT

Step-by-step adjustment of digital potentiometers is a procedure that requires reading back the current status of the potentiometer wiper. On the other hand, when simply restoring a previously saved position, a single writing cycle is sufficient.

Moving the potentiometer wiper to find the right position is a task performed automatically during calibration and manually for adjusting the bucking signal amplitude. A simple flow chart that illustrates this procedure is shown in figure 10.2.

It must be pointed out that all the three digital potentiometers used to calibrate each channel are daisy chained.

10.4 INTERRUPT HANDLING

Interrupt handling is performed by executing an interrupt service routine that reads the status word of the interrupt managers. The hardware interrupt

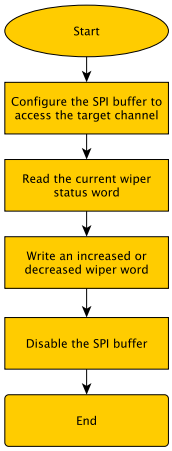


Figure 10.2: Step-by-step potentiometer adjustment flow chart.

will be ignored while the embedded controller is reconfiguring the signal conditioner, it will be caught and handled at the end of that procedure.

No special procedure is required to access the interrupt managers via SPI, since they are directly connected to the embedded controller SPI bus and have their own slave select line.

Part IV

CONCLUSION AND FUTURE DEVELOPMENTS

11 PROJECT ACHIEVEMENTS AND TRADE-OFFS

This signal conditioner design project reached the stage where the hardware was completely designed and ready for manufacturing.

A custom analog circuitry was designed from scratch, obtaining a hardware substantially compliant with the performances originally requested. The gain accuracy requirement was respected by using high resolution calibration circuits, while other circuit parameters were designed for compromise.

In particular, the low-noise performance of the signal conditioner was traded-off for an high input impedance, with the latter being a higher-priority requirement than the former. The small bandwidth requirement of the project allowed to reduce the total noise.

Due to the floating electrical configuration of the magnetic field probes intended to be used with this device, additional paths had to be provided for biasing the amplifier inputs, thus reducing their loading impedance and introducing a slight input voltage offset.

The expected signal conditioner performances, obtained by calculation and simulation, were discussed with the end users and approval was received for all the trade-offs.

Simultaneous analog bucking of the measured signals was provided using a novel current-mode approach, that prevented the various channels from loading each other.

The final circuitry was composed of ten independent signal conditioning channels, plus a bucking channel that can be configured to selectively sum all the signals. All the features of the device were made remotely programmable.

Two printed circuit boards were laid out and routed to accommodate the custom circuitry, following good electromagnetic compatibility practices aimed at the reduction of interference and cross-talk. The resulting boards were made ready for manufacturing.

A third-party single-board embedded controller was selected to interface the external instrumentation network, used in the test facility to communicate with all the automated test equipment, with the signal conditioner internal circuitry. Additional functions provided by the controller were diagnostics, logging and a front panel human interface.

Firmware design for the embedded controller was started with the definition of low-level routines and programming codes.

Proper third-party power supplies were chosen after estimating the device consumption. These supplies were selected to be stable, reliable and low in noise.

12 COMMISSIONING AND FURTHER DEVELOPMENT

When the analog boards will be ready, the firmware design will be completed using the feedback from the hardware. At that point, the last remaining manufacturing step will be putting all the parts together.

Once assembled within a suitable rack enclosure, the signal conditioner will be thoroughly tested following the procedure reported below:

1. Warm-up and bias testing.

   The device will be powered up and the quiescent power consumption will be monitored. All the amplifiers will be checked for proper biasing and the outputs will be monitored for drifts, in order to measure the warm-up time of the analog circuitry.

2. Functionality test of the embedded controller.

   The firmware of the embedded controller will be tested with the execution of remote commands. All the possible signal conditioner configurations will be tried to assess their actual functioning.
   Interrupts will be forced to check the controller response to these events.

3. Calibration testing.

   An initial full calibration will be performed. Upon successful completion, the effects of storing and restoring the calibration settings will be tested.
   Conservation of calibration will be tested when power-cycling the signal conditioner.

4. Signal conditioning test.

   The performances of each channel will be tested regarding noise, linearity and interference, using real-world signals. Long running tests (at least 2 hours) will be done to monitor the retention of these performances over time.

If all the tests are successful, the signal conditioner will be deployed to an instrumentation rack cabinet of the Magnet Test Facility, along with a stable voltage source and a precision voltmeter, which were planned to be constantly available for calibration checking and execution.

This project has room for improvement particularly on the analog circuitry. As a matter of fact, most of the performance limitations and forced tradeoffs were caused by the characteristics of the commercially available active components. It is expected that, with the current pace of analog integrated circuits improvement, better components will be available in the near future.

The same goes true for digital potentiometers and semiconductor switches.

If necessary, a cooling system might be added to stabilize the device internal temperature, this will limit thermal drifts related to active analog components (passive components were already chosen to be practically insensitive to temperature variations).

On the digital side, the entire logic architecture can be rebuilt using programmable logic devices instead of a large number of generic integrated

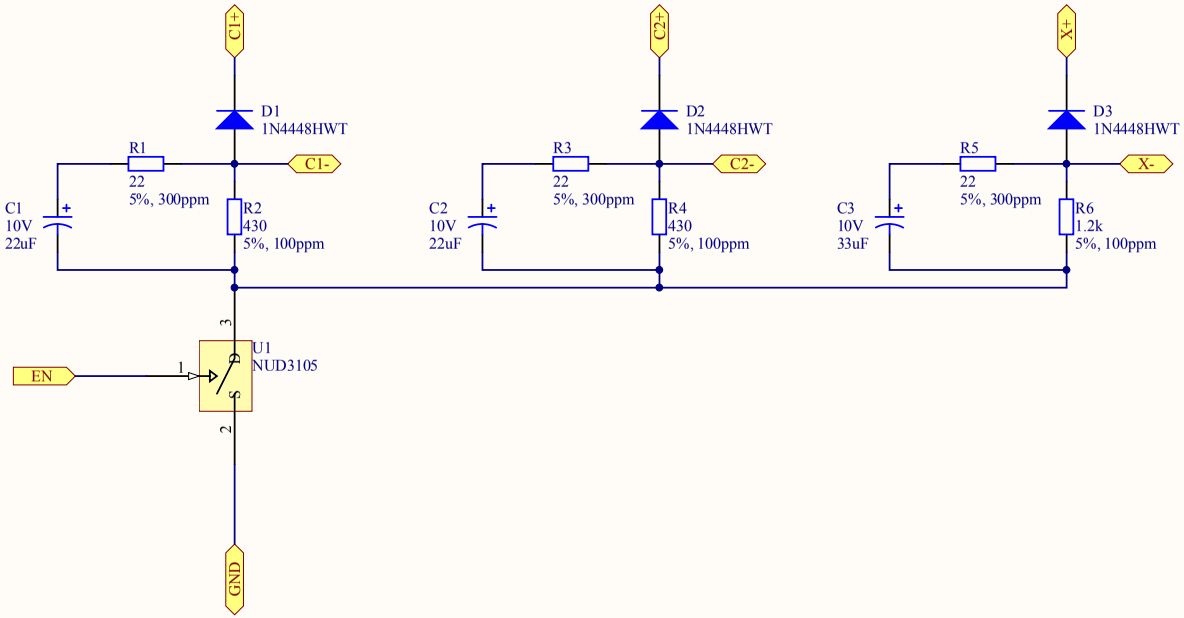
circuits, which will simplify the whole digital part. This will require the development of a potentially big specific hardware code.

Part V

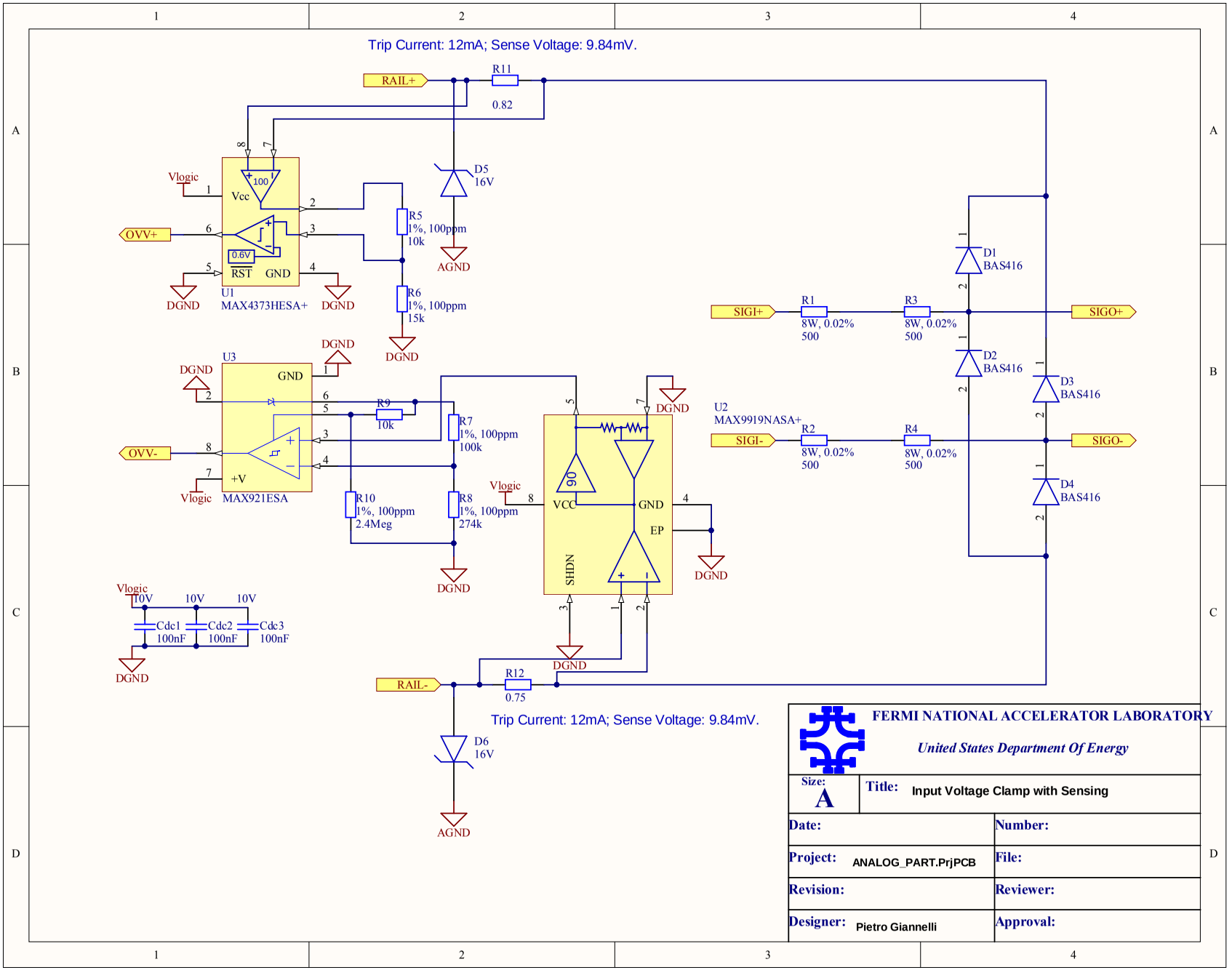
APPENDIX

A

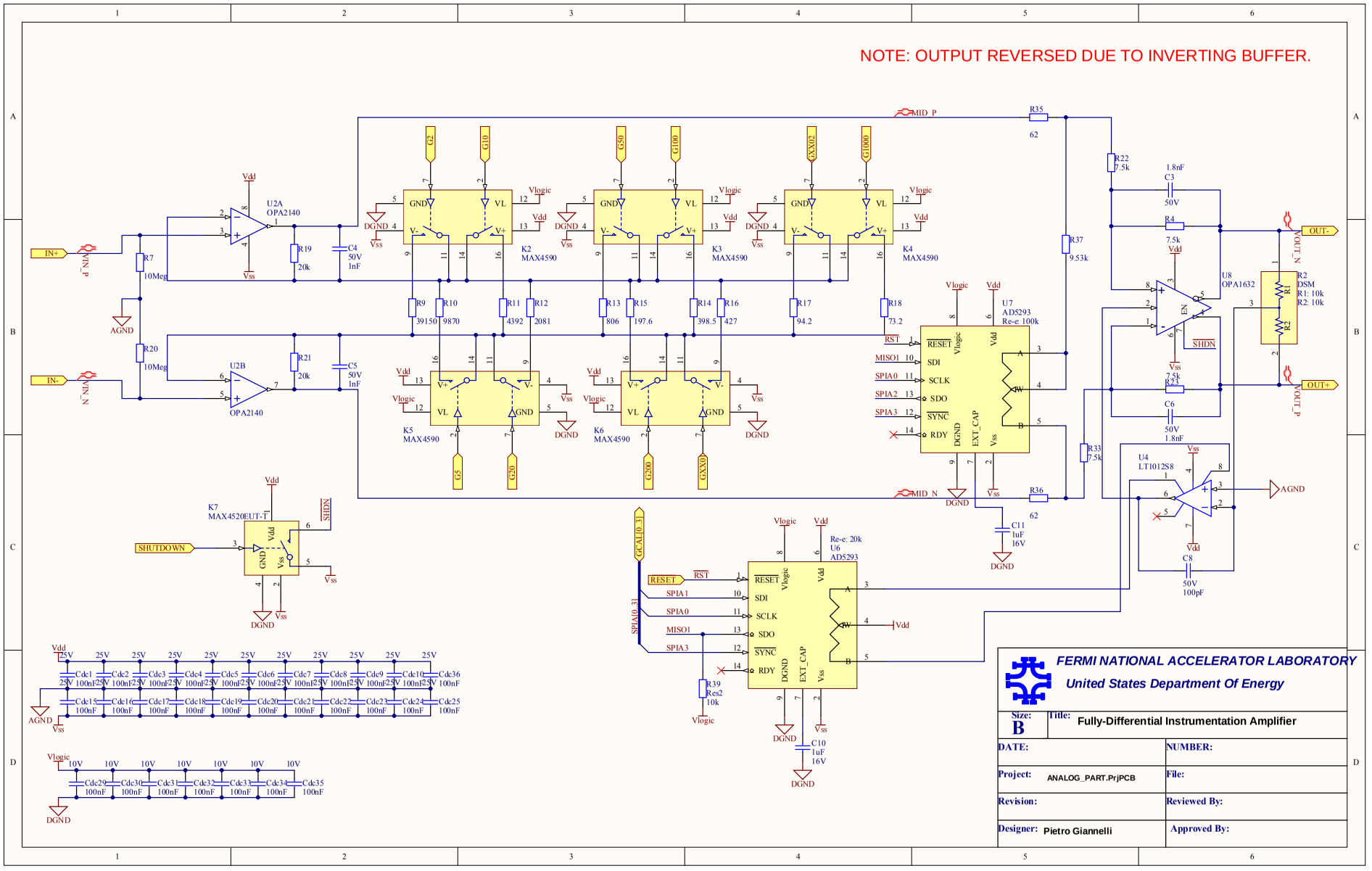
CIRCUIT SCHEMATICS

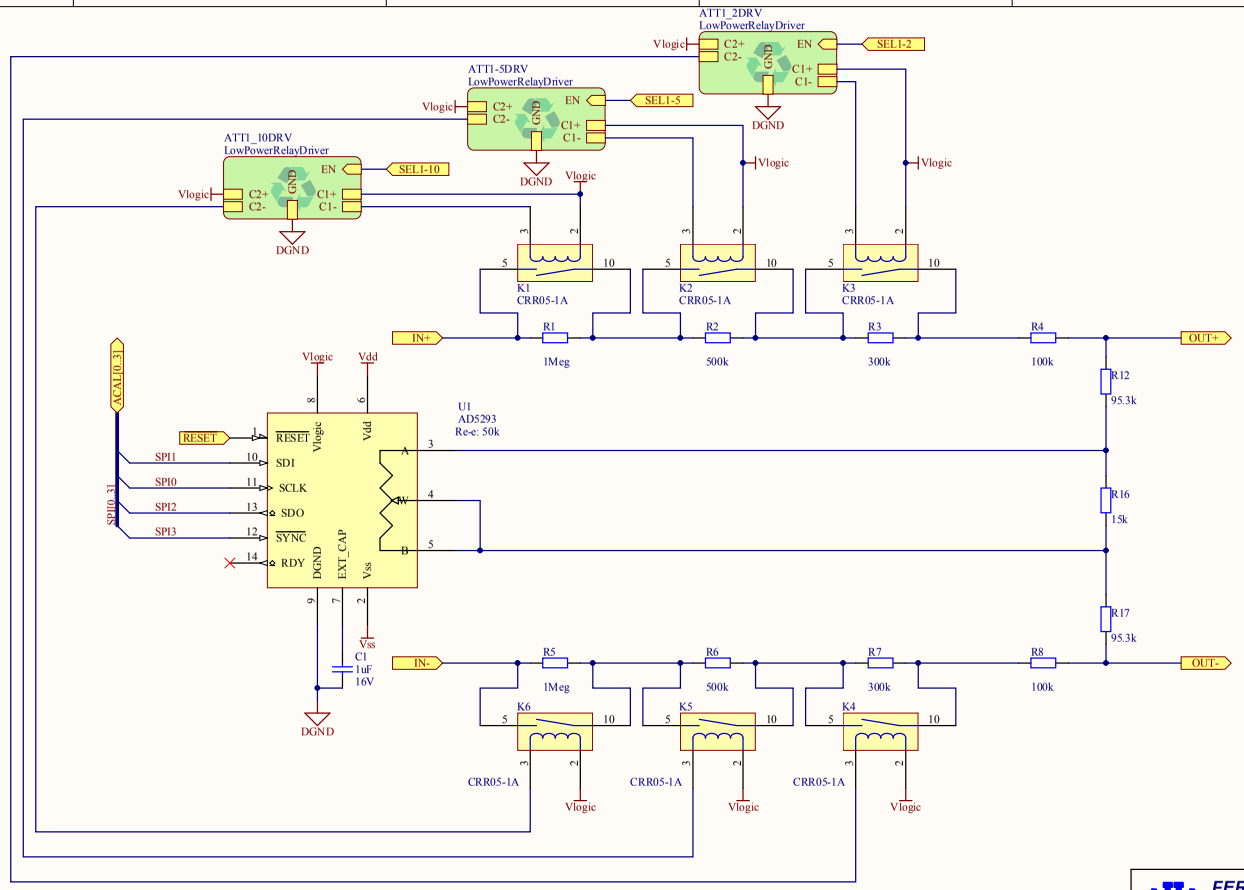


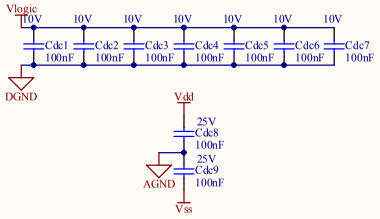
FERMI NATIONAL ACCELERATOR LABORATORY *United States Department Of Energy*	
Size: A	Title: Low power relay driver 3
Date:	Number:
Project:	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:



FERMI NATIONAL ACCELERATOR LABORATORY	
United States Department Of Energy	
Size: A	Title: Input Voltage Clamp with Sensing
Date:	Number:
Project: ANALOG_PART.PrjPCB	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:


NOTE: OUTPUT REVERSED DUE TO INVERTING BUFFER.
IN+
IN-
U2A
OPA2140
U2B
OPA2140
R7
10Meg
R20
10Meg
R19
20k
R21
20k
C4
50V
1nF
C5
50V
1nF
AGND
K2
MAX4590
K3
MAX4590
K4
MAX4590
K5
MAX4590
K6
MAX4590
R9
39150
R10
9870
R11
4392
R12
2081
R13
806
R15
197.6
R14
398.5
R16
427
R17
94.2
R18
73.2
MID_P
MID_N
R35
62
R36
62
R37
9.53k
R33
7.5k
U7
AD5293
Re-e: 100k
U6
AD5293
Re-e: 20k
R22
7.5k
C3
1.8nF
50V
R4
7.5k
U8
OPA1632
R2
DSM
R1: 10k
R2: 10k
R23
7.5k
C6
50V
1.8nF
U4
LT1012S8
OUT-
OUT+
SHDN
K7
MAX4520EUT-T
SHUTDOWN
R39
Res2
10k
C11
1uF
16V
C10
1uF
16V
C8
50V
100pF
Cdc1
Cdc2
Cdc3
Cdc4
Cdc5
Cdc6
Cdc7
Cdc8
Cdc9
Cdc10
Cdc36
Cdc15
Cdc16
Cdc17
Cdc18
Cdc19
Cdc20
Cdc21
Cdc22
Cdc23
Cdc24
Cdc25
Cdc29
Cdc30
Cdc31
Cdc32
Cdc33
Cdc34
Cdc35
100nF
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: B
Title: Fully-Differential Instrumentation Amplifier
DATE:
NUMBER:
Project: ANALOG_PART.PrjPCB
File:
Revision:
Reviewed By:
Designer: Pietro Giannelli
Approved By:

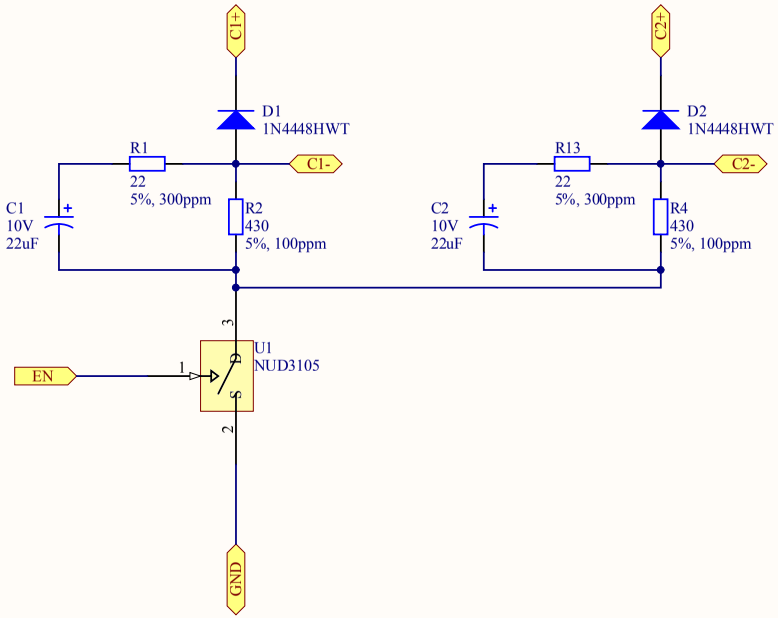




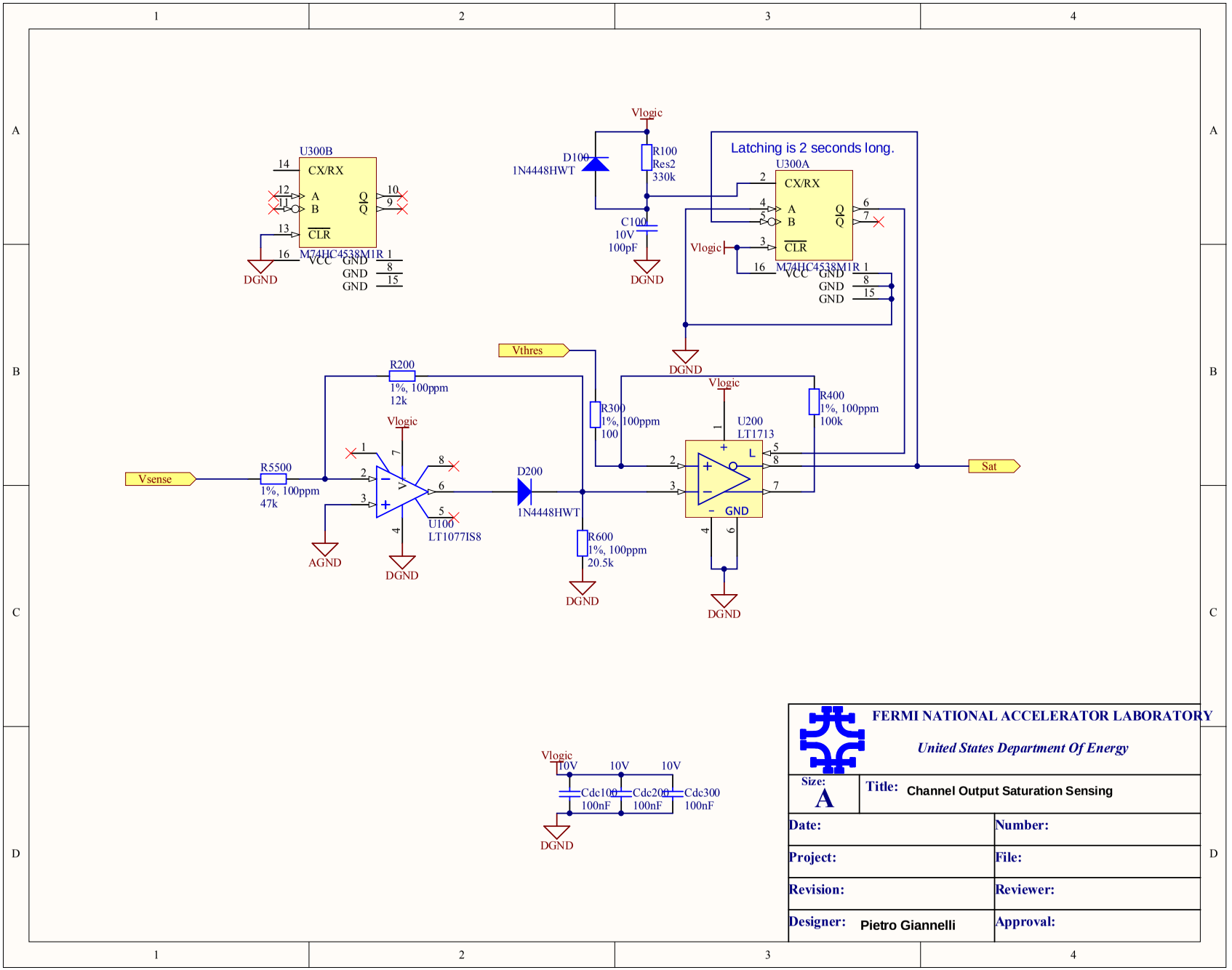
FERMI NATIONAL ACCELERATOR LABORATORY

United States Department Of Energy

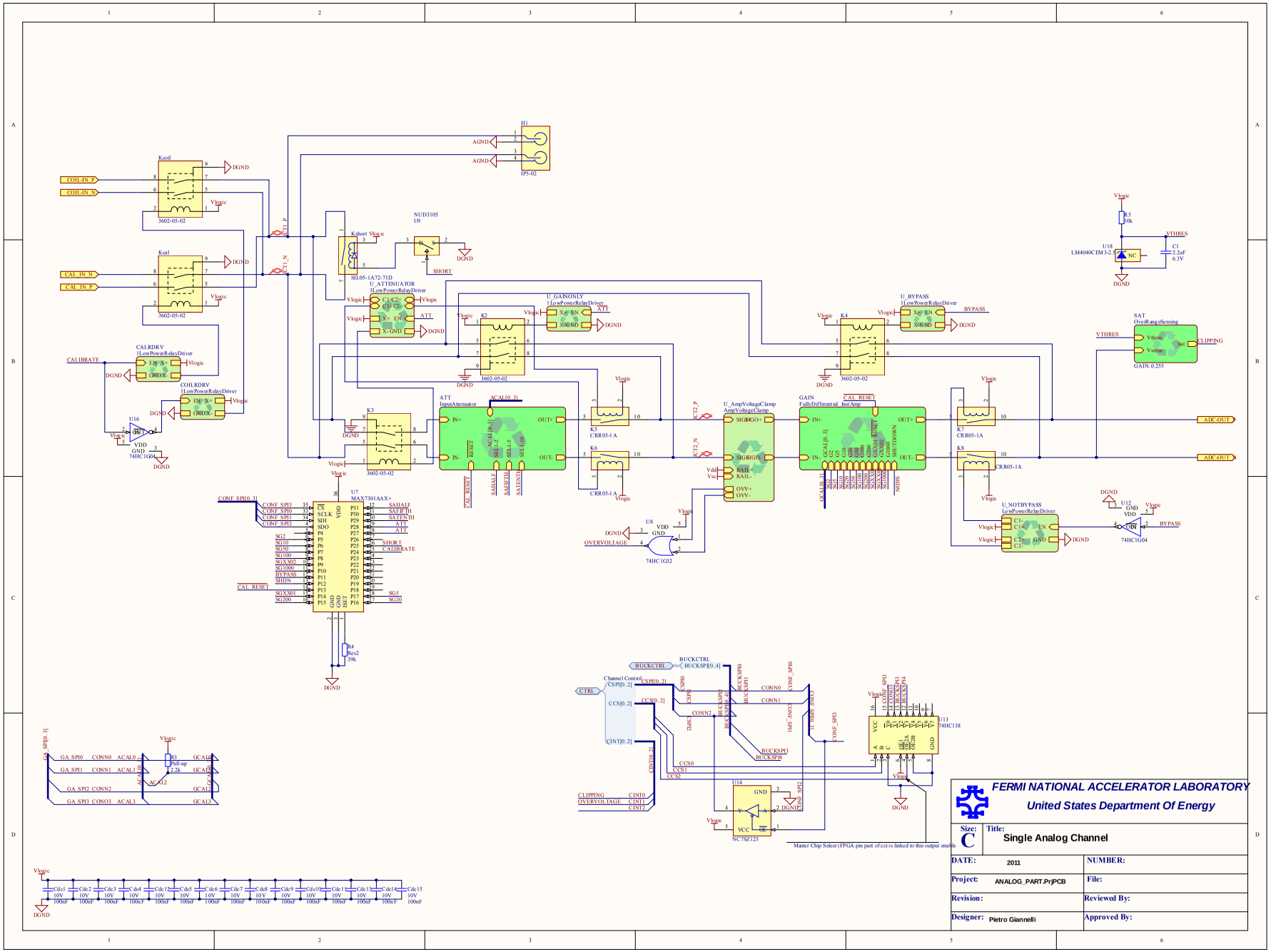
Size: B	Title: Input Attenuator
DATE:	NUMBER:
Project:	File:
Revision:	Reviewed By:
Designer: Pietro Giannelli	Approved By:

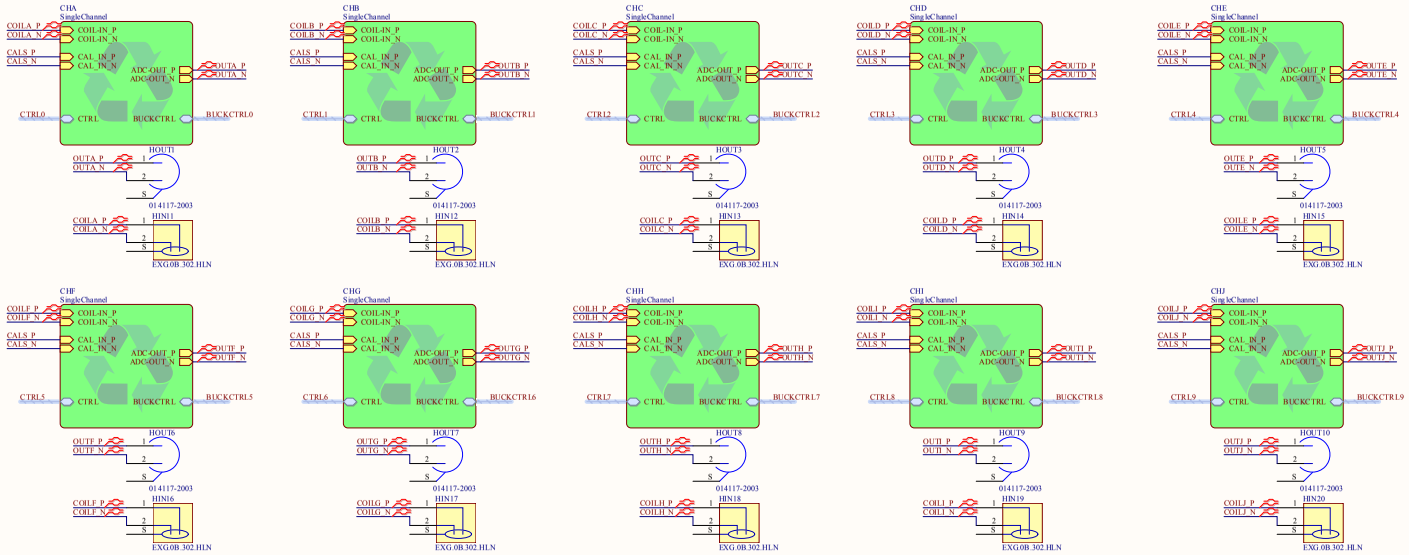


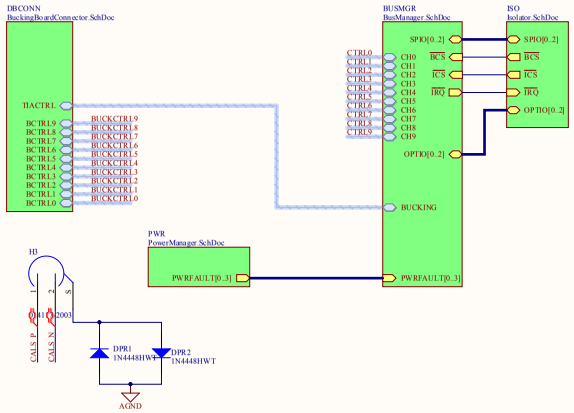
FERMI NATIONAL ACCELERATOR LABORATORY	
United States Department Of Energy	
Size: A	Title: Low power relay driver 2
Date:	Number:
Project:	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:



FERMI NATIONAL ACCELERATOR LABORATORY	
United States Department Of Energy	
Size: A	Title: Channel Output Saturation Sensing
Date:	Number:
Project:	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:


FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: C
Title: Single Analog Channel
DATE: 2011
NUMBER:
Project: ANALOG_PART.PrjPCB
File:
Revision:
Reviewed By:
Designer: Pietro Giannelli
Approved By:
Master Chip Select (FPGA pin part of cs) is linked to this output enable

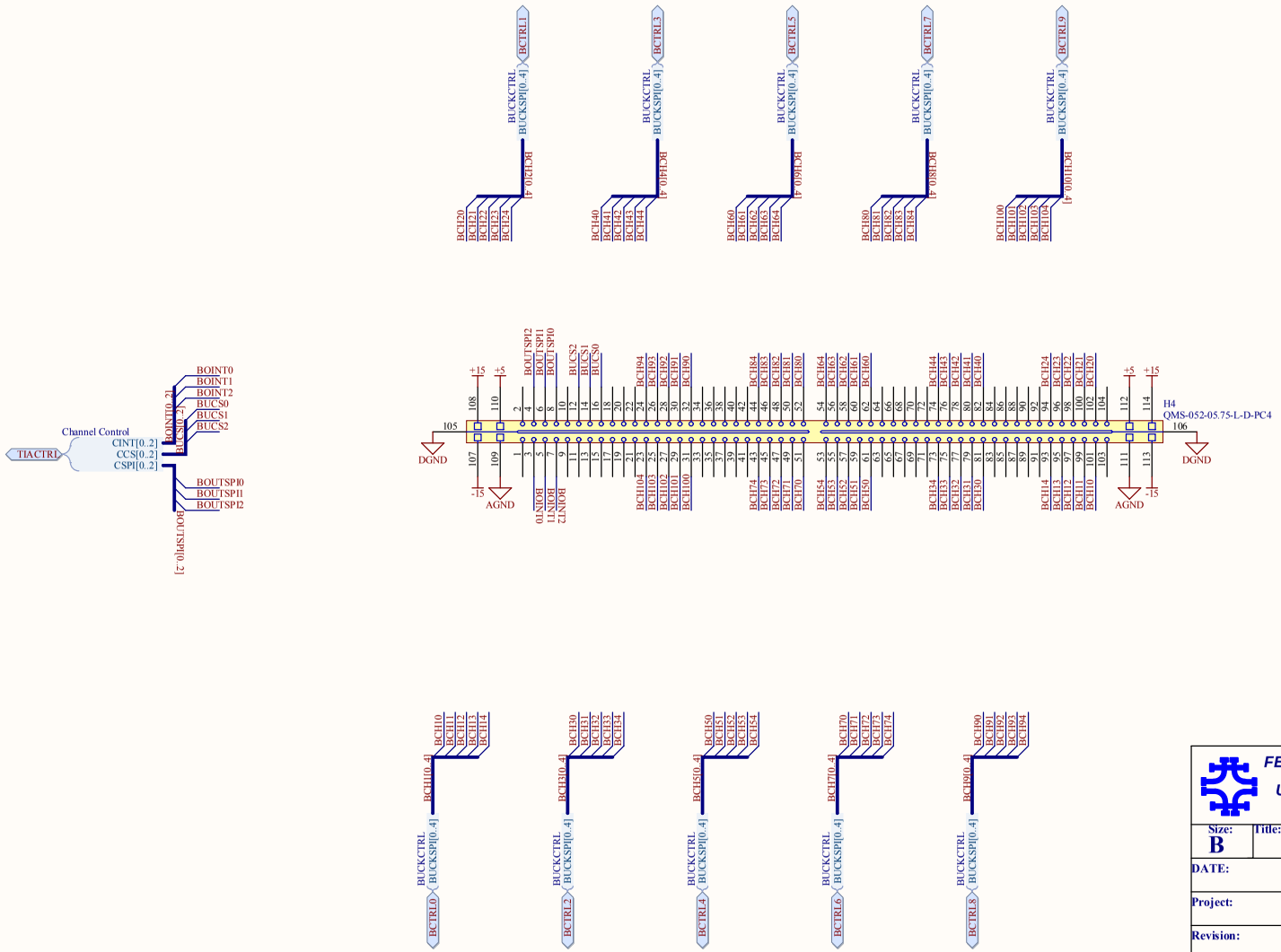




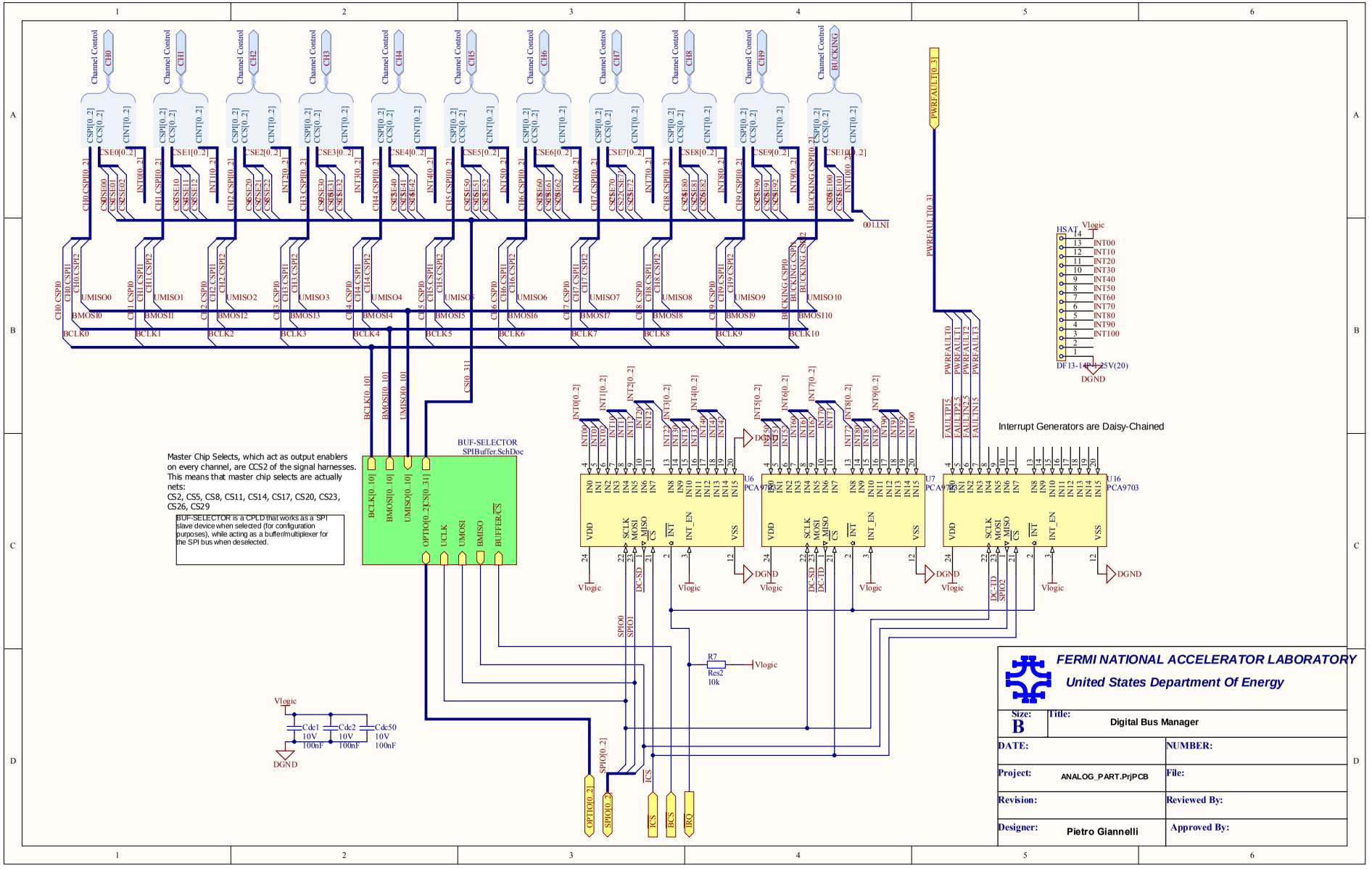
FERMI NATIONAL ACCELERATOR LABORATORY

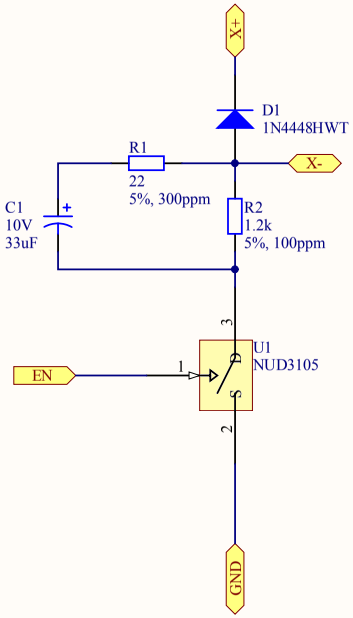
United States Department Of Energy

Size: C	Title: Analog Board
DATE:	NUMBER:
Project:	File: ANALOG_PART.PrjPCB
Revision:	Reviewed By:
Designer: Pietro Giannelli	Approved By:

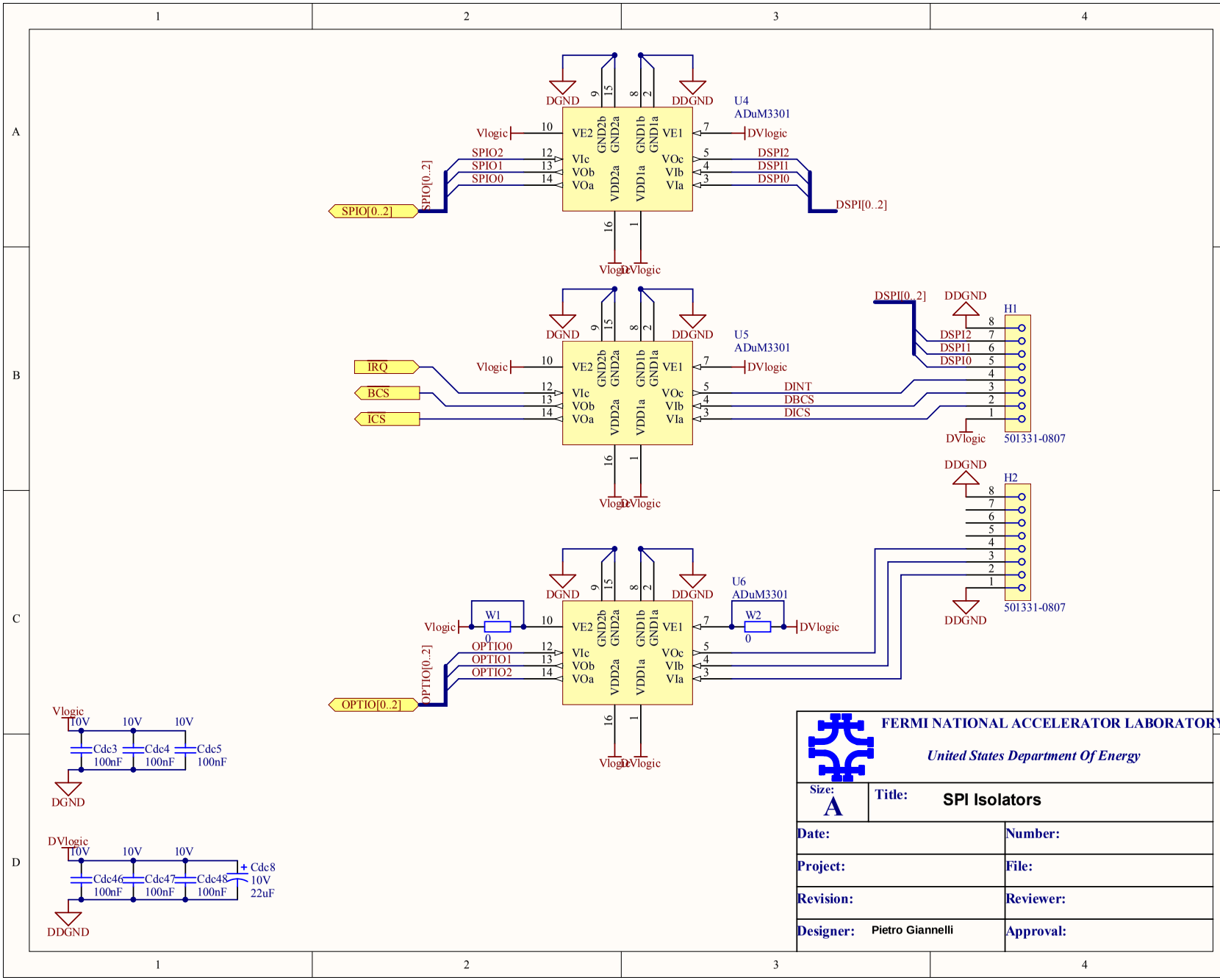


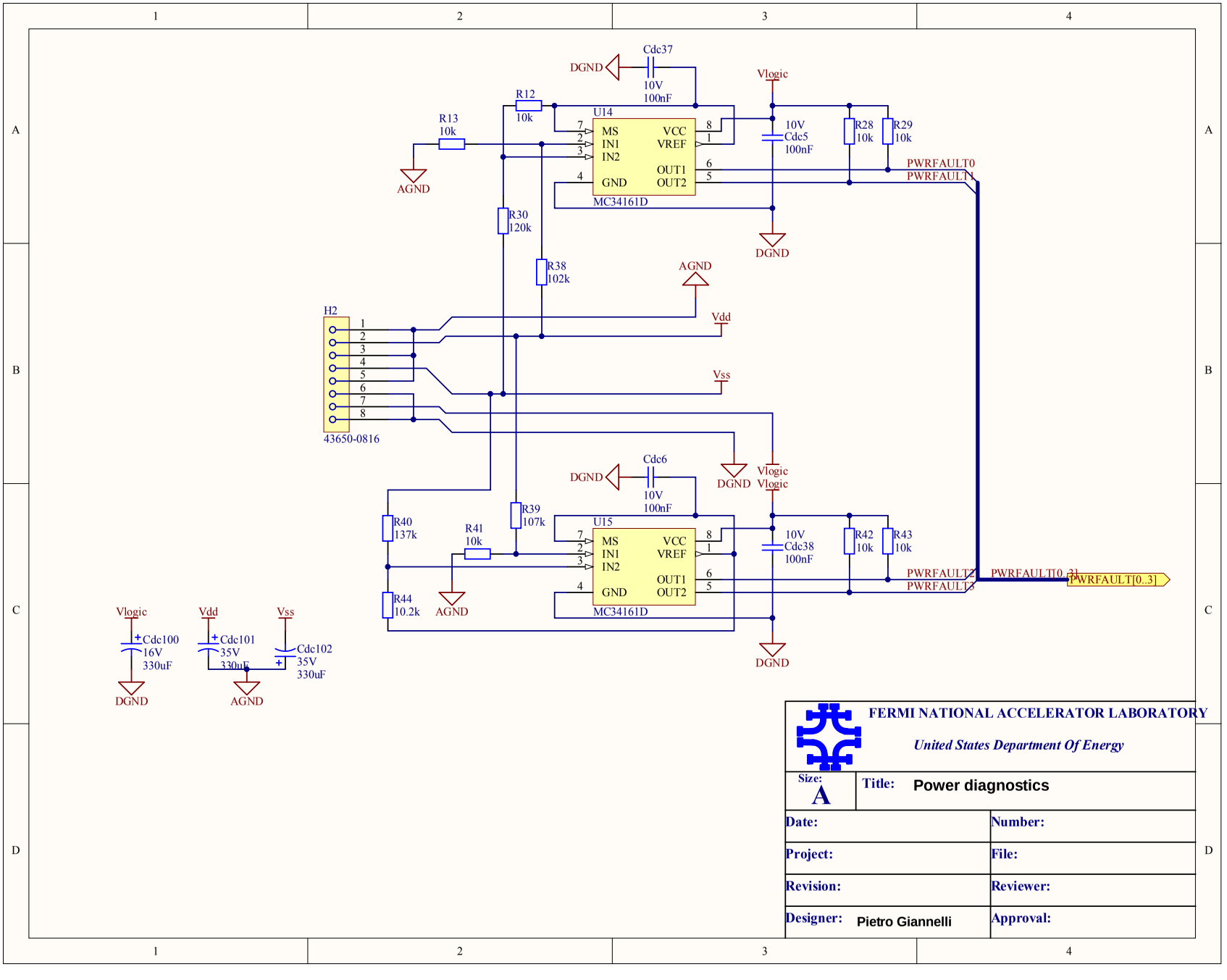
FERMI NATIONAL ACCELERATOR LABORATORY	
United States Department Of Energy	
Size: B	Title: Board-to-board digital connector
DATE:	NUMBER:
Project:	File:
Revision:	Reviewed By:
Designer: Pietro Giannelli	Approved By:

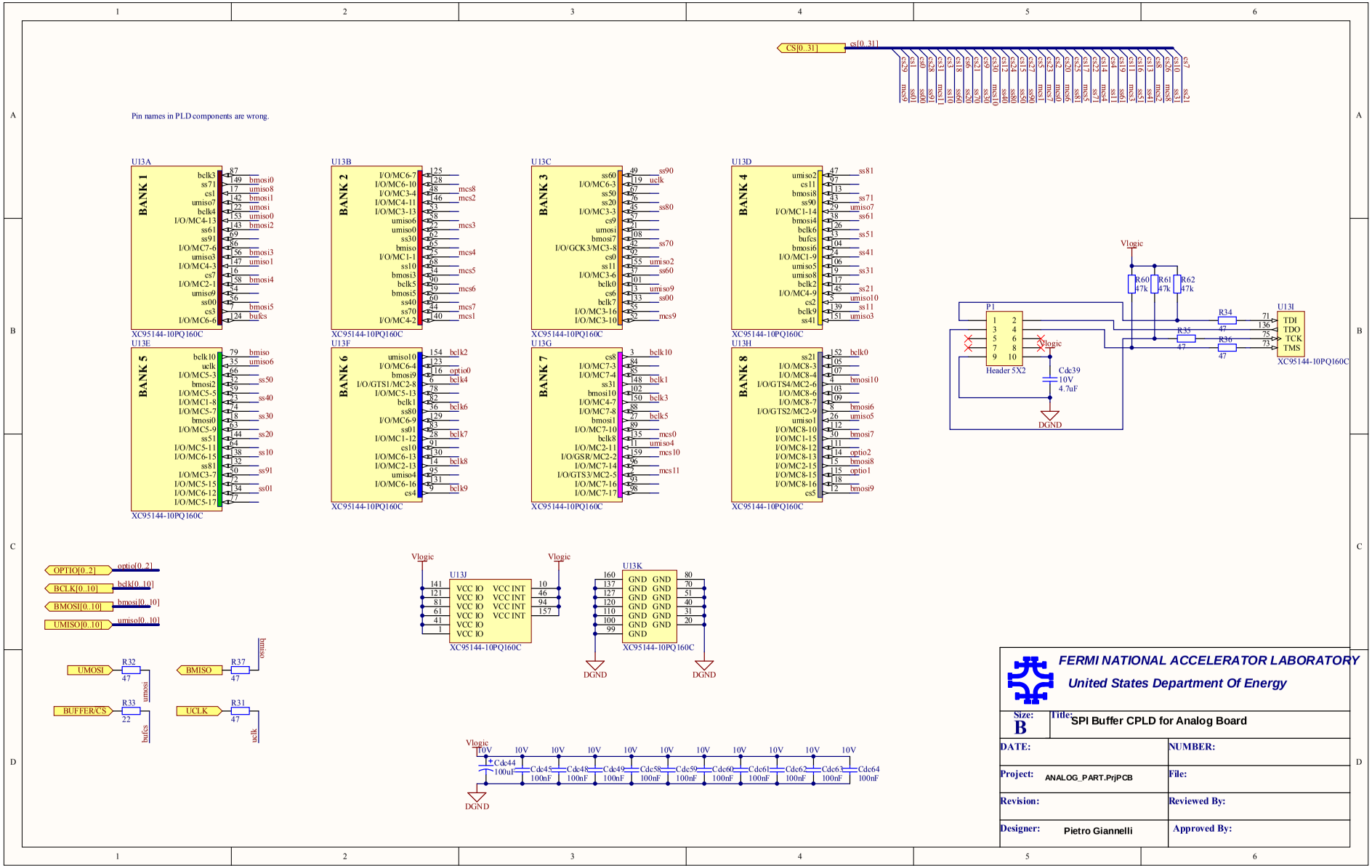

Channel Control CH0
Channel Control CH1
Channel Control CH2
Channel Control CH3
Channel Control CH4
Channel Control CH5
Channel Control CH6
Channel Control CH7
Channel Control CH8
Channel Control CH9
Channel Control BUCKING
CSP[0..2]
CCS[0..2]
CINT[0..2]
CSE0[0..2]
CSE1[0..2]
CSE2[0..2]
CSE3[0..2]
CSE4[0..2]
CSE5[0..2]
CSE6[0..2]
CSE7[0..2]
CSE8[0..2]
CSE9[0..2]
CSE10[0..2]
INT00[0..2]
INT10[0..2]
INT20[0..2]
INT30[0..2]
INT40[0..2]
INT50[0..2]
INT60[0..2]
INT70[0..2]
INT80[0..2]
INT90[0..2]
INT100[0..2]
001.LNI
PWRFAULT[0..31]
PWRFAULT0
PWRFAULT1
PWRFAULT2
PWRFAULT3
HSAT_14
DF13-14P-1.25V(20)
DGND
Vlogic
UMISO0
UMISO1
UMISO2
UMISO3
UMISO4
UMISO5
UMISO6
UMISO7
UMISO8
UMISO9
UMISO10
BMOSI0
BMOSI1
BMOSI2
BMOSI3
BMOSI4
BMOSI5
BMOSI6
BMOSI7
BMOSI8
BMOSI9
BMOSI10
BCLK0
BCLK1
BCLK2
BCLK3
BCLK4
BCLK5
BCLK6
BCLK7
BCLK8
BCLK9
BCLK10
BUF-SELECTOR
SPIBuffer.SchDoc
Master Chip Selects, which act as output enablers on every channel, are CCS2 of the signal harnesses. This means that master chip selects are actually nets:
CS2, CS5, CS8, CS11, CS14, CS17, CS20, CS23, CS26, CS29
BUF-SELECTOR is a CPLD that works as a SPI slave device when selected (for configuration purposes), while acting as a buffer/multiplexer for the SPI bus when deselected.
Interrupt Generators are Daisy-Chained
U6 PCA9703
U7 PCA9703
U16 PCA9703
SCLK
MOSI
MISO
CS
INT
INT_EN
VDD
VSS
DC-SD
DC-TD
SPIO0
SPIO1
SPIO2
SPIO[0..2]
OPTIC[0..2]
ICS
BCS
IRQ
R7
Res2
10k
Cdc1
Cdc2
Cdc50
10V
100nF
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: B
Title: Digital Bus Manager
DATE:
NUMBER:
Project: ANALOG_PART.PrjPCB
File:
Revision:
Reviewed By:
Designer: Pietro Giannelli
Approved By:

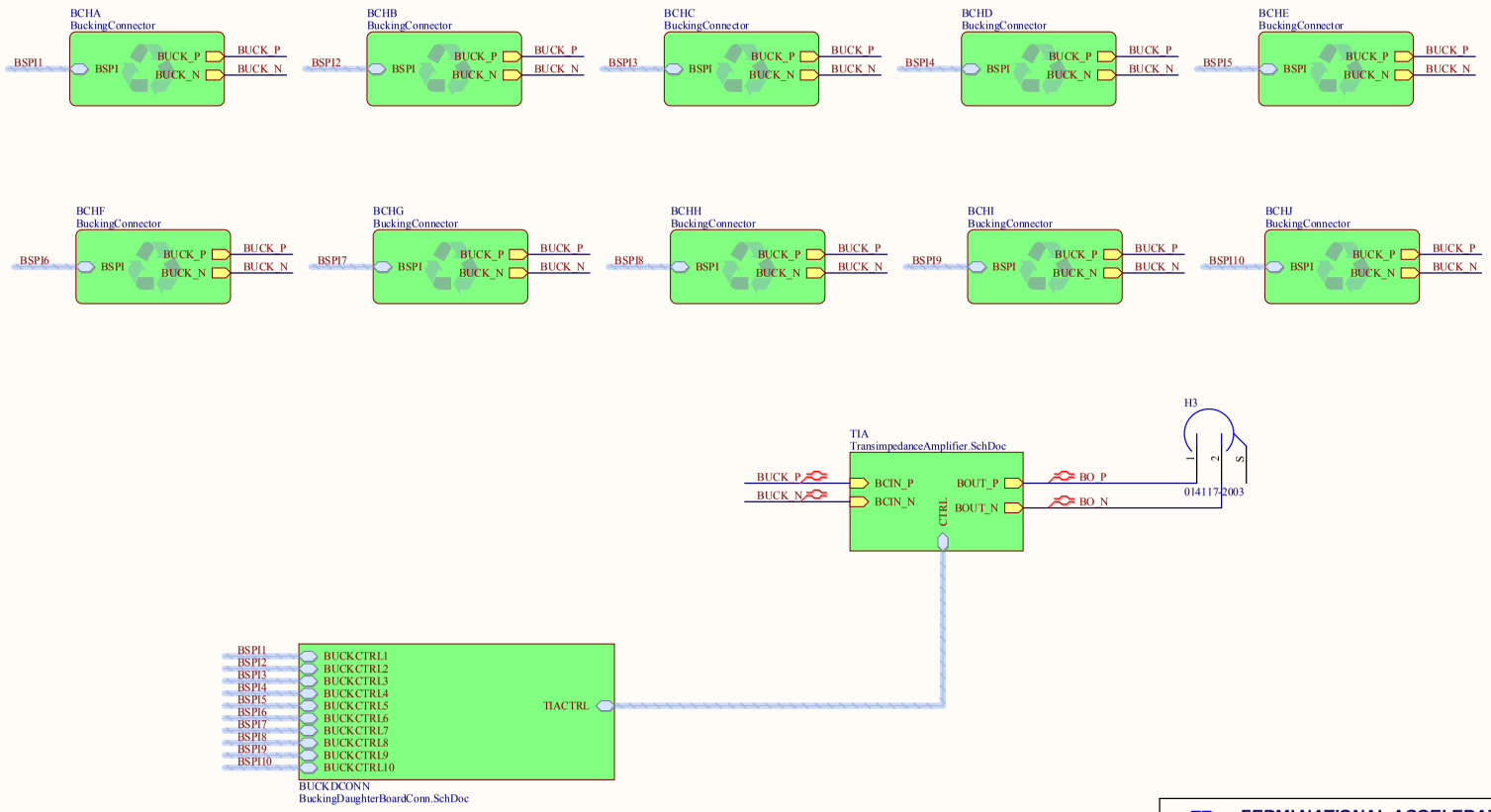


FERMI NATIONAL ACCELERATOR LABORATORY *United States Department Of Energy*	
Size: A	Title: Low power relay driver 1
Date:	Number:
Project: ANALOG_PART.PrjPCB	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:

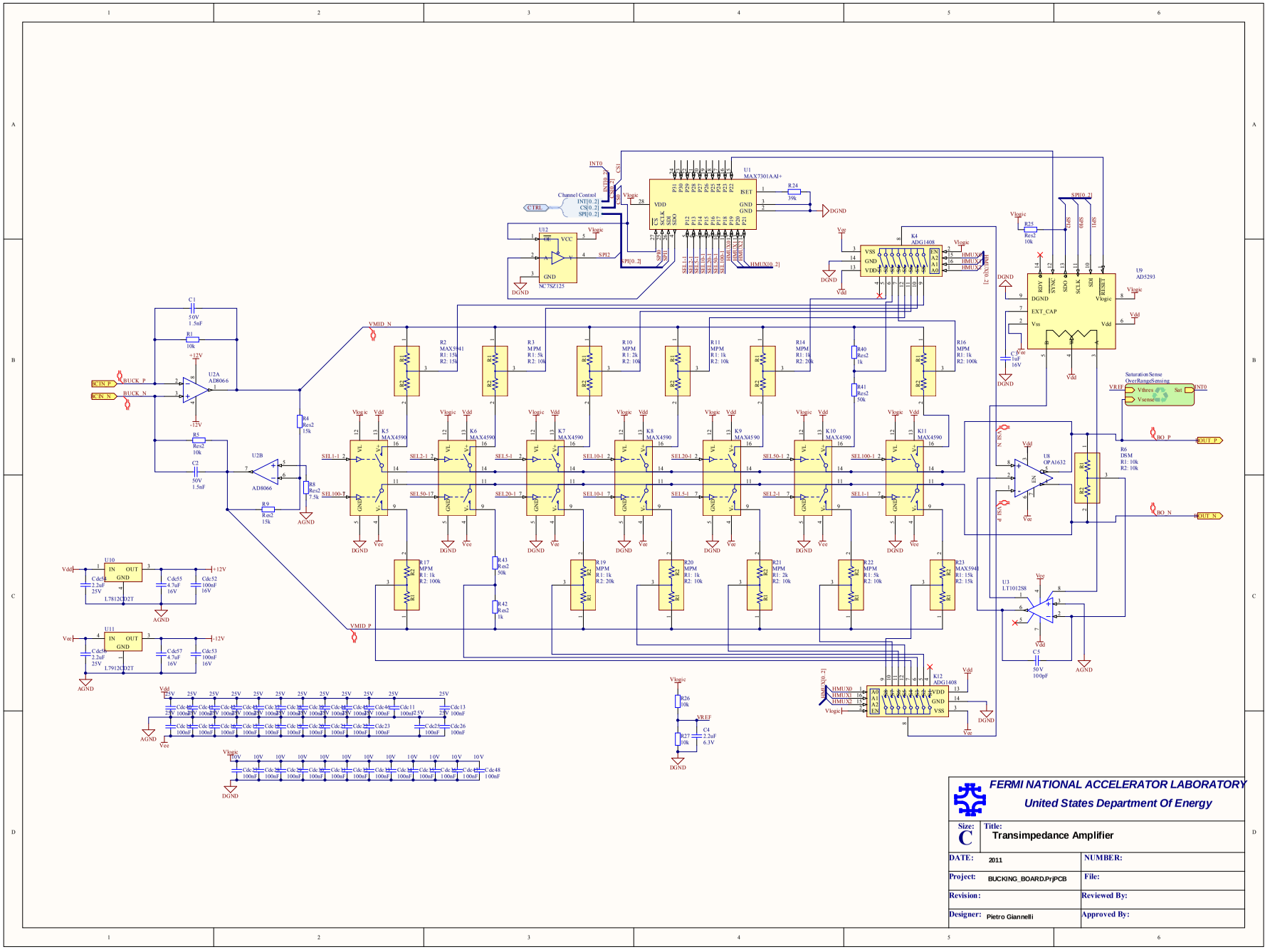

U4
ADuM3301
U5
ADuM3301
U6
ADuM3301
DGND
DDGND
DVlogic
Vlogic
SPIO[0..2]
DSPI[0..2]
IRQ
BCS
ICS
DINT
DBCS
DICS
H1
H2
501331-0807
W1
W2
OPTIO[0..2]
Cdc3
Cdc4
Cdc5
Cdc46
Cdc47
Cdc48
Cdc8
100nF
10V
22uF
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: A
Title: SPI Isolators
Date:
Number:
Project:
File:
Revision:
Reviewer:
Designer: Pietro Giannelli
Approval:

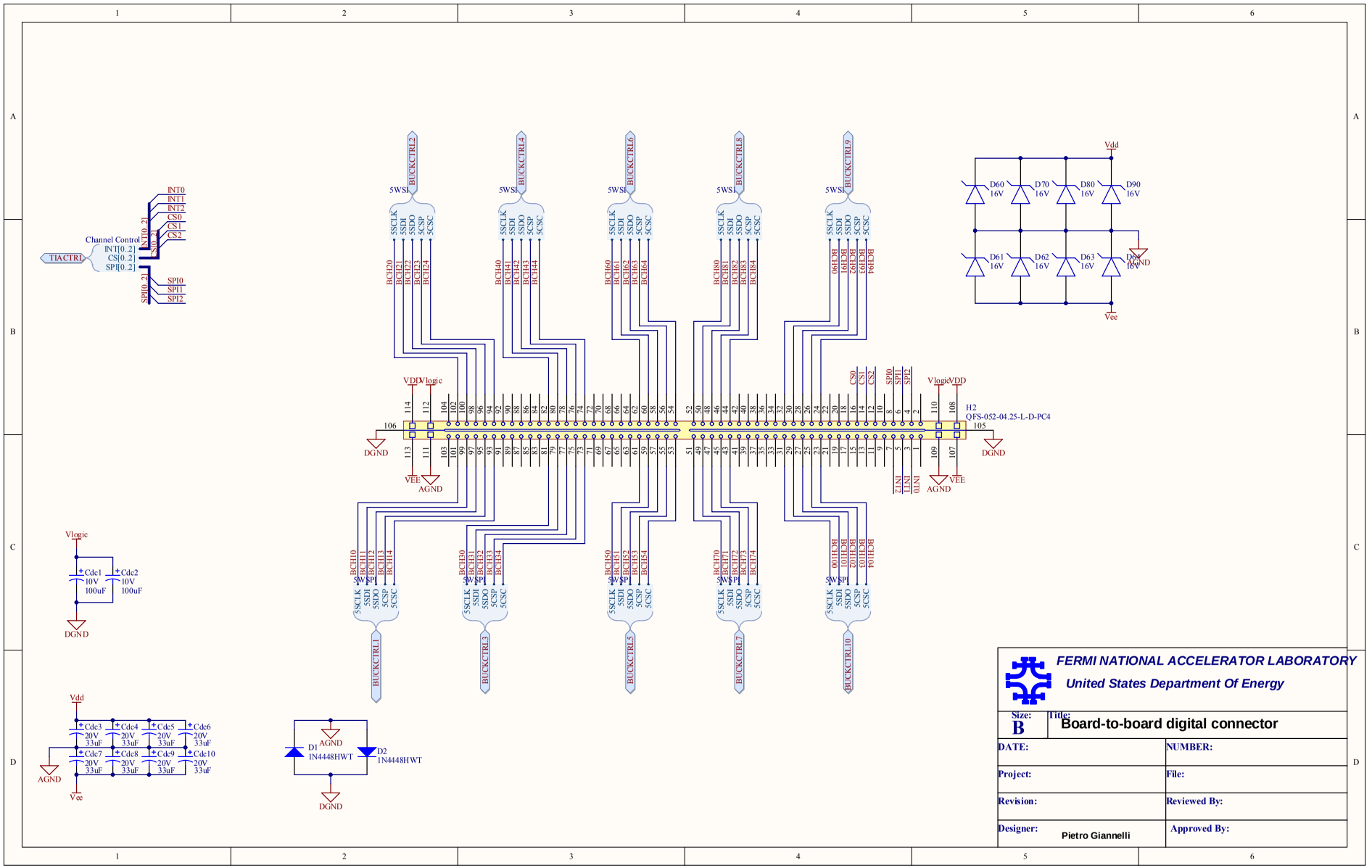

Cdc37
DGND
10V
100nF
Vlogic
R12
10k
R13
10k
U14
MS
IN1
IN2
GND
VCC
VREF
OUT1
OUT2
MC34161D
AGND
10V
Cdc5
100nF
R28
10k
R29
10k
PWRFAULT0
PWRFAULT1
R30
120k
R38
102k
AGND
H2
1
2
3
4
5
6
7
8
43650-0816
Vdd
Vss
Cdc6
DGND
10V
100nF
Vlogic
Vlogic
DGND
R39
107k
R40
137k
R41
10k
U15
MS
IN1
IN2
GND
VCC
VREF
OUT1
OUT2
MC34161D
10V
Cdc38
100nF
R42
10k
R43
10k
PWRFAULT2
PWRFAULT3
PWRFAULT[0..3]
R44
10.2k
AGND
DGND
Vlogic
Vdd
Vss
Cdc100
16V
330uF
Cdc101
35V
330uF
Cdc102
35V
330uF
DGND
AGND
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size:
A
Title:
Power diagnostics
Date:
Number:
Project:
File:
Revision:
Reviewer:
Designer:
Pietro Giannelli
Approval:

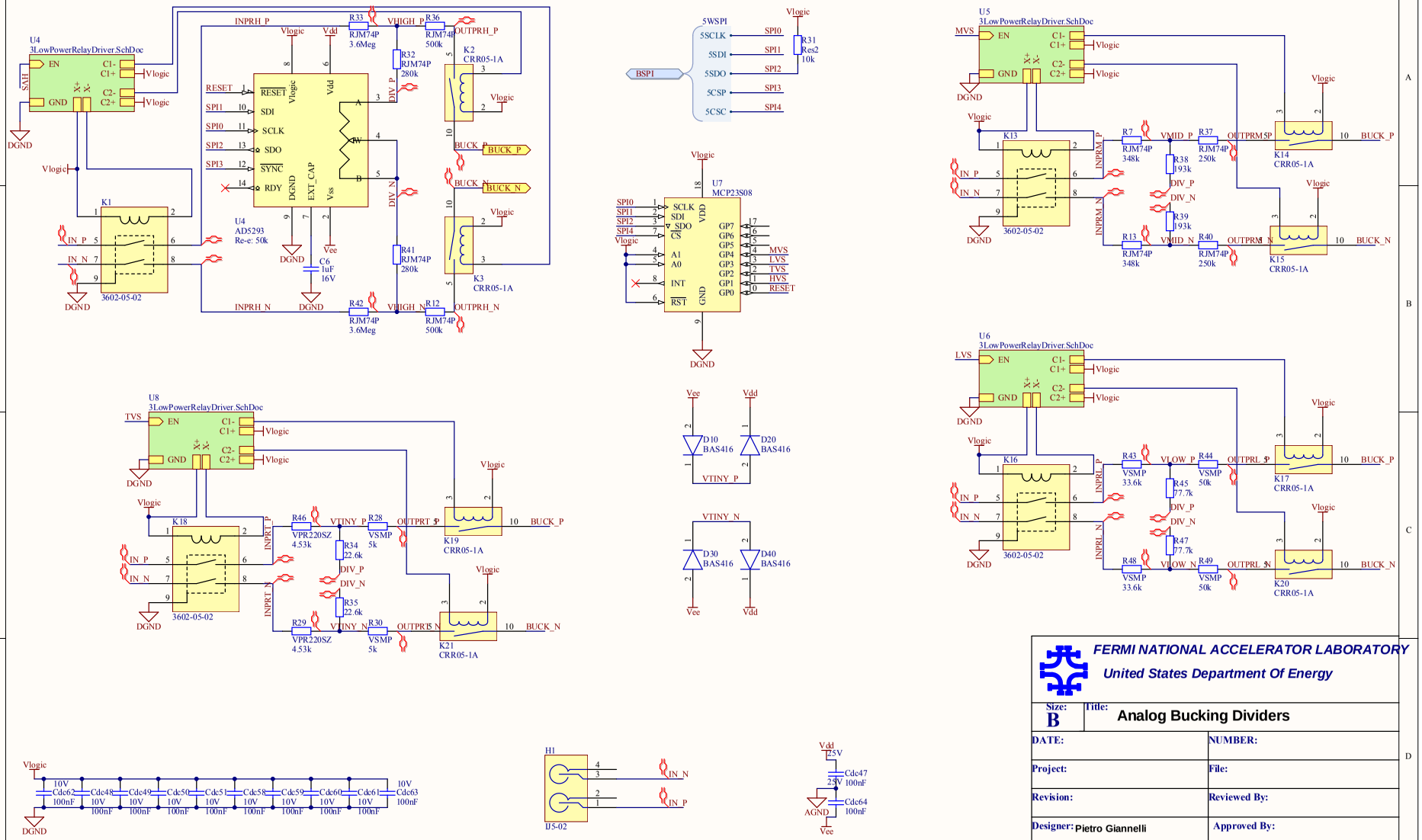

Pin names in PLD components are wrong.
CS[0..31]
ss[0..31]
U13A
BANK 1
XC95144-10PQ160C
U13B
BANK 2
XC95144-10PQ160C
U13C
BANK 3
XC95144-10PQ160C
U13D
BANK 4
XC95144-10PQ160C
U13E
BANK 5
XC95144-10PQ160C
U13F
BANK 6
XC95144-10PQ160C
U13G
BANK 7
XC95144-10PQ160C
U13H
BANK 8
XC95144-10PQ160C
Vlogic
P1
Header 5X2
Cdc39
10V
4.7uF
DGND
R60
47k
R61
47k
R62
47k
R34
47
R35
47
R36
47
U13I
TDI
TDO
TCK
TMS
XC95144-10PQ160C
OPTIO[0..2]
BCLK[0..10]
BMOSI[0..10]
UMISO[0..10]
UMOSI
BMISO
BUFFER/CS
UCLK
R32
R33
R37
R31
U13J
U13K
Cdc44
100uF
Cdc45
Cdc48
Cdc49
Cdc58
Cdc59
Cdc60
Cdc61
Cdc62
Cdc63
Cdc64
100nF
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: B
Title: SPI Buffer CPLD for Analog Board
DATE:
NUMBER:
Project: ANALOG_PART.PrjPCB
File:
Revision:
Reviewed By:
Designer: Pietro Giannelli
Approved By:

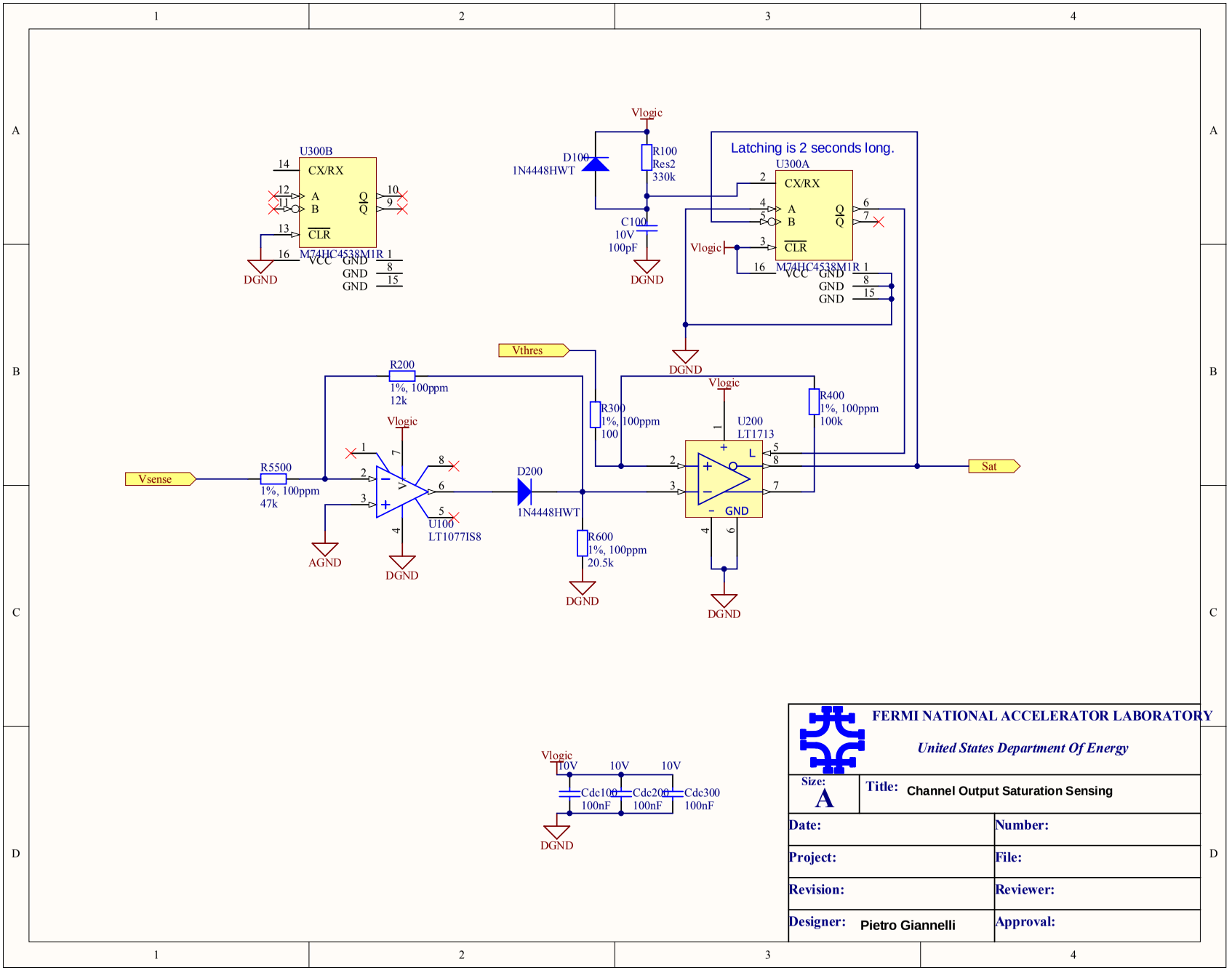


FERMI NATIONAL ACCELERATOR LABORATORY United States Department Of Energy	
Size: B	Title: Bucking board outline
DATE:	NUMBER:
Project:	File:
Revision:	Reviewed By:
Designer: Pietro Giannelli	Approved By:

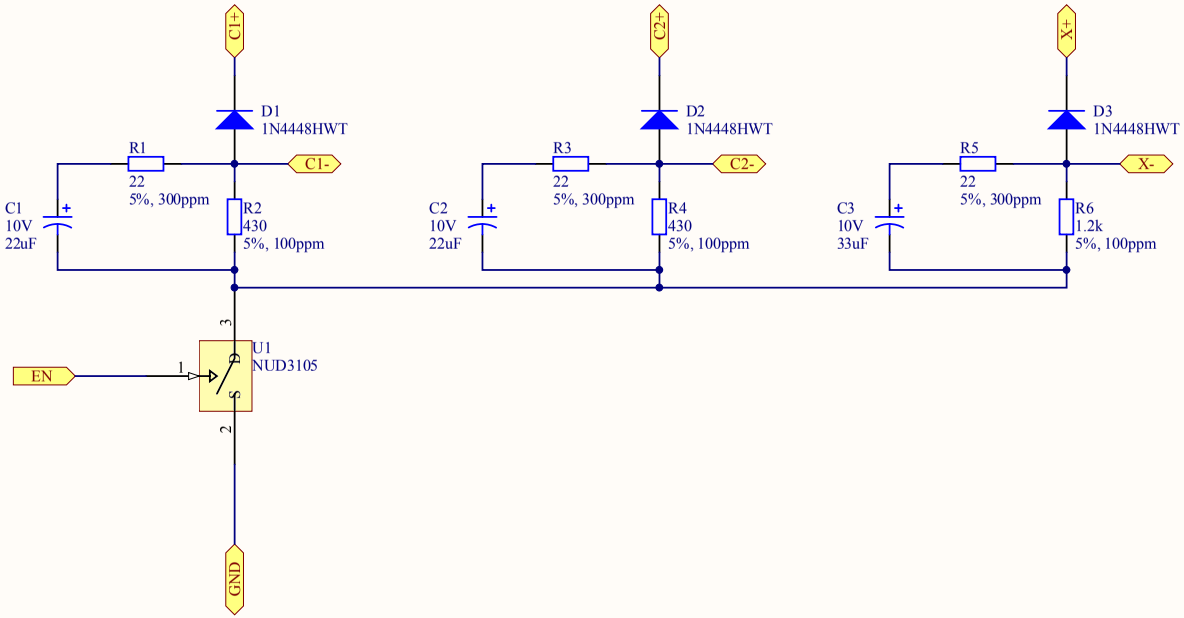

FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size: C
Title: Transimpedance Amplifier
DATE: 2011
NUMBER:
Project: BUCKING_BOARD.PrjPCB
File:
Revision:
Reviewed By:
Designer: Pietro Giannelli
Approved By:


TIA CTRL
Channel Control
INT[0..2]
CS[0..2]
SPI[0..2]
INT0
INT1
INT2
CS0
CS1
CS2
SPI0
SPI1
SPI2
BUCKCTRL2
BUCKCTRL4
BUCKCTRL6
BUCKCTRL8
BUCKCTRL9
5WSI
5SCLK
5SDI
5SDO
5CSP
5CSC
BCH20
BCH21
BCH22
BCH23
BCH24
BCH40
BCH41
BCH42
BCH43
BCH44
BCH60
BCH61
BCH62
BCH63
BCH64
BCH80
BCH81
BCH82
BCH83
BCH84
BCH90
BCH91
BCH92
BCH93
BCH94
VDD
Vlogic
DGND
VEE
AGND
H2
QFS-052-04.25-L-D-PC4
Vdd
Vee
D60
D70
D80
D90
D61
D62
D63
D64
16V
BCH10
BCH11
BCH12
BCH13
BCH14
BCH30
BCH31
BCH32
BCH33
BCH34
BCH50
BCH51
BCH52
BCH53
BCH54
BCH70
BCH71
BCH72
BCH73
BCH74
BCH100
BCH101
BCH102
BCH103
BCH104
5WSPI
BUCKCTRL1
BUCKCTRL3
BUCKCTRL5
BUCKCTRL7
BUCKCTRL10
Cdc1
Cdc2
Cdc3
Cdc4
Cdc5
Cdc6
Cdc7
Cdc8
Cdc9
Cdc10
10V
100uF
20V
33uF
D1
D2
1N4448HWT
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size:
B
Title:
Board-to-board digital connector
DATE:
NUMBER:
Project:
File:
Revision:
Reviewed By:
Designer:
Pietro Giannelli
Approved By:


U4
3LowPowerRelayDriver.SchDoc
INPRH_P
INPRH_N
VHIGH_P
VHIGH_N
OUTPRH_P
OUTPRH_N
R33
RJM74P
3.6Meg
R36
RJM74P
500k
R32
RJM74P
280k
R41
RJM74P
280k
R42
RJM74P
3.6Meg
R12
RJM74P
500k
K1
K2
K3
3602-05-02
CRR05-1A
U4
AD5293
Re-e: 50k
C6
1uF
16V
RESET
SPI1
SPI0
SPI2
SPI3
SDI
SCLK
SDO
SYNC
RDY
DGND
EXT_CAP
Vss
Vdd
Vee
Vlogic
DIV_P
DIV_N
BUCK_P
BUCK_N
IN_P
IN_N
5WSPI
5SCLK
5SDI
5SDO
5CSP
5CSC
BSP1
SPI0
SPI1
SPI2
SPI3
SPI4
R31
Res2
10k
U7
MCP23S08
SCLK
SDI
SDO
CS
A1
A0
INT
RST
GP7
GP6
GP5
GP4
GP3
GP2
GP1
GP0
MVS
LVS
TVS
HVS
U5
U6
U8
MVS
LVS
TVS
R7
R37
R38
193k
R39
193k
R13
R40
RJM74P
348k
RJM74P
250k
K13
K14
K15
K16
K17
K18
K19
K20
K21
R43
R44
R45
77.7k
R47
77.7k
R48
R49
VSMP
33.6k
VSMP
50k
R46
R28
R34
22.6k
R35
22.6k
R29
R30
VPR220SZ
4.53k
VSMP
5k
D10
D20
D30
D40
BAS416
VTINY_P
VTINY_N
H1
IJ5-02
Vdd
25V
Cdc47
100nF
Cdc64
100nF
AGND
Cdc62
Cdc48
Cdc49
Cdc50
Cdc51
Cdc58
Cdc59
Cdc60
Cdc61
Cdc63
10V
100nF
FERMI NATIONAL ACCELERATOR LABORATORY
United States Department Of Energy
Size:
B
Title:
Analog Bucking Dividers
DATE:
NUMBER:
Project:
File:
Revision:
Reviewed By:
Designer:
Pietro Giannelli
Approved By:



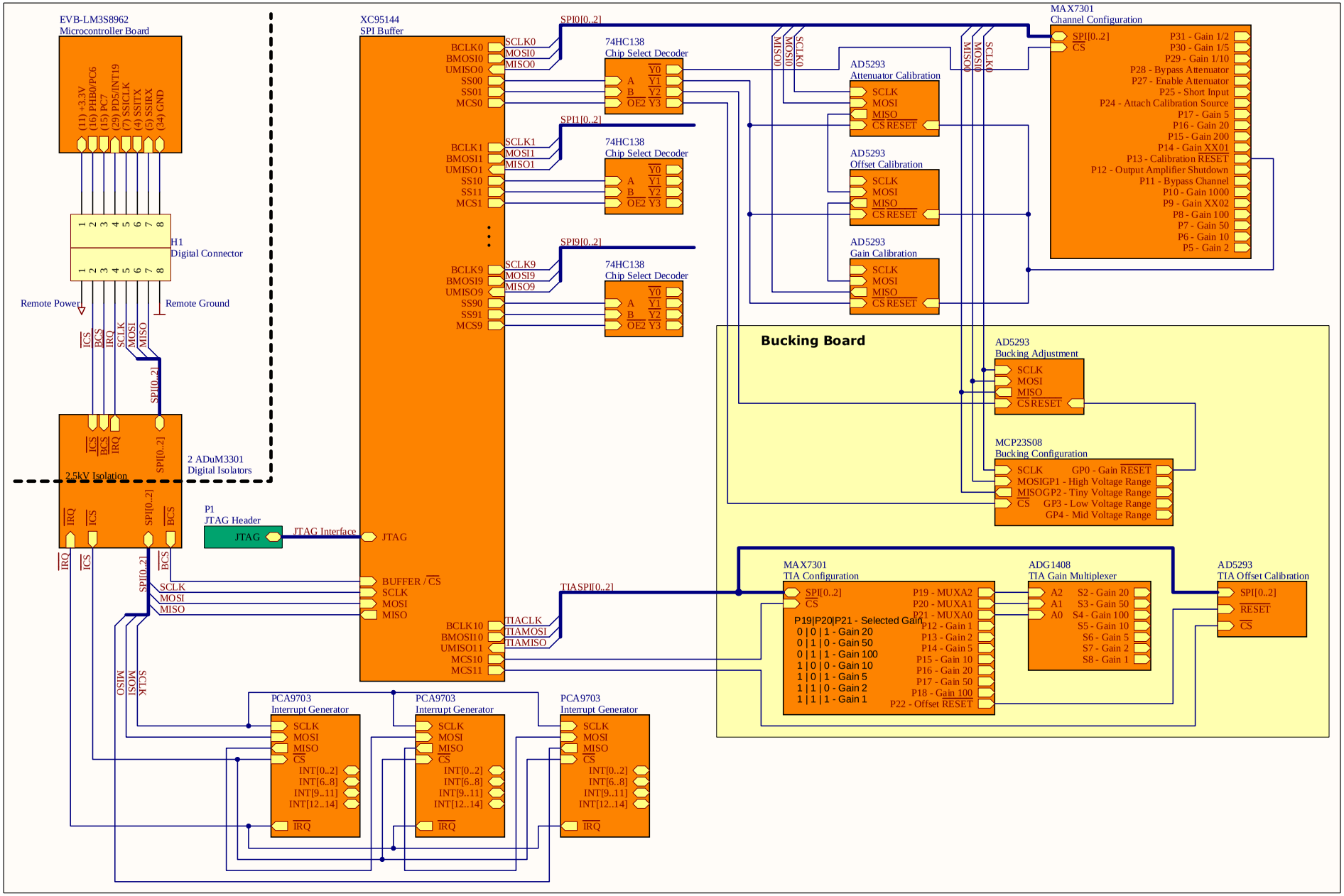
FERMI NATIONAL ACCELERATOR LABORATORY	
United States Department Of Energy	
Size: A	Title: Channel Output Saturation Sensing
Date:	Number:
Project:	File:
Revision:	Reviewer:
Designer: Pietro Giannelli	Approval:



FERMI NATIONAL ACCELERATOR LABORATORY *United States Department Of Energy*		
Size: A	Title: Low power relay driver 3	
Date:		Number:
Project:		File:
Revision:		Reviewer:
Designer: Pietro Giannelli		Approval:

B

DIGITAL CONNECTIONS SCHEME


EVB-LM3S8962
Microcontroller Board
(11) +3.3V
(16) PH0/PC6
(15) PC7
(29) PD5/INT19
(7) SSICLK
(4) SSITX
(5) SSIRX
(34) GND
H1
Digital Connector
Remote Power
Remote Ground
ICS
BCS
IRQ
SCLK
MOSI
MISO
SPI[0..2]
2 ADuM3301
Digital Isolators
2.5kV Isolation
P1
JTAG Header
JTAG
JTAG Interface
XC95144
SPI Buffer
BCLK0
BMOSI0
UMISO0
SS00
SS01
MCS0
SCLK0
MOSI0
MISO0
SPI0[0..2]
BCLK1
BMOSI1
UMISO1
SS10
SS11
MCS1
SCLK1
MOSI1
MISO1
SPI1[0..2]
BCLK9
BMOSI9
UMISO9
SS90
SS91
MCS9
SCLK9
MOSI9
MISO9
SPI9[0..2]
74HC138
Chip Select Decoder
A
B
OE2
Y0
Y1
Y2
Y3
BUFFER / CS
SCLK
MOSI
MISO
BCLK10
BMOSI10
UMISO11
MCS10
MCS11
TIACLK
TIAMOSI
TIAMISO
TIASPI[0..2]
AD5293
Attenuator Calibration
Offset Calibration
Gain Calibration
CS RESET
MAX7301
Channel Configuration
P31 - Gain 1/2
P30 - Gain 1/5
P29 - Gain 1/10
P28 - Bypass Attenuator
P27 - Enable Attenuator
P25 - Short Input
P24 - Attach Calibration Source
P17 - Gain 5
P16 - Gain 20
P15 - Gain 200
P14 - Gain XX01
P13 - Calibration RESET
P12 - Output Amplifier Shutdown
P11 - Bypass Channel
P10 - Gain 1000
P9 - Gain XX02
P8 - Gain 100
P7 - Gain 50
P6 - Gain 10
P5 - Gain 2
Bucking Board
AD5293
Bucking Adjustment
MCP23S08
Bucking Configuration
GP0 - Gain RESET
GP1 - High Voltage Range
GP2 - Tiny Voltage Range
GP3 - Low Voltage Range
GP4 - Mid Voltage Range
MAX7301
TIA Configuration
P19|P20|P21 - Selected Gain
0 | 0 | 1 - Gain 20
0 | 1 | 0 - Gain 50
0 | 1 | 1 - Gain 100
1 | 0 | 0 - Gain 10
1 | 0 | 1 - Gain 5
1 | 1 | 0 - Gain 2
1 | 1 | 1 - Gain 1
P19 - MUXA2
P20 - MUXA1
P21 - MUXA0
P12 - Gain 1
P13 - Gain 2
P14 - Gain 5
P15 - Gain 10
P16 - Gain 20
P17 - Gain 50
P18 - Gain 100
P22 - Offset RESET
ADG1408
TIA Gain Multiplexer
A2
A1
A0
S2 - Gain 20
S3 - Gain 50
S4 - Gain 100
S5 - Gain 10
S6 - Gain 5
S7 - Gain 2
S8 - Gain 1
AD5293
TIA Offset Calibration
RESET
PCA9703
Interrupt Generator
INT[0..2]
INT[6..8]
INT[9..11]
INT[12..14]

C

SPI BUFFER VHDL CODE

```
1  ----------------------------------------------------------------------------
2  -- Company: Fermilab
3  -- Author: Pietro Giannelli
4  --
5  -- Create Date:      06/10/2011
6  -- Design Name:
7  -- Module Name:      SPI_DIST
8  -- Project Name:     Harmonics Signal Conditioner
9  -- Target Devices: XC95144-10PQ160
10 -- Tool versions:   ISE WebPack 13.1 - Altium Designer 10
11 -- Description:      SPI buffer / selector for the signal conditioner
12 --
13 -- Dependencies:
14 --
15 -- Version: 0.1
16 -- Additional Comments:
17 --
18 ----------------------------------------------------------------------------
19
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24 -- MAIN BLOCK
25 entity SPIBUF_IN is
26     port (
27   -- Controller Side
28   uclk, umosi : in STD_LOGIC; -- serial input ports
29   bmiso : out STD_LOGIC; -- serial output; tri-state!
30   bufcs : in STD_LOGIC; -- selector: buffer output (high) / program (low)
31   -- Board Side
32   bclk, bmosi: out STD_LOGIC_VECTOR (10 downto 0); -- buffered serial output
33   umiso: in STD_LOGIC_VECTOR (10 downto 0); -- serial input
34   mcs: out STD_LOGIC_VECTOR (11 downto 0); -- master chip selects
35   ss0: out STD_LOGIC_VECTOR (1 downto 0);
36   ss1: out STD_LOGIC_VECTOR (1 downto 0);
37   ss2: out STD_LOGIC_VECTOR (1 downto 0);
38   ss3: out STD_LOGIC_VECTOR (1 downto 0);
39   ss4: out STD_LOGIC_VECTOR (1 downto 0);
40   ss5: out STD_LOGIC_VECTOR (1 downto 0);
41   ss6: out STD_LOGIC_VECTOR (1 downto 0);
42   ss7: out STD_LOGIC_VECTOR (1 downto 0);
43   ss8: out STD_LOGIC_VECTOR (1 downto 0);
44   ss9: out STD_LOGIC_VECTOR (1 downto 0)
45     );
46 end SPIBUF_IN;
47
48 architecture Structure of SPIBUF_IN is
49
50 component shift_reg
51     port (
52       ser_ss : out STD_LOGIC_VECTOR (11 downto 0); -- to the outside world (global ↵
53                                                    CS)
54   int_ss: out STD_LOGIC_VECTOR (11 downto 0); -- internal copy of the previous
55   int_coded_ss: out STD_LOGIC_VECTOR (1 downto 0); -- coded cs for internal use (↵
56                                                    diverted to output buffers)
57       ser_in  : in  STD_LOGIC; -- mosi from controller
58       ser_out : out  STD_LOGIC; -- miso towards controller
59       clock : in  STD_LOGIC; -- serial clock from controller
60       ss_en : in STD_LOGIC -- active low
61     );
```

```
62 end component;
63
64 component spi_fanout
65     port (
66   sclk: out STD_LOGIC; -- clock out
67   mclk: in STD_LOGIC; -- clock in
68   sdo : out STD_LOGIC; -- mosi out
69   mosi : in STD_LOGIC; -- mosi in
70   ssa: in STD_LOGIC; -- slave select global selector (active-low)
71   coded_cs_in0: in STD_LOGIC;
72   coded_cs_in1: in STD_LOGIC;
73   coded_cs_buf: out STD_LOGIC_VECTOR (1 downto 0)
74   );
75 end component;
76
77 component miso_mux
78     port (
79   sel0,sel1,sel2,sel3,sel4,sel5,sel6,sel7,sel8,sel9,sel10 : in STD_LOGIC; -- ↩
80   Selectors (active-low, last two are together)
81   sin: in STD_LOGIC_VECTOR (10 downto 0); -- MISO from all the devices
82   sout: out STD_LOGIC -- Selected MISO
83   );
84 end component;
85
86 signal chipsel: STD_LOGIC_VECTOR (11 downto 0); --internal chip select signal
87 signal coded_chipsel: STD_LOGIC_VECTOR (1 downto 0); --internal coded chipsel
88 signal tia_selector: STD_LOGIC; -- handles the two chip selects for the ↩
89 transimpedance amplifier
90
91 begin
92     tia_selector <= chipsel(10) and chipsel(11); --assign master chip selects 10 and ↩
93                     11 to the transimpedance amplifier
94     -- shift register
95     SREG : shift_reg port map (mcs, chipsel, coded_chipsel, umosi, bmiso, uclk, ↩
96                                bufcs);
97     -- MISO multiplexer
98     MUX: miso_mux port map (chipsel(0),chipsel(1),chipsel(2),chipsel(3),chipsel(4), ↩
99                             chipsel(5),chipsel(6),chipsel(7),chipsel(8),chipsel(9), ↩
100                            tia_selector, umiso, bmiso);
101    -- SPI buffers
102    SBUF0 : spi_fanout port map(bclk(0), uclk, bmosi(0), umosi, chipsel(0), ↩
103                                coded_chipsel(0), coded_chipsel(1), ss0);
104    SBUF1 : spi_fanout port map(bclk(1), uclk, bmosi(1), umosi, chipsel(1), ↩
105                                coded_chipsel(0), coded_chipsel(1), ss1);
106    SBUF2 : spi_fanout port map(bclk(2), uclk, bmosi(2), umosi, chipsel(2), ↩
107                                coded_chipsel(0), coded_chipsel(1), ss2);
108    SBUF3 : spi_fanout port map(bclk(3), uclk, bmosi(3), umosi, chipsel(3), ↩
109                                coded_chipsel(0), coded_chipsel(1), ss3);
110    SBUF4 : spi_fanout port map(bclk(4), uclk, bmosi(4), umosi, chipsel(4), ↩
111                                coded_chipsel(0), coded_chipsel(1), ss4);
112    SBUF5 : spi_fanout port map(bclk(5), uclk, bmosi(5), umosi, chipsel(5), ↩
113                                coded_chipsel(0), coded_chipsel(1), ss5);
114    SBUF6 : spi_fanout port map(bclk(6), uclk, bmosi(6), umosi, chipsel(6), ↩
115                                coded_chipsel(0), coded_chipsel(1), ss6);
116    SBUF7 : spi_fanout port map(bclk(7), uclk, bmosi(7), umosi, chipsel(7), ↩
117                                coded_chipsel(0), coded_chipsel(1), ss7);
118    SBUF8 : spi_fanout port map(bclk(8), uclk, bmosi(8), umosi, chipsel(8), ↩
119                                coded_chipsel(0), coded_chipsel(1), ss8);
120    SBUF9 : spi_fanout port map(bclk(9), uclk, bmosi(9), umosi, chipsel(9), ↩
121                                coded_chipsel(0), coded_chipsel(1), ss9);
122    SBUF10 : spi_fanout port map(bclk(10), uclk, bmosi(10), umosi, tia_selector, ↩
```

```
123                                     coded_chipsel(0), coded_chipsel(1), open);
124 end Structure;
125
126 ----------------------------------------------------------------------
127 ----------------------------------------------------------------------
128 library IEEE;
129 use IEEE.STD_LOGIC_1164.ALL;
130 use IEEE.STD_LOGIC_ARITH.ALL;
131 use IEEE.STD_LOGIC_UNSIGNED.ALL;
132
133 ----------------------------------------
134 -- NOTE: Shift register is loaded MSB first
135 ----------------------------------------
136
137 entity shift_reg is
138     Port (
139     ser_ss : out STD_LOGIC_VECTOR (11 downto 0);
140         int_ss: out STD_LOGIC_VECTOR (11 downto 0); -- internal copy of the ↩
141                                                 previous
142         int_coded_ss: out STD_LOGIC_VECTOR (1 downto 0); -- coded cs for internal ↩
143                                                     use (diverted to output buffers)
144     ser_in  : in  STD_LOGIC; -- mosi from controller
145     ser_out : out  STD_LOGIC; -- miso towards controller
146     clock : in  STD_LOGIC; -- serial clock from controller
147     ss_en : in STD_LOGIC -- active low
148         );
149 end shift_reg;
150
151 architecture Behavioral of shift_reg is
152 signal int_ss_addr_reg : STD_LOGIC_VECTOR (5 downto 0); -- immission register
153 signal ss_addr : STD_LOGIC_VECTOR (5 downto 0); -- actual register
154 signal ss_reg_out : STD_LOGIC;
155 signal ss_dec_reg: STD_LOGIC_VECTOR (11 downto 0);
156 begin
157
158 process (clock)
159 begin
160   if clock'event and clock = '1' then
161       if ss_en = '0' then
162       int_ss_addr_reg <= int_ss_addr_reg(4 downto 0) & ser_in;
163       end if;
164   end if;
165 end process;
166
167 process (clock)
168 begin
169   if clock'event and clock = '0' then
170       if ss_en = '0' then
171       ss_reg_out <= int_ss_addr_reg(5); -- puts out the last bit
172       end if;
173   end if;
174 end process;
175
176 process (ss_en)
177 begin
178     if ss_en'event and ss_en = '1' then
179   ss_addr <= int_ss_addr_reg; -- writes to register
180   end if;
181 end process;
182
183     -- 6 bit decoder here:
```

```
184     ss_dec_reg <= "111111111110" when ss_addr = "0000--" else
185     "111111111101" when ss_addr = "0001--" else
186     "111111111011" when ss_addr = "0010--" else
187     "111111110111" when ss_addr = "0011--" else
188     "111111101111" when ss_addr = "0100--" else
189     "111111011111" when ss_addr = "0101--" else
190     "111110111111" when ss_addr = "0110--" else
191     "111101111111" when ss_addr = "0111--" else
192     "111011111111" when ss_addr = "1000--" else
193     "110111111111" when ss_addr = "1001--" else
194     "101111111111" when ss_addr = "1010--" else
195     "011111111111" when ss_addr = "1011--" else
196     "111111111111";
197     -- ends decoder
198
199     -- output ss is active only when shift register deselected
200     ser_ss <= ss_dec_reg when ss_en='1' else "111111111111";
201     int_ss <= ss_dec_reg when ss_en='1' else "111111111111";
202     int_coded_ss(0) <= ss_addr(0);
203     int_coded_ss(1) <= ss_addr(1);
204
205   ser_out <= ss_reg_out when  ss_en ='0' else 'Z'; -- internally connected to other
206               MISO
207 end Behavioral;
208
209
210 --- Single-Channel Buffered Output
211 library IEEE;
212 use IEEE.STD_LOGIC_1164.ALL;
213 use IEEE.STD_LOGIC_ARITH.ALL;
214 use IEEE.STD_LOGIC_UNSIGNED.ALL;
215
216 entity spi_fanout is
217     Port (
218   sclk: out STD_LOGIC; -- clock out
219   mclk: in STD_LOGIC; -- clock in
220   sdo : out STD_LOGIC; -- mosi out
221   mosi : in STD_LOGIC; -- mosi in
222   ssa: in STD_LOGIC; -- slave select global selector (active-low)
223   coded_cs_in0: in STD_LOGIC;
224   coded_cs_in1: in STD_LOGIC;
225   coded_cs_buf: out STD_LOGIC_VECTOR (1 downto 0)
226     );
227 end spi_fanout;
228
229 architecture Behavioral of spi_fanout is
230     begin
231     sclk <= mclk when ssa='0' else '0';
232     sdo <= mosi when ssa='0' else '0';
233     coded_cs_buf(0) <= coded_cs_in0; -- these two may be always-on
234     coded_cs_buf(1) <= coded_cs_in1;
235 end Behavioral;
236
237 ----------------------------------------------------------------------------
238
239 library IEEE;
240 use IEEE.STD_LOGIC_1164.ALL;
241 use IEEE.STD_LOGIC_ARITH.ALL;
242 use IEEE.STD_LOGIC_UNSIGNED.ALL;
243
244 entity miso_mux is
```

```
245     port (
246   sel0,sel1,sel2,sel3,sel4,sel5,sel6,sel7,sel8,sel9,sel10 : in STD_LOGIC; -- )
247   Selectors (active-low, last two are together)
248   sin: in STD_LOGIC_VECTOR (10 downto 0); -- MISO from all the devices
249   sout: out STD_LOGIC -- Selected MISO
250   );
251 end miso_mux;
252
253 architecture Behavioral of miso_mux is
254 begin
255     sout <= sin(0) when sel0='0' else
256   sin(1) when sel1='0' else
257   sin(2) when sel2='0' else
258   sin(3) when sel3='0' else
259   sin(4) when sel4='0' else
260   sin(5) when sel5='0' else
261   sin(6) when sel6='0' else
262   sin(7) when sel7='0' else
263   sin(8) when sel8='0' else
264   sin(9) when sel9='0' else
265   sin(10) when sel10='0' else
266   'Z';
267 end Behavioral;
```

SPI CONFIGURATION COMMANDS

D

MAX7301 SPI programming for Channel Configuration (36 pin SSOP version)				
Power-on state:	All ports set to input Hi-Z			
Coded chip select:	MSB	0	0	LSB

16 bit shift register Write MSB first CPOL=0 CPHA=0

Port	Function	Command Byte								Data Byte								Notes	Active
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
P5	Set logic output	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	M	Amplifier: Gain 2	High
P6	Set logic output	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	M	Amplifier: Gain 10	High
P7	Set logic output	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	M	Amplifier: Gain 50	High
P8	Set logic output	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	M	Amplifier: Gain 100	High
P9	Set logic output	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	M	Amplifier: Gain XX02	High
P10	Set logic output	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	M	Amplifier: Gain 1000	High
P11	Set logic output	0	0	1	0	1	0	1	1	0	0	0	0	0	0	0	M	Bypass Channel	High
P12	Set logic output	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	M	Amplifier Shutdown	High
P13	Set logic output	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	M	Calibration Reset	Low
P14	Set logic output	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	M	Amplifier: Gain XX01	High
P15	Set logic output	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	M	Amplifier: Gain 200	High
P16	Set logic output	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	M	Amplifier: Gain 20	High
P17	Set logic output	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	M	Amplifier: Gain 5	High
P24	Set logic output	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	M	Attach Calibrator	High
P25	Set logic output	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	M	Short Input Signal	High
P27	Set logic output	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	M	Attach Attenuator	High
P28	Set logic output	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	M	Bypass Attenuator	High
P29	Set logic output	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	M	Attenuator: Gain 1/10	High
P30	Set logic output	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	M	Attenuator: Gain 1/5	High
P31	Set logic output	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	M	Attenuator: Gain 1/2	High
P7-P4	Port Configuration	0	0	0	0	1	0	0	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P11-P8	Port Configuration	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P15-P12	Port Configuration	0	0	0	0	1	0	1	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P19-P16	Port Configuration	0	0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P23-P20	Port Configuration	0	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P27-P24	Port Configuration	0	0	0	0	1	1	1	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P31-P28	Port Configuration	0	0	0	0	1	1	1	1	0	1	0	1	0	1	0	1	Set ports to GPO	

MCP23S08 SPI programming					
Power-on state:	All ports set to input Hi-Z, pin hardware addressing disabled (D18 and D17 are 0.				
Coded chip select:	MSB	1	1	LSB	

24 bit shift register Write MSB first CPOL=0 CPHA=0

		Device Opcode (Fixed)							R/W	Register Address								Data Byte								
Port	**Function**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Notes**
GP7-GP0	Set logic output	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	
GP7-GP0	Set ports to GPO	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Mandatory set-up

Port	**Function**	**Act.**
GP7	Unused	
GP6	Unused	
GP5	Unused	
GP4	Enable Mid-Voltage Range (20V~2V)	High
GP3	Enable Low-Voltage Range (2V~0.2V)	High
GP2	Enable Tiny-Voltage Range (0.2V~0.02V)	High
GP1	Enable High-Voltage Range (200V~20V)	High
GP0	Reset Gain Adjustment	Low

AD5293 SPI programming					
Power-on state:	RDAC set to 0x200, 2ms turn-on time				
Coded chip select: Calibration	MSB	0	1	LSB	3 daisy-chained potentiometers: word size is 48 bits.
Coded chip select: Bucking	MSB	1	0	LSB	1 potentiometer: word size is 16 bits.

16 bit shift register Write MSB first CPOL=0 CPHA=1

Function	Command Byte						RDAC Data										Notes
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Unlock RDAC register	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	Mandatory
Program RDAC	0	0	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0x0000 connects W to B
Prepare RDAC for reading	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Wait 450ns for set-up after this
Clock out RDAC register	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NOP: MISO out clocking

MAX7301 SPI programming for Transimpedance Amplifier Configuration (28 pin SSOP)	
Power-on state:	All ports set to input Hi-Z

16 bit shift register Write MSB first CPOL=0 CPHA=0

Port	Function	Command Byte								Data Byte								Notes	Active
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
P12	Set logic output	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	M	TIA: Gain 1	High
P13	Set logic output	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	M	TIA: Gain 2	High
P14	Set logic output	0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	M	TIA: Gain 5	High
P15	Set logic output	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	M	TIA: Gain 10	High
P16	Set logic output	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	M	TIA: Gain 20	High
P17	Set logic output	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	M	TIA: Gain 50	High
P18	Set logic output	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	M	TIA: Gain 100	High
P19	Set logic output	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	M	Multiplexer A2 (15)	Coded
P20	Set logic output	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	M	Multiplexer A1 (16)	Coded
P21	Set logic output	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	M	Multiplexer A0 (1)	Coded
P22	Set logic output	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	M	Calibration Reset	Low
P7-P4	Port Configuration	0	0	0	0	1	0	0	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P11-P8	Port Configuration	0	0	0	0	1	0	1	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P15-P12	Port Configuration	0	0	0	0	1	0	1	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P19-P16	Port Configuration	0	0	0	0	1	1	0	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P23-P20	Port Configuration	0	0	0	0	1	1	0	1	0	1	0	1	0	1	0	1	Set ports to GPO	
P27-P24	Port Configuration	0	0	0	0	1	1	1	0	0	1	0	1	0	1	0	1	Set ports to GPO	
P31-P28	Port Configuration	0	0	0	0	1	1	1	1	0	1	0	1	0	1	0	1	Set ports to GPO	

PCA9703 SPI Programming	
Power-on state:	All interrupts masked

16 bit shift register Write MSB first CPOL=0 CPHA=1

Port	Function	Command																Notes
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
All	Enable interrupts	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Clock this in when reading the status
All	Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Clears mask and status

XC95144 SPI Buffer Programming	
Power-on state:	Unknown

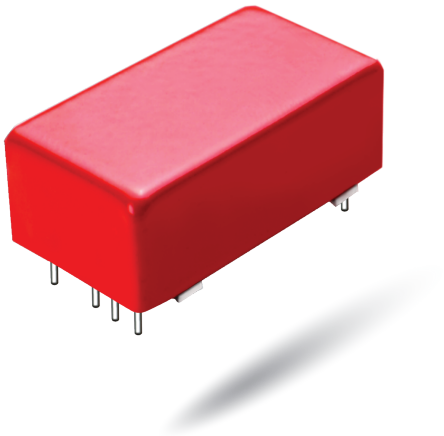
6 bit shift register | Write MSB first | CPOL=0 | CPHA=0

Port	Function	Command Byte								Notes
		D15	D14	D13	D12	D11	D10	D9	D8	
P0	Set logic output	X	X	0	0	0	0	SS1	SS0	Attach Channel 1
P1	Set logic output	X	X	0	0	0	1	SS1	SS0	Attach Channel 2
P2	Set logic output	X	X	0	0	1	0	SS1	SS0	Attach Channel 3
P3	Set logic output	X	X	0	0	1	1	SS1	SS0	Attach Channel 4
P4	Set logic output	X	X	0	1	0	0	SS1	SS0	Attach Channel 5
P5	Set logic output	X	X	0	1	0	1	SS1	SS0	Attach Channel 6
P6	Set logic output	X	X	0	1	1	0	SS1	SS0	Attach Channel 7
P7	Set logic output	X	X	0	1	1	1	SS1	SS0	Attach Channel 8
P8	Set logic output	X	X	1	0	0	0	SS1	SS0	Attach Channel 9
P9	Set logic output	X	X	1	0	0	1	SS1	SS0	Attach Channel 10
TIA	Set logic output	X	X	1	0	1	0	SS1	SS0	Tia Gain Control
TIA	Port Configuration	X	X	1	0	1	1	SS1	SS0	TIA Offset Calibration
	Disable Buffer	X	X	1	1	1	1	SS1	SS0	This will put MISO in Hi-Z

E

DATASHEETS

3600 SERIES/LOW THERMAL EMF REED RELAYS



3600 Series Low Thermal EMF Reed Relays

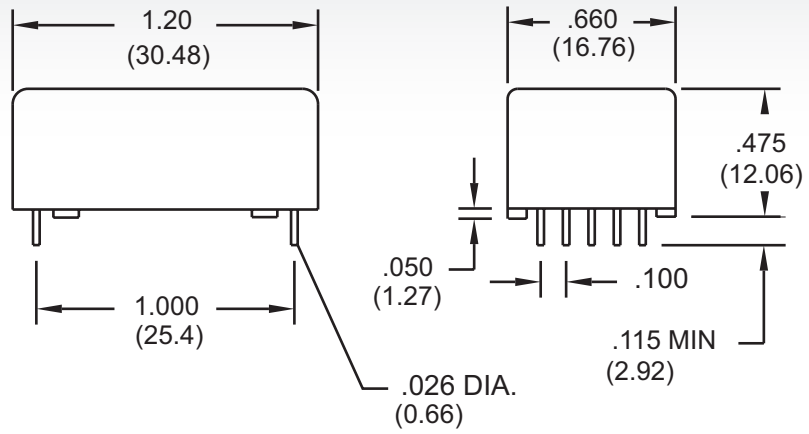
The 3600 Series is ideally suited to the needs of Instrumentation, Data Acquisition, and Process Control. The specification tables allow you to select the appropriate relay for your particular application. Recommended for use in Scanners, Multiplexers and Digital or Analog Multipoint Recorders. If your requirements differ from the selection options, please consult Coto's Factory to discuss a custom reed relay.

3600 Series Features

- Low Thermal EMF: < 5 µV through < 0.5 µV with 50 nV stability
- Patented Low Thermal Design. U.S. Patent #4,084,142
- Low power coils to ensure low thermal EMF
- High Insulation Resistance - $10^{12}\Omega$
- Control/Signal isolation of 1500 VDC
- High speed switching compared to electromechanical relays
- High reliability, hermetically sealed contacts
- Various Form A contacts. High Dielectric Strength
- Epoxy coated steel shell provides magnetic shielding
- Electrostatic shield standard for reducing capacitive coupling
- RoHS compliant

DIMENSIONS

in Inches (Millimeters)



Bottom View

Ordering Information

Part Number XXXX-XX-X2

Model Number
3602 3650 3660

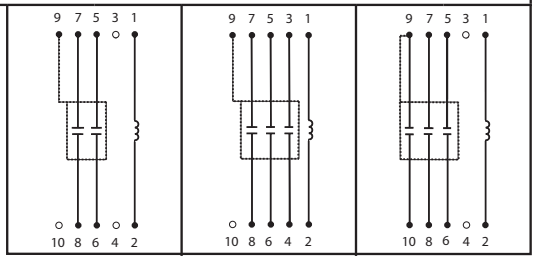
Coil Voltage
05=5 volts
12=12 volts

Thermal EMF Rating
See available ratings in specification table.
9=<5µV
8=<3µV
7=<1µV
5=<0.5µV

tel: (401) 943.2686 | fax: (401) 942.0920

MODELNUMBER			3602	3650[3]	3660[2]
Parameters	**Test Conditions**	**Units**	**2 Form A**	**3 Form A**	**3 Form A**
Thermal EMF Options	Measured after 5 minutes at nominal coil voltage (Refer to Reed Relay Technical Section for details)	µV	Individual <5µV <3µV <1µV <0.5µV	Differential <5µV <3µV <1µV <0.5µV	Differential <5µV <3µV <1µV <0.5µV
COIL SPECS.					
Nom. Coil Voltage		VDC	5 12	5 12	5 12
Coil Resistance	+/- 10%, 25° C	Ω	350 2000	350 2000	350 2000
Operate Voltage	Must Operate by	VDC - Max.	3.8 9.0	3.8 9.0	3.8 9.0
Release Voltage	Must Release by	VDC - Min.	0.4 1.0	0.4 1.0	0.4 1.0
CONTACT RATINGS					
Switching Voltage	Max DC/Peak AC Resist.	Volts	150	150	150
Switching Current	Max DC/Peak AC Resist.	Amps	0.25	0.25	0.25
Carry Current	Max DC/Peak AC Resist.	Amps	1.5	1.5	1.5
Contact Rating	Max DC/Peak AC Resist.	Watts	5	5	5
Life Expectancy-Typical[1]	Signal Level 1.0V, 10mA	x 10^6 Ops.	500	500	500
Static Contact Resistance (max. init.)	50mV, 10mA	Ω	0.100	0.100	0.100
Dynamic Contact Resistance (max. init.)	0.5V, 50mA at 100 Hz, 1.5 msec	Ω	0.200	0.200	0.200
RELAY SPECIFICATIONS					
Insulation Resistance (minimum)	Between all Isolated Pins at 100V, 25°C, 40% RH	Ω	10^{12}	10^{12}	10^{12}
Capacitance - Typical Across Open Contacts Contact to Shield	Shield Floating Shield Guarding Contacts Open Shield & Coil Tied Common	pF pF pF pF	1.2 0.2 2.5 2.5	1.2 0.2 2.5 2.5	1.2 0.2 2.5 2.5
Dielectric Strength (minimum)	Between Contacts Contacts to Shield Contacts/Shield to Coil	VDC/peak AC VDC/peak AC VDC/peak AC	250 1000 1500	250 1000 1500	250 1000 1500
Operate Time - including bounce - Typical	At Nominal Coil Voltage, 30 Hz Square Wave	msec.	0.75	0.75	0.75
Release Time - Typical		msec.	0.1	0.1	0.1

Top View:
Grid = .1"x.1" (2.54mm x 2.54mm)



Notes:

[1] Consult factory for life expectancy at other switching loads.

[2] Model 3660: Reed switch between pins #9 & #10 is not low thermal and is tied in common with the electrostatic shield.

[3] Model 3650: Reed switch between pins #3 & #4 is not low thermal and is not tied in common with the electrostatic shield. Pin numbers for reference only.

Environmental Ratings:

Storage Temp: -35°C to +100°C; *Operating Temp:* -20°C to +85°C; *Solder Temp:* 270°C max; 10 sec. max
All electrical parameters measured at 25°C unless otherwise specified.
Vibration: 20 G's to 2000 Hz; *Shock:* 50 G's

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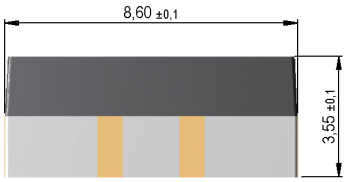
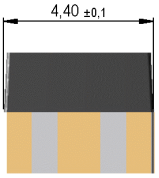
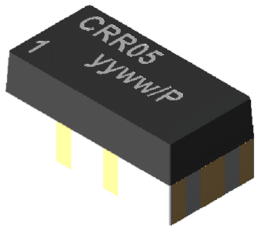
Item No.:
9605180012
Item:
CRR05-1A

Dimensions mm[inch]
tolerances acc. to DIN ISO 2768-m
Toleranzen gem. DIN ISO 2768-m

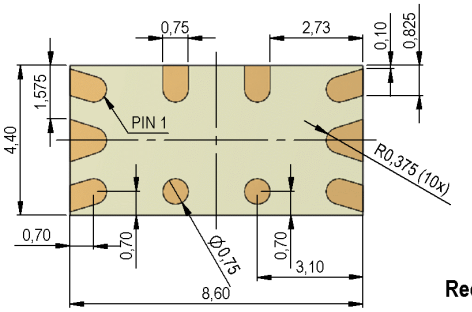




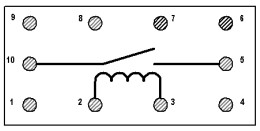
Isometric
Scale 5:1
Maßstab 5:1



Relay pad layout
Bottom view
Ansicht von unten

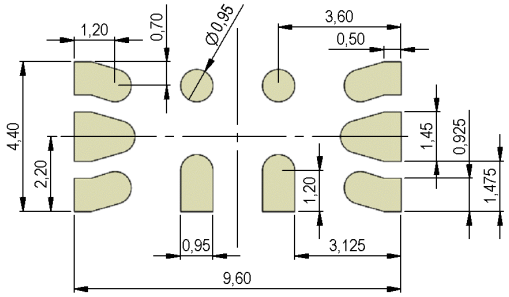


Schematic
Top view
Draufsicht



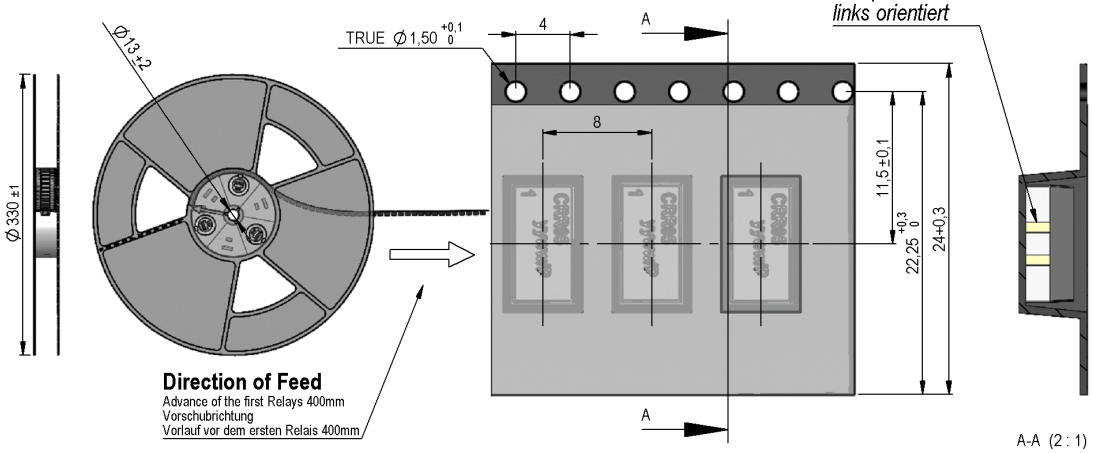
Marking
according to EN60062/factory code
gem. EN60062/Fertigungsstätte

Recommended PCB Pad Layout
top view / *Ansicht von oben*



Relay packaging orientation

Gold pads facing to the left
Goldpads nach links orientiert



Direction of Feed
Advance of the first Relays 400mm
Vorschubrichtung
Vorlauf vor dem ersten Relais 400mm

Modifications in the sense of technical progress are reserved

Designed at:	07.12.09	Designed by:	MAPODACA	Approval at:	21.07.11	Approval by:	CRUF	
Last Change at:	06.09.11	Last Change by:	CRUF	Approval at:	06.09.11	Approval by:	CRUF	**Version:** 05

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Item No.:
9605180012
Item:
CRR05-1A

Coil Data at 20 °C	Conditions	Min	Typ	Max	Unit
Coil resistance		135	150	165	Ohm
Coil voltage			5		VDC
Rated power			167		mW
Pull-In voltage				3,75	VDC
Drop-Out voltage		0,75			VDC

Contact data 80/1	Conditions	Min	Typ	Max	Unit
Contact-No.		80/1			
Contact-form		A			
Contact rating	Any DC combination of V & A			10	W
Switching voltage	DC or Peak AC			170	V
Switching current	DC or Peak AC			0,5	A
Carry current	DC or Peak AC			1	A
Contact resistance static	Measured with 40% overdrive			200	mOhm
Insulation resistance	RH <45 %, 100 V test voltage	1	10		GOhm
Breakdown voltage	according to IEC 255-5	210			VDC
Operate time incl. bounce	measured with 40% overdrive			0,6	ms
Release	measured with no coil excitation			0,05	ms
Capacity	@ 10 kHz across open switch		0,4		pF

Special Product Data	Conditions	Min	Typ	Max	Unit
Number of contacts		1			
Contact - form		A - NO			
Dielectric Strength Coil/Contact	according to EN 60255-5	1,5			kV DC
Insulation resistance Coil/Contact	RH <45%, 200 VDC measuring voltage	10	100		TOhm
Case color		black/white			
Housing material		Ceramic + mineral filled epoxy			
Material conection pads		W, Ni, gold plated			
Reach / RoHS conformity		yes			

Environmental data	Conditions	Min	Typ	Max	Unit
Shock	1/2 sine, duration 11ms, in 3 axis			50	g
Vibration	from 10 - 2000 Hz			20	g
Operating temperature		-40		125	°C
Storage temperature		-55		125	°C
Soldering Temperature Tsold	Reflow according IPC/JEDEC J-STD-0			260	°C
Washability		fully sealed			

General data	Conditions	Min	Typ	Max	Unit
Total weigth			0,37		g
Packaging		Tape & Reel / 1000 pcs.			

High-Performance, Fully-Differential AUDIO OPERATIONAL AMPLIFIER

Check for Samples: OPA1632

FEATURES

- **SUPERIOR SOUND QUALITY**
- **ULTRA LOW DISTORTION: 0.000022%**
- **LOW NOISE: 1.3nV/√Hz**
- **HIGH SPEED:**
  - **Slew Rate: 50V/μs**
  - **Gain Bandwidth: 180MHz**
- **FULLY DIFFERENTIAL ARCHITECTURE:**
  - **Balanced Input and Output Converts Single-Ended Input to Balanced Differential Output**
- **WIDE SUPPLY RANGE: ±2.5V to ±16V**
- **SHUTDOWN TO CONSERVE POWER**

APPLICATIONS

- **AUDIO ADC DRIVER**
- **BALANCED LINE DRIVER**
- **BALANCED RECEIVER**
- **ACTIVE FILTER**
- **PREAMPLIFIER**

DESCRIPTION

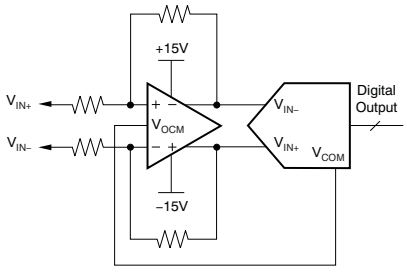
The OPA1632 is a fully-differential amplifier designed for driving high-performance audio analog-to-digital converters (ADCs). It provides the highest audio quality, with very low noise and output drive characteristics optimized for this application. The OPA1632's excellent gain bandwidth of 180MHz and very fast slew rate of 50V/μs produce exceptionally low distortion. Very low input noise of 1.3nV/√Hz further ensures maximum signal-to-noise ratio and dynamic range.

The flexibility of the fully differential architecture allows for easy implementation of a single-ended to fully-differential output conversion. Differential output reduces even-order harmonics and minimizes common-mode noise interference. The OPA1632 provides excellent performance when used to drive high-performance audio ADCs such as the PCM1804. A shutdown feature also enhances the flexibility of this amplifier.

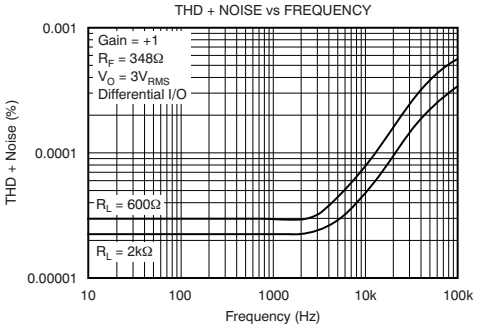
The OPA1632 is available in an SO-8 package and a thermally-enhanced MSOP-8 PowerPAD™ package.

RELATED PRODUCTS

PRODUCT	DESCRIPTION
OPAx134	High-Performance Audio Amplifiers
OPA627/OPA637	Precision High-Speed DiFET Amplifiers
OPAx227/OPAx228	Low-Noise Bipolar Amplifiers



Typical ADC Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

High-Precision, Low-Noise, Rail-to-Rail Output, 11MHz JFET Op Amp

Check for Samples: OPA140, OPA2140, OPA4140

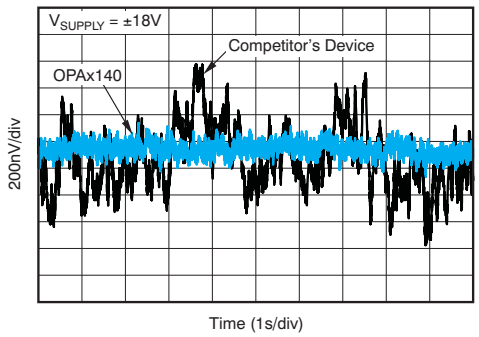
FEATURES

- **Very Low Offset Drift: 1μV/°C max**
- **Very Low Offset: 120μV**
- **Low Input Bias Current: 10pA max**
- **Very Low 1/f Noise: 250nV$_{PP}$, 0.1Hz to 10Hz**
- **Low Noise: 5.1nV/√Hz**
- **Slew Rate: 20V/μs**
- **Low Supply Current: 2.0mA max**
- **Input Voltage Range Includes V– Supply**
- **Single-Supply Operation: 4.5V to 36V**
- **Dual-Supply Operation: ±2.25V to ±18V**
- **No Phase Reversal**
- **Industry-Standard SO Packages**
- **MSOP-8, TSSOP, and SOT23 Packages**

APPLICATIONS

- **Battery-Powered Instruments**
- **Industrial Controls**
- **Medical Instrumentation**
- **Photodiode Amplifiers**
- **Active Filters**
- **Data Acquisition Systems**
- **Automatic Test Systems**

0.1Hz to 10Hz NOISE



DESCRIPTION

The OPA140, OPA2140, and OPA4140 op amp family is a series of low-power JFET input amplifiers that feature good drift and low input bias current. The rail-to-rail output swing and input range that includes V– allow designers to take advantage of the low-noise characteristics of JFET amplifiers while also interfacing to modern, single-supply, precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

The OPA140 achieves 11MHz unity-gain bandwidth and 20V/μs slew rate while consuming only 1.8mA (typ) of quiescent current. It runs on a single 4.5 to 36V supply or dual ±2.25V to ±18V supplies.

All versions are fully specified from –40°C to +125°C for use in the most challenging environments. The OPA140 (single) is available in the SOT23-5, MSOP-8, and SO-8 packages; the OPA2140 (dual) is available in both MSOP-8 and SO-8 packages; and the OPA4140 (quad) is available in the SO-14 and TSSOP-14 packages.

RELATED PRODUCTS

FEATURES	PRODUCT
Low-Power, 10MHz FET Input Industrial Op Amp	OPA141
2.2nV/√Hz, Low-Power, 36V Operational Amplifier in SOT23 Package	OPA209
Low-Noise, High-Precision, 22MHz, 4nV/√Hz JFET-Input Operational Amplifier	OPA827
Low-Noise, Low I_O Precision CMOS Operational Amplifier	OPA376
High-Speed, FET-Input Operational Amplifier	OPA132

High Performance, 145 MHz *FastFET* Op Amps

AD8065/AD8066

FEATURES

Qualified for automotive applications
FET input amplifier
1 pA input bias current
Low cost
High speed: 145 MHz, −3 dB bandwidth (G = +1)
180 V/µs slew rate (G = +2)
Low noise
  7 nV/√Hz (f = 10 kHz)
  0.6 fA/√Hz (f = 10 kHz)
Wide supply voltage range: 5 V to 24 V
Single-supply and rail-to-rail output
Low offset voltage 1.5 mV maximum
High common-mode rejection ratio: −100 dB
Excellent distortion specifications
SFDR −88 dBc @ 1 MHz
Low power: 6.4 mA/amplifier typical supply current
No phase reversal
Small packaging: SOIC-8, SOT-23-5, and MSOP-8

APPLICATIONS

Automotive driver assistance systems
Photodiode preamps
Filters
A/D drivers
Level shifting
Buffering

CONNECTION DIAGRAMS

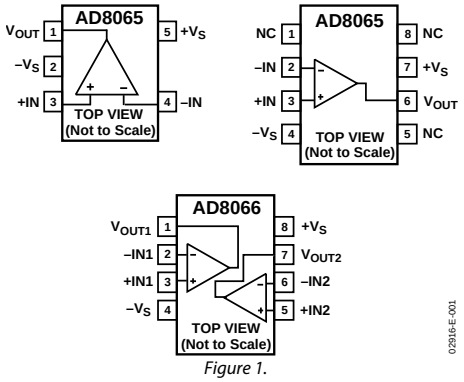


Figure 1.

GENERAL DESCRIPTION

The AD8065/AD8066[1] *FastFET*™ amplifiers are voltage feedback amplifiers with FET inputs offering high performance and ease of use. The AD8065 is a single amplifier, and the AD8066 is a dual amplifier. These amplifiers are developed in the Analog Devices, Inc. proprietary XFCB process and allow exceptionally low noise operation (7.0 nV/√Hz and 0.6 fA/√Hz) as well as very high input impedance.

With a wide supply voltage range from 5 V to 24 V, the ability to operate on single supplies, and a bandwidth of 145 MHz, the AD8065/AD8066 are designed to work in a variety of applications. For added versatility, the amplifiers also contain rail-to-rail outputs.

Despite the low cost, the amplifiers provide excellent overall performance. The differential gain and phase errors of 0.02% and 0.02°, respectively, along with 0.1 dB flatness out to 7 MHz, make these amplifiers ideal for video applications. Additionally, they offer a high slew rate of 180 V/µs, excellent distortion (SFDR of −88 dBc @ 1 MHz), extremely high common-mode rejection of −100 dB, and a low input offset voltage of 1.5 mV maximum under warmed up conditions. The AD8065/AD8066 operate using only a 6.4 mA/amplifier typical supply current and are capable of delivering up to 30 mA of load current.

The AD8065/AD8066 are high performance, high speed, FET input amplifiers available in small packages: SOIC-8, MSOP-8, and SOT-23-5. They are rated to work over the industrial temperature range of −40°C to +85°C.

The AD8065WARTZ-REEL7 is fully qualified for automotive applications. It is rated to operate over the extended temperature range (−40°C to +105°C), up to a maximum supply voltage range of ±5V only.

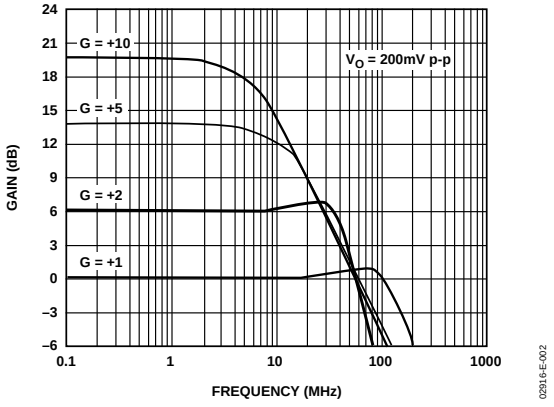


Figure 2. Small Signal Frequency Response

[1] Protected by U. S. Patent No. 6,262,633.

Rev. J

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

Single-Channel, 1024-Position, 1% R-Tolerance Digital Potentiometer

AD5293

FEATURES

- Single-channel, 1024-position resolution
- 20 kΩ, 50 kΩ, and 100 kΩ nominal resistance
- Calibrated 1% nominal resistor tolerance (resistor performance mode)
- Rheostat mode temperature coefficient: 35 ppm/°C
- Voltage divider temperature coefficient: 5 ppm/°C
- Single-supply operation: 9 V to 33 V
- Dual-supply operation: ±9 V to ±16.5 V
- SPI-compatible serial interface
- Wiper setting readback

APPLICATIONS

- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacements
- Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

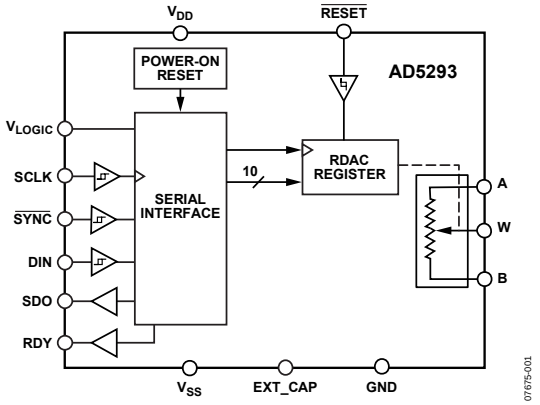


Figure 1.

GENERAL DESCRIPTION

The AD5293 is a single-channel, 1024-position digital potentiometer[1] with a <1% end-to-end resistor tolerance error. The AD5293 performs the same electronic adjustment function as a mechanical potentiometer with enhanced resolution, solid state reliability, and superior low temperature coefficient performance. This device is capable of operating at high voltages and supporting both dual-supply operation at ±10.5 V to ±15 V and single-supply operation at 21 V to 30 V.

The AD5293 offers guaranteed industry-leading low resistor tolerance errors of ±1% with a nominal temperature coefficient of 35 ppm/°C. The low resistor tolerance feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5293 is available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −40°C to +105°C.

[1] In this data sheet, the terms digital potentiometer and RDAC are used interchangeably.

Rev. D

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

LT1012A/LT1012

Picoamp Input Current, Microvolt Offset, Low Noise Op Amp

FEATURES

- OP-07 Type Performance:
  at 1/8th of OP-07's Supply Current
  at 1/20th of OP-07's Bias and Offset Currents
- *Guaranteed* Offset Voltage: 25µV Max
- *Guaranteed* Bias Current: 100pA Max
- *Guaranteed* Drift: 0.6µV/°C Max
- Low Noise, 0.1Hz to 10Hz: 0.5μV_{P-P}
- *Guaranteed* Low Supply Current: 500µA Max
- *Guaranteed* CMRR: 114dB Min
- *Guaranteed* PSRR: 114dB Min
- *Guaranteed* Operation at ±1.2V Supplies

APPLICATIONS

- Replaces OP-07 While Saving Power
- Precision Instrumentation
- Charge Integrators
- Wide Dynamic Range Logarithmic Amplifiers
- Light Meters
- Low Frequency Active Filters
- Thermocouple Amplifiers

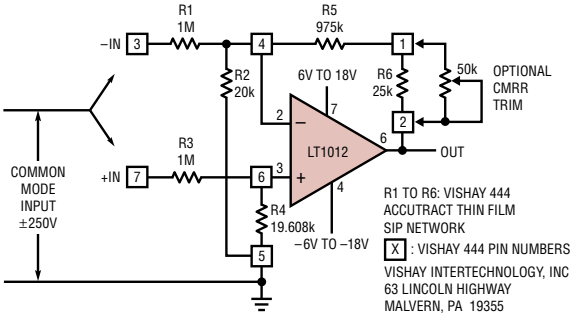
DESCRIPTION

The LT®1012 is an internally compensated universal precision operational amplifier which can be used in practically all precision applications. The LT1012 combines picoampere bias currents (which are maintained over the full –55°C to 125°C temperature range), microvolt offset voltage (and low drift with time and temperature), low voltage and current noise, and low power dissipation. The LT1012 achieves precision operation on two Ni-Cad batteries with 1mW of power dissipation. Extremely high common mode and power supply rejection ratios, practically unmeasurable warm-up drift, and the ability to deliver 5mA load current with a voltage gain of one million round out the LT1012's superb precision specifications.

The all around excellence of the LT1012 eliminates the necessity of the time consuming error analysis procedure of precision system design in many applications; the LT1012 can be stocked as the universal internally compensated precision op amp.

TYPICAL APPLICATION

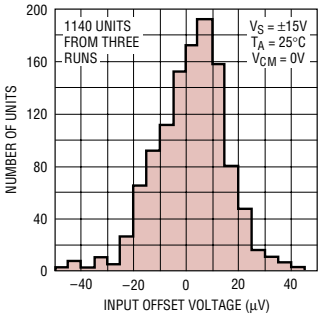
±250V Common Mode Range Instrumentation Amplifier (A_V = 1)



COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
WITH OPTIONAL TRIM = 130dB
OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500µV
OUTPUT OFFSET DRIFT = 10µV/°C
INPUT RESISTANCE = 1M

LT1012A • TA01

Typical Distribution of Input Offset Voltage



LT1012A • TA02

XC95144 In-System Programmable CPLD

DS067 (v5.7) May 28, 2009

Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block (FB)
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3V or 5V I/O capability
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 100-pin PQFP, 100-pin TQFP, and 160-pin PQFP packages

Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95144 device.

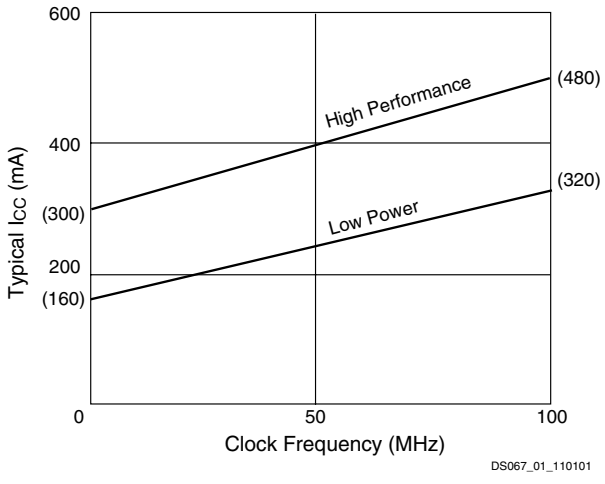


Figure 1: **Typical I_{CC} vs. Frequency for XC95144**

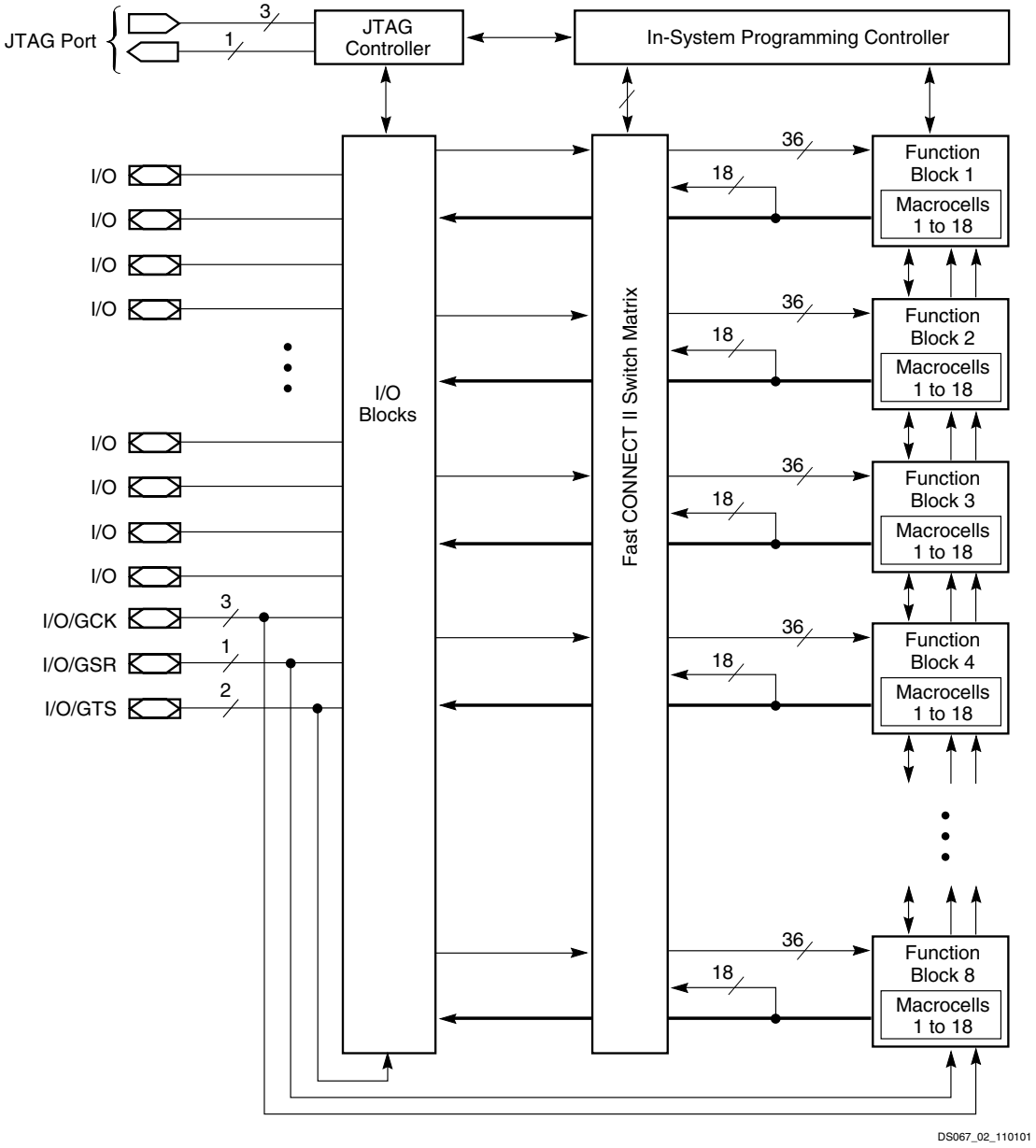
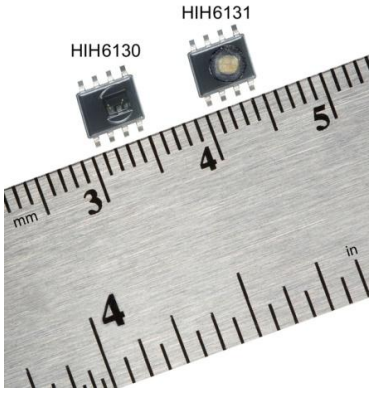


Figure 2: **XC95144 Architecture**
Function block outputs (indicated by the bold line) drive the I/O blocks directly.

Honeywell

Honeywell HumidIcon™ Digital Humidity/Temperature Sensors: HIH6130/6131 Series



DESCRIPTION (★ = *competitive differentiator)*
Honeywell HumidIcon™ Digital Humidity/Temperature Sensors: HIH6130/6131 Series, is a digital output-type relative humidity (RH) and temperature sensor combined in the same package. These devices offer several competitive advantages, including:

- Industry-leading Total Error Band
- Industry-leading stability
- Industry-leading reliability
- Lowest total cost solution
- True temperature-compensated digital I^2C output
- Energy efficiency
- Ultra-small package

★ **Industry-leading Total Error Band (TEB) (±5 %RH):** Honeywell specifies Total Error Band—the most comprehensive, clear, and meaningful measurement –that provides the sensor's true accuracy of ±5 %RH over a compensated range of 5 °C to 50 °C [41 °F to 122 °F] and 10 %RH to 90 %RH. TEB includes all errors due to:

- Humidity non-linearity
- Humidity hysteresis
- Humidity non-repeatability
- Thermal effect on zero
- Thermal effect on span
- Thermal hysteresis

Total Error Band should not be confused with "Accuracy", which is actually a component of Total Error Band. Many competitors simply specify the accuracy of their device; however, the specification may exclude hysteresis and temperature effects, and may be calculated over a very narrow range, at only one point in the range, or at their absolute best accuracy level. It is then up to the customer to calibrate the device to make sure it has the accuracy needed for the life of the application.

Honeywell's industry-leading Total Error Band provides the following benefits to the customer:

- Eliminates individually testing and calibrating every sensor, which can increase their manufacturing time and process
- Supports system accuracy and warranty requirements
- Helps to optimize system uptime
- Provides excellent sensor interchangeability—the customer can remove one sensor from the tape, remove the next sensor from the tape, and there is no part-to-part variation in accuracy

For more information about Total Error Band, please see the related Technical Note "Explanation of the Total Error Band Specification for Honeywell's Digital Humidity/Temperature Sensors."

★ **Industry-leading long term stability (1.2 %RH over five years):** Competitive humidity sensors need to go through a 12 hour at 75 %RH rehydration process (which requires special equipment chambers) to correct reflow temperature offset. Honeywell's sensor also experiences an offset after reflow; however, it only requires a five hour rehydration under ambient conditions (>50 %RH). Honeywell's industry-leading long term stability provides the following benefits to the customer:

- Minimizes system performance issues
- Helps support system uptime by eliminating the need to service or replace the sensor during its application life
- Eliminates the need to regularly recalibrate the sensor in their application, which can be inconvenient and costly

★ **Industry-leading reliability:** Honeywell's new HIH6130/6131 Series sensors use a laser trimmed, thermoset polymer capacitive sensing element. The element's multilayer construction provides resistance to most application hazards such as condensation, dust, dirt, oils, and common environmental chemicals which help provide industry-leading stability and reliability.

Honeywell HumidIcon™ Digital Humidity/Temperature Sensors

★ **Lowest total cost solution:** Offers customers the lowest total cost solution due to the sensor's industry-leading Total Error Band and its being a combined humidity/temperature sensor.

★ **True, temperature-compensated digital I^2C output:** Typically allows the customer to remove the components associated with signal conditioning from the PCB to free up space and reduce costs associated with those components (e.g., acquisition, inventory, assembly). Often eliminates problems that could occur from having multiple signal conditioning components across the PCB. Simplifies integration to the microprocessor, eliminating the need for customer-implemented, complex signal conditioning.

★ **Energy efficient**
- **Low supply voltage:** Can operate down to 2.3 Vdc, which allows use in low energy and wireless-compatible applications to enhance energy savings and prolong system battery life.
- **Low power consumption:** The sensor goes into sleep mode when not taking a measurement within the application, consuming only 1 µA of power versus 650 µA in full operation in a battery operated system. Sleep mode helps maximize battery life, reduces power supply size, and reduces the application's overall weight.

★ **Ultra-small package:** SOIC-8 SMD (Surface Mount Device) package is ultra small, including the condensation-resistant model with hydrophobic filter on-board (HIH6131). Allows for flexibility of use within the application, occupies less space on the PCB, and typically simplifies placement on crowded PCBs or in small devices.

- **Combined humidity and temperature sensor:** The humidity and temperature sensors are co-located in the same package. This allows the RH measurement to be temperature compensated and provides a second, standalone temperature sensor output. This allows the user to purchase one sensor instead of two.

- **Tape and reel packaging:** Cost-effective tape-and-reel packaging allows for use in high volume, automated pick-and-place manufacturing, eliminating lead misalignment to the PCB and helping the customer to reduce manufacturing costs.

- **High resolution:** High 14-bit humidity sensor resolution and 14-bit temperature sensor resolution within the application help the user's system detect the smallest relative humidity or temperature change.

FEATURES AND BENEFITS
- **Wide operating temperature range** of -25 °C to 85 °C [-13 °F to 185 °F] allows for use in many applications
- **Optional one or two %RH level alarm outputs** provide the user the ability to monitor whether the RH level has exceeded or fallen below pre-determined and critical levels within the application
- **Multi-function ASIC** provides flexibility within the application by lowering or eliminating the risk and cost of OEM calibration
- **Industry-standard package** provides easy design-in
- **RoHS and WEEE compliant; halogen-free**
- **Two configurations** increase flexibility of use: HIH6130: no filter, non-condensing; HIH6131: hydrophobic filter and condensation-resistant allow use in many condensing environments

POTENTIAL APPLICATIONS
- **HVAC/R:** May be used to provide precision RH and temperature measurement in air conditioning/air movement systems, enthalpy sensing, thermostats, humidifiers/de-humidifiers, and humidistats to maintain occupant comfort and ideal storage humidity/temperature while achieving low energy consumption, supporting system accuracy and warranty requirements, maximizing system uptime, and improving overall system quality.
- **Respiratory therapy:** May be used to provide precision RH and temperature measurement in sleep apnea machines and ventilators, enhancing patient comfort, safety and treatment effectiveness with warm and humidified air.
- **Incubators/microenvironments:** May be used to provide optimal temperature and RH levels to support critical processes and experiments, enhancing process efficiency with desired climate conditions.
- **Air compressors:** May be used to provide precision RH measurement in compressed air lines, allowing the system to remove any condensation; dry compressed air is critical for customer process control measurement.
- **Weather stations:** May be used to provide precision RH and temperature measurement in ground-based and air-born weather stations, allowing real time and highly accurate monitoring and reporting of actual weather conditions.
- **Telecom cabinets:** May be used to provide precision RH and temperature measurement in the telecom cabinet HVAC system; maintaining proper temperature and humidity levels in the cabinet provides maximum system uptime and performance.

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COLOPHON

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