TN-72-7
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COUNT RATE CONTROL MODULE FOR TSI SCALERS

I. Introduction

A digital count rate meter has several useful functions at SLAC including monitoring of beam rates for central control, etc. A 100 MHz four-channel instrument for this purpose has been developed at SLAC[1] and is available from HEEP. Due to a limited number of units, however, there are rarely enough channels to satisfy needs.

For this reason a count rate control module has been developed which permits the use of conventional TSI scalers as count rate meters. That is, the module generates the proper gate and reset signals on a cyclic basis so that the display indicates the total input pulses during N beam pulses (N = 10, or 100, or 1000), thereby displaying the "average" counts per beam pulse. No display storage is provided, however, as in the Count Rate Meter.

The module drives both standard HEEP scalers 1535, M-71 or M-70, or the older start-stop scalers such as 1511B. Many channels may be driven in parallel, and these may be intermixed among the types mentioned above.

The circuit is packaged in a double width NIM module and includes an internal +5V dc power supply for the IC's to reduce the loading in the +12V NIM supply.

II. Theory of Operation

As opposed to the Count Rate Meter,[1] the count rate control module contains no high speed counting circuits, but utilizes the fast front end of the TSI to do the high speed counting. Conventional IC's are used, except that a complementary pair emitter follower is used to drive the gate, $\overline{\text{gate}}$, and reset cables to the scalers to achieve higher voltage, high speed cable drive. This permits the use of the beam pretrigger as the trigger signal. This pulse is about 700 nsec wide, and precedes the beam by 1 - 2 μsec. It is assumed that the fast discriminators feeding the TSI's are gated by a beam gate.

The complete schematic is shown in Fig. 1. The +10V beam trigger is terminated in 50 Ω and divided by 2. The SP380A has a high impedance input

and a switching point of about +2V, making it a good choice for general interfacing. FF1 is the J-K gate flip-flop which is turned on by the trailing edge of the beam trigger to start a cycle, and turned off by the reset input generated after the Nth beam trigger. The gate G1 enables trigger pulses to the three 8280 decade counters; note that the counters count to 1 after the second beam pulse. When the counters count N beam pulses (N=10 or 100 or 1000) the first one-shot (OS1) triggers by sensing the trailing edge of the corresponding "8" bit. This one-shot generates the internal reset pulse that resets FF1, terminating the count, and resets FF2, the enable gate for the FF1-J input. The TSI counters then hold the display for .5 - 5 seconds as selected by the display time potentiometer.

At the end of the desired display interval the second one-shot (OS2) triggers and generates a 200 μsec reset pulse which is sent to the TSI scalers via a cable driver. A "long" 200 μsec pulse is necessary since the internal reset in some TSI scalers is regenerated to about 100 μsec. At the end of the 200 μsec reset pulse, FF2 is set, enabling the J input of FF1 to re-start the cycle on the trailing edge of the following beam trigger.

If the cycle should stop for any reason it may be restarted by pushing the reset pushbutton.

III. The Cable Driver Circuits

Complementary drivers are used for reset, gate, and $\overline{\text{gate}}$. Note that +12V levels are achieved by the use of open collector SN7401 with pullups to +12V. These circuits are relatively fast and produce clean driving of 50 Ω cable, due primarily to the $\approx 50\ \Omega$ back termination of the cable. Pictures of positive going and negative going edges of the gate signal with 10 feet of RG58C/U are shown in Fig. 2. Note that the overall delay from the trailing edge of the beam trigger is less than 75 nsec.

It is estimated that with 1K input impedance of the M-71 scalers, the module can drive approximately 20 channels.

IV. System Connection

Interconnection of the module and scalers is shown in Fig. 3. Scalers may be intermixed as described before. The discriminators should be beam gated for reduction of background.

V. Acknowledgements

The writer appreciates the suggestions of E. Cisneros in developing the cable driving circuits. Tests on the cable drivers were done by F. Rosche, and construction of the module was done by P. Arechiga. The project was initiated by F. Winkelmann and D. Farwell.

VI. Reference

1. J.-L. Pellegrin, "Operation of a 100 MHz Count-Rate Meter," Report No. SLAC-PUB-661 (1969).

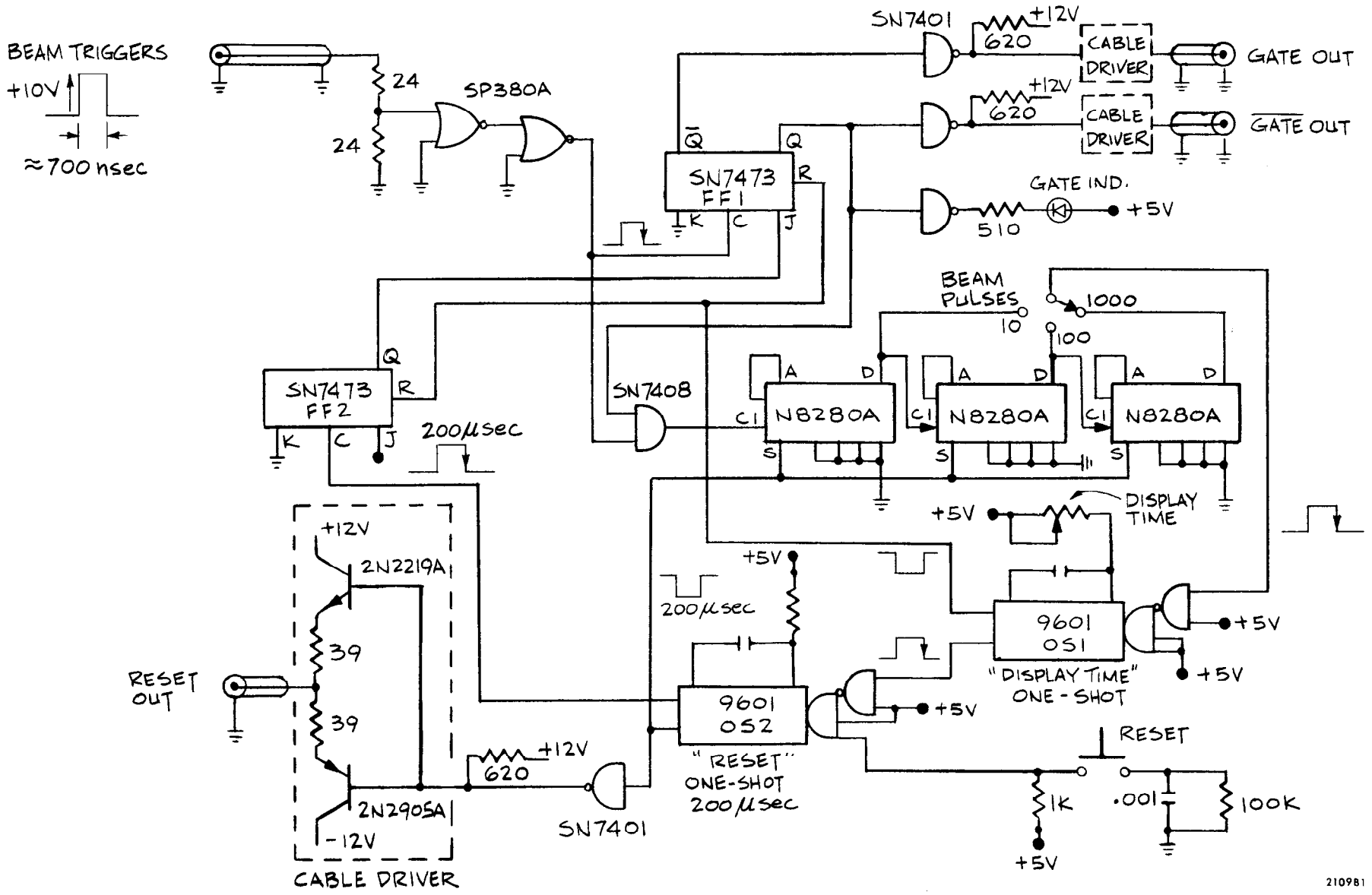
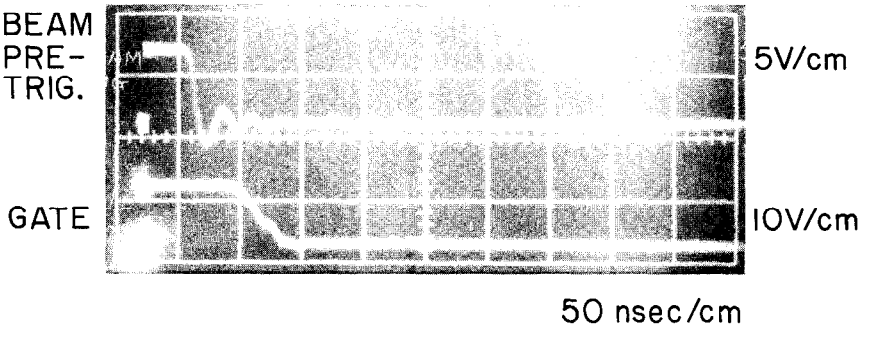
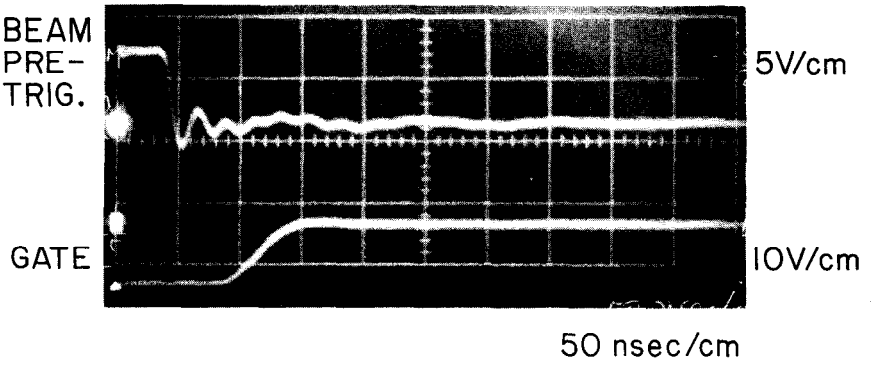


FIG. 1--Schematic of count rate control module.



(a) GATE "OFF" DELAY



(b) GATE "ON" DELAY

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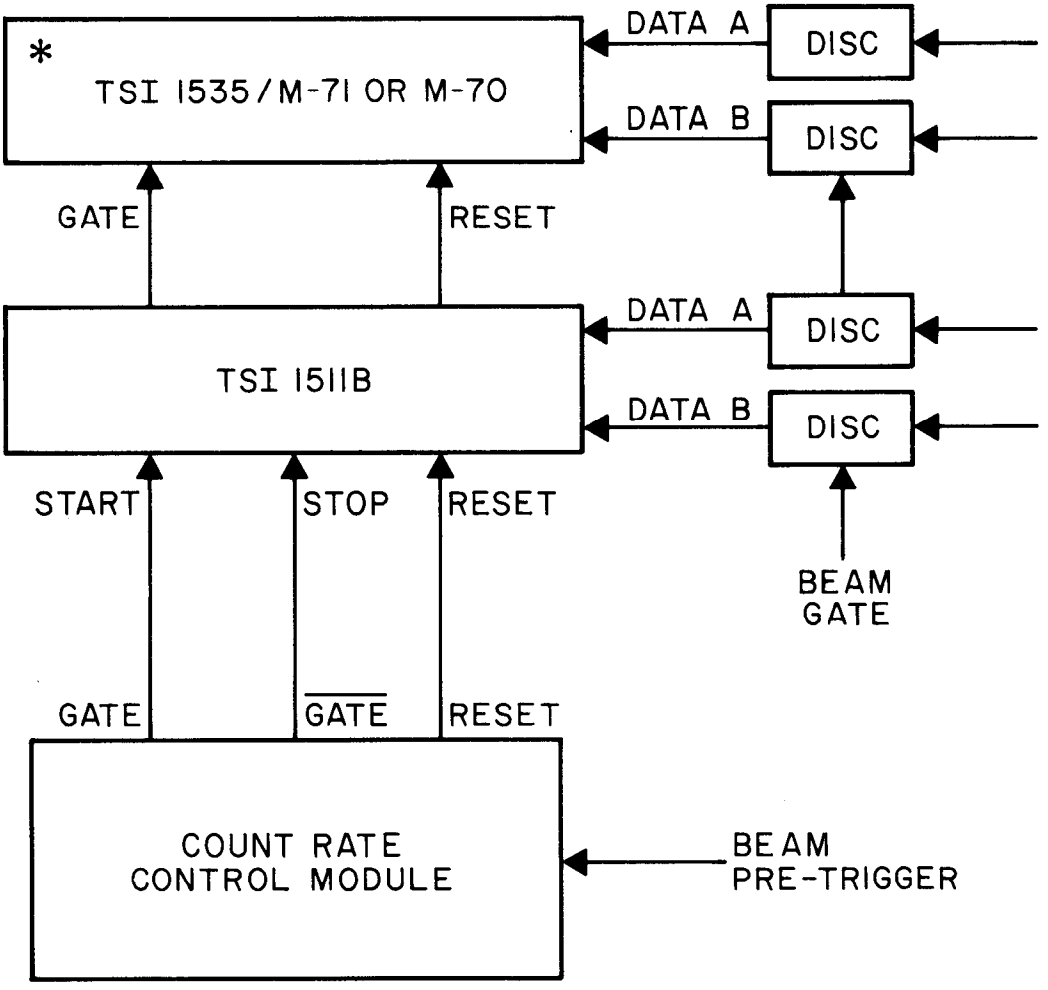
FIG. 2--Typical waveforms.



*NOTE:

GATE CONTROL IN "GATED" POSITION FOR M-71,
"ELECTRICAL" POSITION FOR M-70.

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FIG. 3--System interconnection.