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The R-ϕ Silicon Vertex Detector Simulation as Implemented in SICB

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Abstract

This note describes the current implementation of the silicon vertex detector simulation. The description includes the salient details of the silicon wafer geometry and the corresponding support material as well as the digitisation schemes employed. The note also explains the structure of the banks and errors on the cluster positions which are available to the user and, finally, lists a few items which have not been implemented at the time of this version (SICB v111), but which will be added to the simulation in future releases. This document is intended as a source of input for the corresponding section of the LHCB technical proposal.

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1 Introduction

The R-ϕ geometry of the silicon vertex detector is the successor to the X-Y geometry found in the LHCB letter of intent. The reasons for this change in design and the associated history are available elsewhere [1] and are not discussed in this note.

The geometry has been adapted and extended from the previous X-Y code. The silicon wafers are entirely new; but the support structures have largely been adapted to conform to the new wafer dimensions. Additionally, the upper and lower half stations have now been separated in Z, i.e. along the beam axis, to allow better coverage of gaps.

The digitisation distributes the charge collected on silicon strips which are subsequently reconstructed into clusters. The raw hit information, the digitised hit information, and the reconstructed cluster information are stored in ZEBRA [3] banks for access by the user. Error information on the cluster location is available via access routines.

2 The Geometry Description

The vertex detector, as implemented in the simulation, is divided into seventeen stations perpendicular to the beam axis (Z). Each station is divided into a physically decoupled upper and lower half. Each half consists of two planes of silicon, associated support plates and cooling plates, as well as RF shielding. Figure 1 shows a transparent view of the supports surrounding one of the upper half stations and a side view showing the various support and and cooling plates. The RF shield is not shown; it encases the entire structure shown in the figure.

The first (lower in Z) silicon plane in each half-station consists of twelve wafers with curved strips which maintain a constant radius (R). The second plane consists of six wafers which have strips which run along a tilted phi coordinate (ϕ). The strip rotation is 5° around the point of the strip's intersection with the minimum radius of its silicon section (or wafer.) The sign of this tilt alternates at each station. This stereo angle allows one to resolve ambiguities in the track reconstruction. Figure 2 shows the arrangement of these wafers for the R and ϕ cases.

Within each type of R wafer, the strip pitch is a constant. For the ϕ wafers, however, this is not possible without leaving large insensitive areas. So, the ϕ strips "grow" with radius out to a value of near around 100 μm at the outermost radius of the wafer; at the innermost radius, the pitch corresponds to that of the innermost R wafers. This is summarized in the table below:

Location	**Wafers per Half-Station**	**Pitch**
Inner R	6	40 μm
Middle R	3	60 μm
Outer R	3	80 μm
Inner ϕ	3	40-104μm
Outer ϕ	3	40-104μm

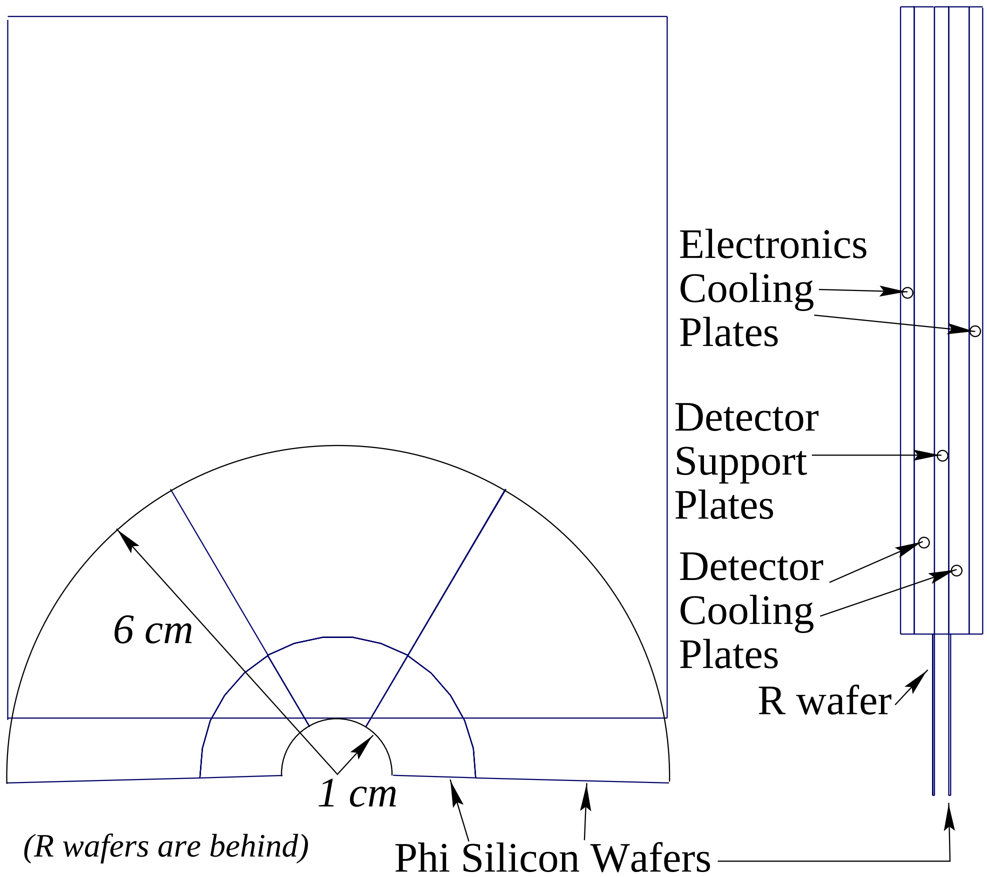

Figure 1: Front and Side Transparent Views of an Upper-Half Station

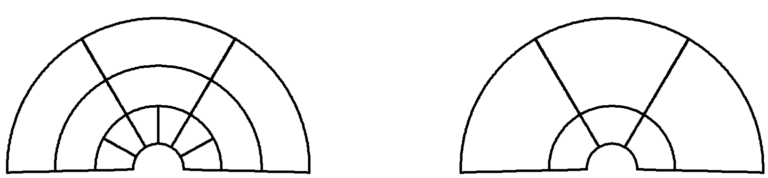

Figure 2: The wafer arrangement for the R and ϕ planes

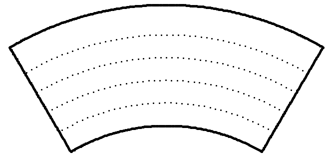

Figure 3: One of the middle R wafers with every 50th strip shown (scale 1:1)

The alignment of the strips of two different wafers is shown in figures 3 and 4.

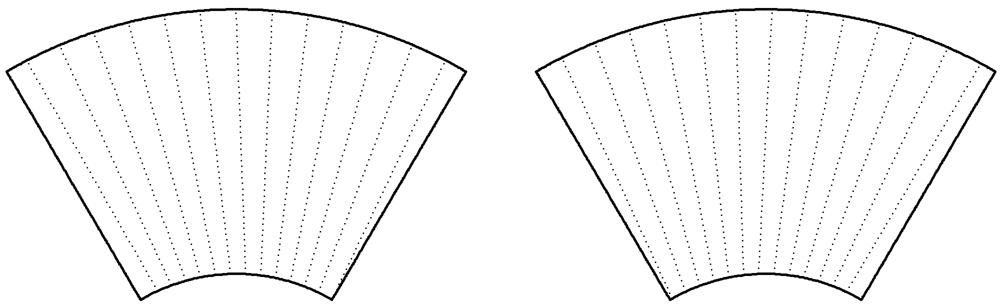

Figure 4: Two Outer ϕ Wafers with Every 50th Strip Shown (scale 1:1, note the stereo angle)

The geometry description has been implemented in GÉANT 3.21 [2] with the various silicon wafers being represented by separate GÉANT volumes which are summarized in the following table:

Name	**Description**	**Material**	**Shape**	**Z Extent**	**Instances**
VSRP	Silicon Wafer	Silicon	Tube Sec.	150μm	612
RFFB	F/R RF-Shield	Aluminum	Box	100μm	136
RFSD	Lower Side RF	Aluminum	Box	NA	136
RFBT	Top/Bottom RF	Aluminum	Box	NA	68
DCPU	Si Cooling Plate (Upper)	Beryllium	Box	1000μm	17
DCPD	Si Cooling Plate (Lower)	Beryllium	Box	1000μm	17
ECPU	Elec. Cooling Plate (Upper)	Beryllium	Box	1000μm	34
ECPD	Elec. Cooling Plate (Lower)	Beryllium	Box	1000μm	34
DSPU	Si Support Plate (Upper)	Beryllium	Box	1500μm	34
DSPD	Si Support Plate (Lower)	Beryllium	Box	1500μm	34
VSPC	Hole in Supports	(Vacuum)	Tube Sec.	(varies)	170

A few compromises have been made in the geometry description to accomodate the fact that GÉANT 3.21 only allows relatively simple shapes — e.g. boxes, tubes, spheres, etc....

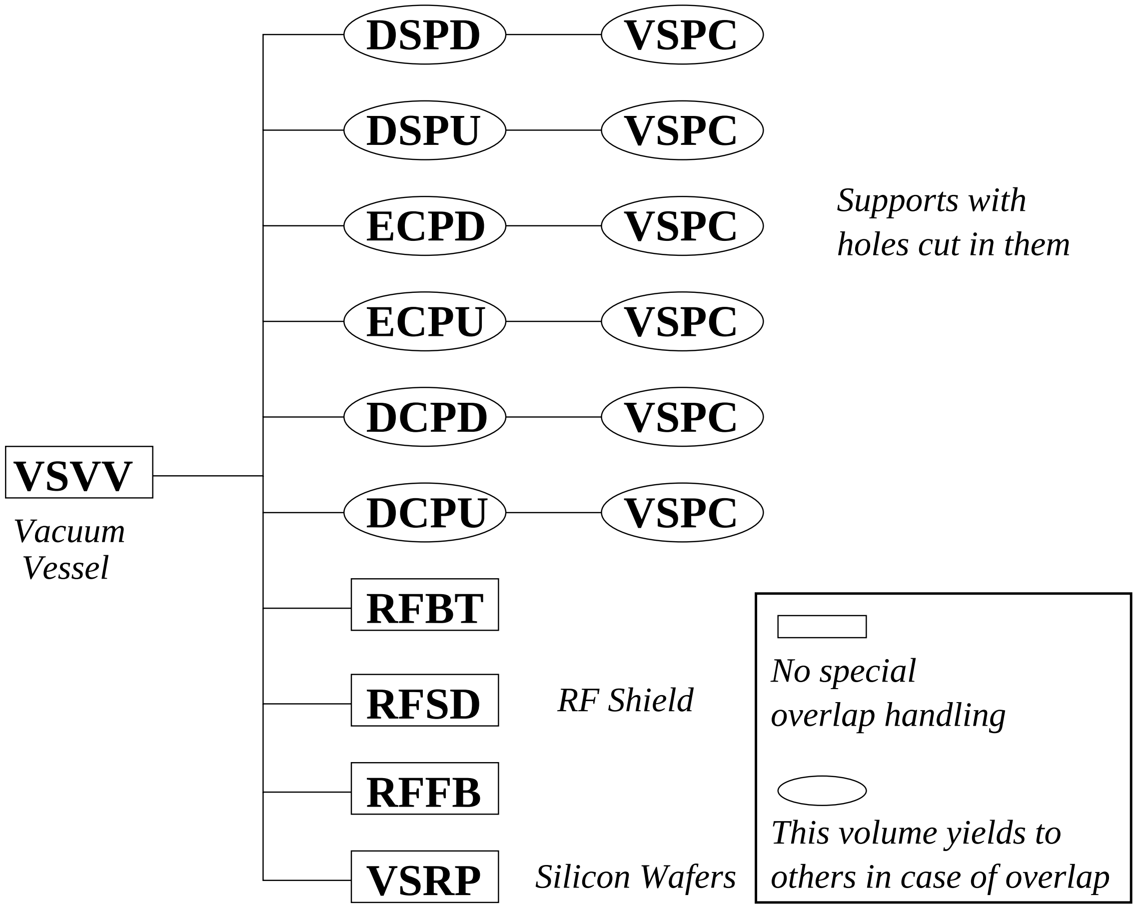

Figure 5: The Hierarchy of the Vertex Detector Volumes

In order to do anything more complex, one may perform simple unions, intersections, and subtractions of the simple volumes. One may also specify that certain volumes should be allowed to overlap other volumes, which is ordinarily not the case except for the normal mother/daughter volume relationship. This “special treatment” is useful in the case where a given volume may intersect several different volumes of different trees.

Both the normal mother/daughter relationship and such special overlap treatment are used in the vertex detector implementation as shown in figure 5. The RF shield and the silicon wafers themselves are defined as normal daughter volumes inside the vacuum vessel (VSVV) and thus supercede the vacuum vessel definition in the volumes that they occupy. For the support and cooling structures, however, it is difficult to conceive of a method to define them such that they have the required box-like shape with the necessary “hole” in the middle without applying special overlap treatment. The solution which has been applied is to define a vacuum volume (VSPC) which is embedded in each of the support and cooling volumes; then, the support, cooling, and vacuum volumes are all flagged so that where they intersect any “normal” volume (which is not similarly flagged), only the “normal” volume is used for purposes of particle propagation through the detector. The only major disadvantage to this technique is that it makes visualization of the vertex detector more complicated since the GÉANT drawing routines do not handle such special overlaps correctly under a number of circumstances.

Using the above set of volumes, the seventeen stations have been placed at the following Z locations in the SICB reference frame:

Station	**Upper Z** (cm)	**Lower Z** (cm)
1	-18	-16
2	-14	-12
3	-10	-8
4	-6	-4
5	-2	0
6	2	4
7	6	8
8	10	12
9	14	16
10	18	20
11	22	24
12	26	28
13	34	36
14	48	50
15	58	60
16	68	70
17	78	80

The following table summarizes the rest of the geometry parameters. Note that most of these are user-adjustable via modification of the vsrp.cdf file.

Vertex Detector Parameters	
Number of Stations	17
Z Offset of Lower Stations Relative to Upper	+2.0 cm
Angular Span of One Half Station	183°
Innermost Wafer Radius (for R and ϕ)	1.0 cm
Transition Radius from Inner to Middle R Wafers	2.5 cm
Transition Radius from Middle to Outer R Wafers	4.1 cm
Transition Radius from Inner to Outer ϕ Wafers	2.5 cm
Outermost Wafer Radius (for R and ϕ)	6.0 cm
Tilt of ϕ Strips	5°
Z Separation between R and ϕ Planes	1.0 mm
Silicon Guard Ring Thickness	52.5 μm
Angular crack between wafers	0.2 °

Note that since each half station is slightly larger that 180°, the lower halves are all offset in Z with respect to their upper halves by +2 cm. The choice of the Z location of each station comes from a qualitative assessment of the competing needs of having many measurements near the interaction point and in obtaining vertex information for tracks at small angles with respect to the beam.

There are a few differences between the vertex detector as found in the SICB simulation (v111) and the final detector as it is envisaged. First, in the simulation, the ϕ wafers have strips which do not traverse the entire R extent of the wafer in which they lie. In the final detector, such strips will not exist since the wafers will actually be cut along a "scribe" line defined by the strips. But since the only effect of this is to change the wafer in which the strip is located, it is not considered at the simulation level. Also, a small ring of material representing the electronics and associated cabling should be added in future releases of the simulation; however, the amount of material which is currently present is considered sufficient to give a reasonable representation of particle passage through the vertex detector.

3 The Hit Digitisation

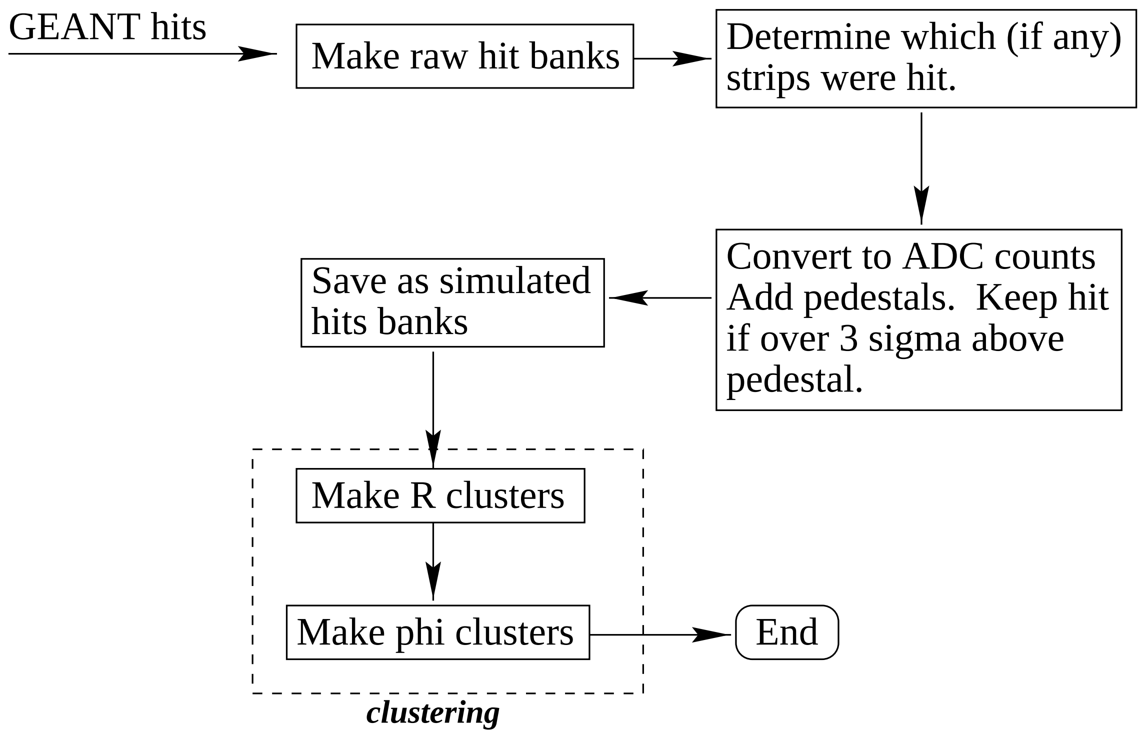

Figure 6: An Overview of the Digitisation and Reconstruction Processes

The digitisation of hits in the vertex simulation is performed in two steps. First, for every track which crosses a silicon wafer, its entry point, exit point, and the energy deposited are extracted from the raw banks (VRPR), and that information is used to determine how many silicon strips were hit and how much energy was deposited in each of them. Then for each wafer, the strips are grouped together into clusters accordingly during the subsequent reconstruction. A flowchart of this is shown in figure 6.

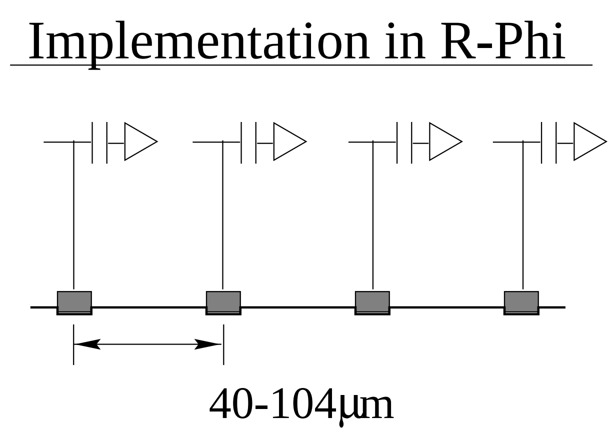

Figure 7: The Strip Implementation

Before considering how this is done, however, it is worth pointing out that in the current R-ϕ setup, capacitive coupling is not used. i.e. every strip is read out; see figure 7. This also has the advantage of eliminating the 35% signal loss which such capacitive coupling induces [4], due to the charge sharing, thus improving the signal-to-noise ratio which is an important factor in such a high radiation environment. In addition to these considerations, the "n-on-n" technology which will be used to improve resistance to radiation damage is incompatible with having floating strips for the strip pitches that we intend to use.

To distribute the energy over the silicon strips, several steps are performed. First, the entry and exit points along the detector are converted to strip numbers; information is also kept to indicate where along the strip the particle entered or exited. The last piece of information is the strip pitch which is a known constant for the R Wafers. For ϕ wafers, the pitch is given by:

$$\mathrm{Pitch}_{\phi}(\mathrm{r}) = \mathrm{Pitch}_{\mathrm{r}=\mathrm{r}_{\mathrm{min}}} \times \mathrm{r}$$

where $\mathrm{Pitch}_{\mathrm{r}=\mathrm{r}_{\mathrm{min}}}$ is defined as the pitch of the inner R wafers, i.e. currently 40 μm. For simplicity, the pitch is assumed to be a constant for a given track and is taken as the average of the pitches at the entry and exit points along the wafer. Then, The total path of the particle through the wafer is calculated. Using the knowledge of the pitch, the energy deposited in the wafer is distributed according to the fraction of the path covered by that strip, i.e.:

$$\mathrm{E}_{\mathrm{strip}} = \frac{\mathrm{d}_{\mathrm{strip}}}{\mathrm{d}_{\mathrm{total}}} \times \mathrm{E}_{\mathrm{total}}.$$

The implemented solution is the most conservative one, given the worst precision. In an attempt to improve how realistically the charge is distributed, we plan to introduce a second version of this routinge which actually simulates the transport of the charge to the strips. It should be introduced in the near future. A flag in the configuration file will enable the user to choose either the old or this new method.

Vertex Detector Digitisation Parameters	
ADC Counts / GeV Deposited	2.0×10^6
Maximum ADC Value	1023 (10 bits)
Mean Pedestal Value	50 ADC Counts
Individual Pedestal Width (constant)	5 ADC Counts
Threshold Cut for Hit Strips	3 Sigma Above Pedestal

For each strip, the energy deposited is converted to an ADC count to which a pedestal value is added. The pedestal value is smeared by the Gaussian with a width defined in the configuration file; this current width is 5 ADC counts for all channels. The resulting hits are required to be three sigma above threshold in order to be kept. The threshold may be changed by the user.

4 The Reconstruction: Clustering, Banks, and Errors

At this point, the information available at the simulation level, is identical to that which is available from real data: i.e. address information and an ADC value for each strip which was hit. The clustering algorithm which follows can thus handle Monte-Carlo and real data.

After all the hit strips have been determined, the strips are grouped into clusters in order to reconstruct the energy deposited from the passage of a single track. Because the clusters are of small dimensions, the maximum being around 500 μm, one can approximate all the strips as being (locally) parallel; in this way, clusters for both the R and ϕ wafers may be treated in the same manner. Then a very simple algorithm, whose flow is shown in figure 8, is used to construct these clusters. The algorithm can be summed up as follows. For each wafer, one takes the strip with the largest energy deposition along with the nearest neighbor strips which have been hit. Also, for each nearest neighbor which has been hit, its next-to-nearest neighbor strip becomes part of the cluster provided it has also been hit. Thus one can have, at maximum, five strips in a cluster. All the strips used in the cluster are marked as used and are not considered for further clusters in the event. The whole process is repeated with the best remaining strip, in terms of energy deposition, being chosen and its neighbors checked, etc... until no hit strips remain in the wafer. There is currently no special treatment of clusters which overlap.

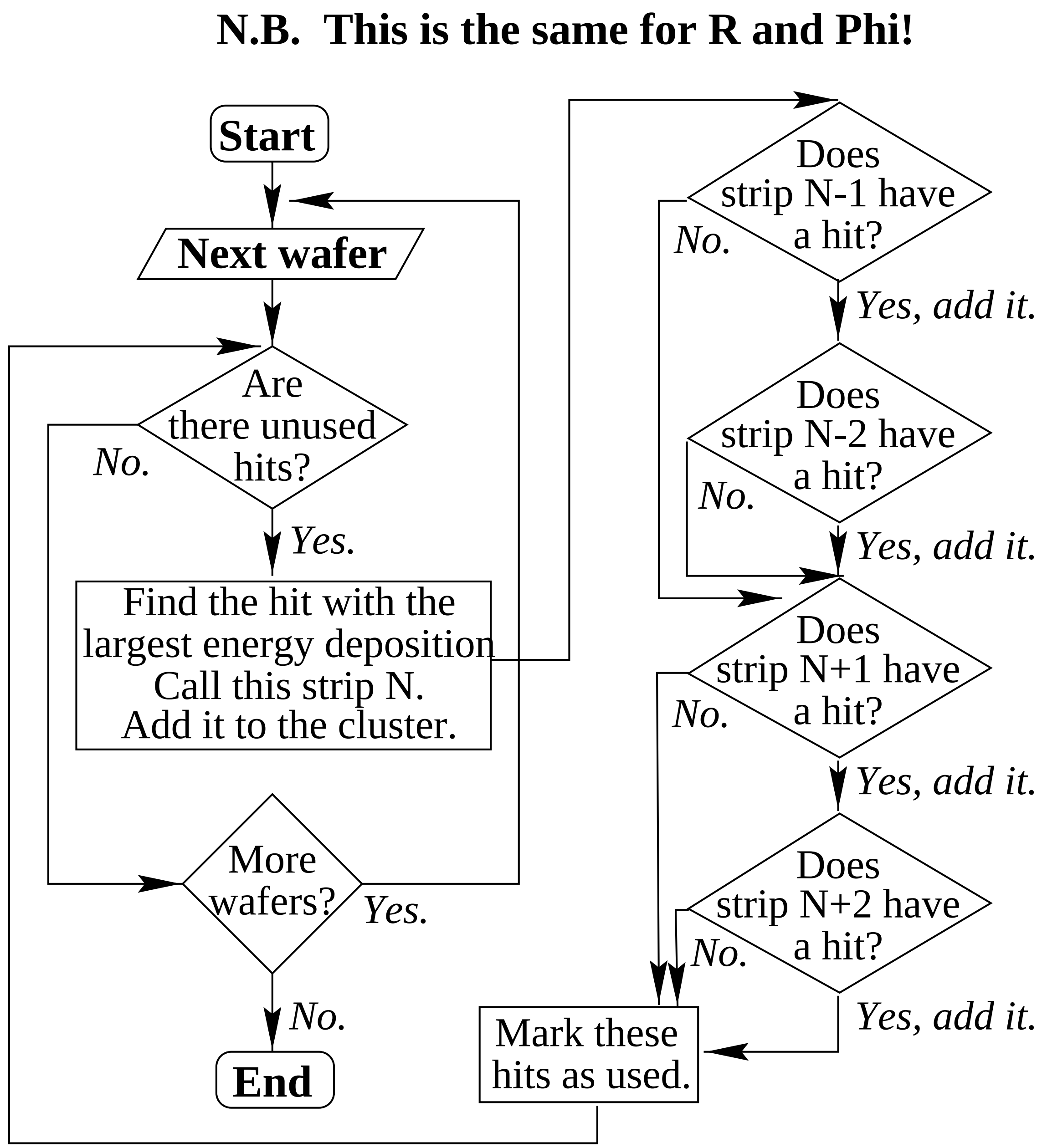

Figure 8: A Flow Diagram of the Clustering Algorithm

All the information which is available: the raw information obtained from GÉANT, the digitised hit information, and the cluster information are stored in banks to which are added links to allow cross-referencing of related information. This includes, not only these banks, but also the Monte-Carlo tracks. Figure 9 shows the organisation of the links between the banks.

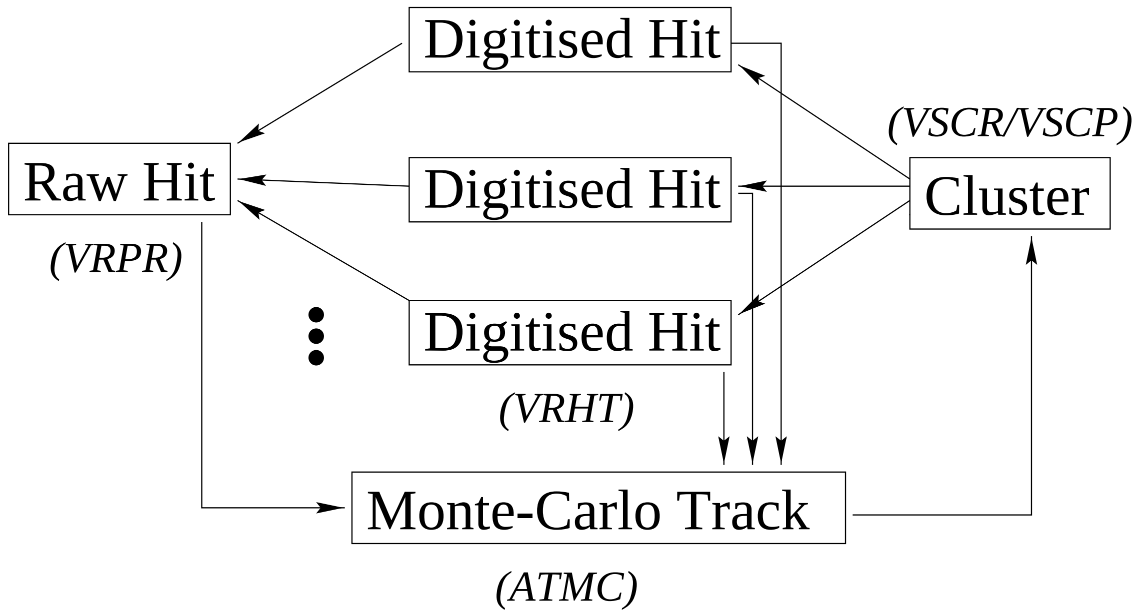

Figure 9: The References between the Various Banks

The contents of the banks, themselves, are given in the following tables:

The Raw Hit Bank - VRPR		
Mnemonic	**Type**	**Meaning**
`EN_R`	`Real`	R Coordinate at Entry Point (cm)
`EN_PH`	`Real`	ϕ Coordinate at Entry Point (cm)
`EN_Z`	`Real`	Z Coordinate at Entry Point (cm)
`EX_R`	`Real`	R Coordinate at Exit Point (cm)
`EX_PH`	`Real`	ϕ Coordinate at Exit Point (cm)
`EX_Z`	`Real`	Z Coordinate at Exit Point (cm)
`EDEP`	`Real`	Energy Deposited in the Wafer (KeV)
`ATMC`		Reference to the Monte-Carlo Track

The Digitised Hit Bank - VRHT		
Mnemonic	**Type**	**Meaning**
`TYP`	`Integer`	R Hit=1, ϕ Hit=2
`DET`	`Integer`	ϕ Sector 1-6
`SEC`	`Integer`	For R: Inner-lesser-ϕ,Inner-greater-ϕ,Middle, Outer = 1,2,3,4
		For ϕ: Inner,Outer = 1,2
`NSTR`	`Integer`	Strip Number
`Q`	`Real`	Non-rounded ADC value
`ADC`	`Integer`	ADC Value
`ATMC`		Reference to the Monte-Carlo Track
`VRPR`		Reference to the Raw Hit Bank

The R Cluster Bank - VSCR		
Mnemonic	**Type**	**Meaning**
R	Real	R Coordinate
DET	Integer	ϕ Sector 1-6
SEC	Integer	(same as SEC for VRHT)
Z	Real	Z Coordinate
CENW	Real	The Weighted Cluster Center (strip number)
CENG	Real	The Unweighted Cluster Center (strip number)
ADC	Real	The Cluster Pulse Height (ADC Counts)
W	Real	The Cluster Width $\equiv$ number of strips
VRHT		Reference to the Digitised Hit Bank(s)

The ϕ Cluster Bank - VSCP		
Mnemonic	**Type**	**Meaning**
PHI	Real	ϕ Coordinate at the Wafer's Minumum Radius
DET	Integer	ϕ Sector 1-6
SEC	Integer	(same as SEC for VRHT)
Z	Real	Z Coordinate
CENW	Real	The Weighted Cluster Center (strip number)
CENG	Real	The Unweighted Cluster Center (strip number)
ADC	Real	The Cluster Pulse Height (ADC Counts)
W	Real	The Cluster Width $\equiv$ number of strips
VRHT		Reference to the Digitised Hit Bank(s)

For the raw and digitised hit banks, the wafer "address" information is given by decoding the partition number for the raw banks. For the cluster banks, there is one partition for each station, the rest of the information being contained in the bank, itself.

Errors on the cluster location are not stored in the cluster banks, but instead, are available via access routines. Currently these routines use only the local strip pitch and the number of strips in the cluster to extract the errors from a hard-coded table. The values in the table, shown below, have been chosen so that the residual distribution, given by:

$$\text{residual} = \frac{\text{Position}_{\text{Reconstructed}} - \text{Position}_{\text{MC}}}{\sigma}$$

has a width of $\cong 1$.

	Number of Strips		
	1	2	$\geq 3^{\dagger}$
Inner R	9 μm	6 μm	20 μm
Middle R	13 μm	10 μm	30 μm
Outer R	18 μm	10 μm	40 μm
ϕ	$\frac{\text{localpitch}}{\sqrt{12}}$		

†Note that in the case of ≥ 3 strips, it is quite likely that two tracks have contributed to the cluster and so we deliberately make the errors somewhat larger in order to reduce the weight

it is given in the Kalman filter used in the tracking routines. ϕ clusters do not have hard coded errors since they are almost always single strip clusters where the formula given in the table applies; a thorough study of the errors for the multi-strip case in ϕ wafers has not been done, but is planned after introducing the proper charge diffusion in the silicon. Also note that the R errors are currently fixed to the current default strip pitches; so the correct error will not be returned if the pitches are changed by the user.

5 Future Improvements

There are a few things that are not present in the default version of SICB v111 which should be added with regard to the reconstruction. These include the addition of noise hits (i.e. to better simulate radiation damage of the detector), handling of cluster overlap, and a more systematic study of the errors as a function of various parameters in order to allow one to change the strip pitch while still obtaining reasonable errors. With regard to the geometry, the cooling and support plate geometry needs to be optimised. I anticipate adding these improvements to future releases.

References

[1] LHCb Technical Proposal, Silicon Vertex Detector Section, , 1998.

[2] M. Goosens et al., *GÉANT — Detector Description and Simulation Tool*, CERN Program Library Long Writeup W5013 (Revised), CERN, Geneva, Switzerland, March, 1995.

[3] M. Goosens et al., *The ZEBRA System*, CERN Program Library Long Writeups Q100/Q101, CERN, Geneva, Switzerland, February, 1995.

[4] P.P. Allport et. al. "Charge Division Issues with LHC Silicon Microstrip Detectors", CERN SCAN preprint.