Design and Simulation of 10 Gigabit Ethernet on Altera FPGA

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Introduction

With the planned increase in beam luminosity [1] for proton-proton and lead-lead collisions at the CERN Large Hadron Collider (LHC), there will be manifold increase in the traffic of experimental data. The ALICE experiment is getting ready to cope up with the increased data rate and data traffic. It is driving scientists and engineers to look for faster network solutions to cater to the needs for increased bandwidth demand. The 10 Gigabit Ethernet standard provides a significant increase in the bandwidth. It retains the key Ethernet architecture, the Media Access Control (MAC) protocol, the Ethernet frame format, and the minimum and maximum data frame size.

Under the Open Systems Interconnection (OSI) model [2], Ethernet is composed of Physical Layer and the Data Link layer as shown in figure 1. It is implemented in the lower sub-layer of the Data Link, which is known as the MAC. The MAC sub-layer has the responsibility for data encapsulation, frame assembly and frame parsing. It also controls the initiation of frame transmission and recovery from transmission failure due to data collision. The upper sub-layer of the Data Link layer is called the Logical Link Control (LLC). It handles the communication between the upper and the lower layers of the Data link.

This paper presents the design of 10 Gigabit Ethernet communications along with its functional simulation on Altera FPGA technology.

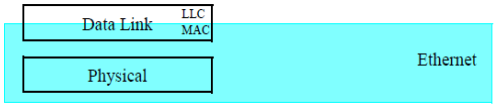

Figure 1: Showing Ethernet position in OSI model

Design for 10 Gigabit Ethernet

The design of 10 Gigabit Ethernet for Altera Stratix V GX chip is accomplished by using Qsys (Altera's System Integration Tool) and NIOS II processor (32 bit embedded processor) with other peripheral components, as shown in figure 2

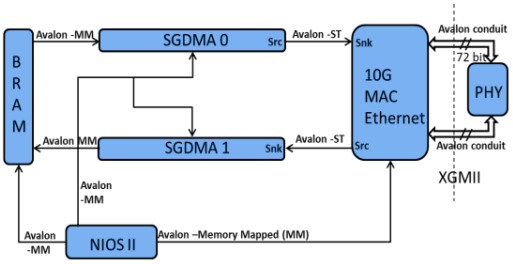

Figure 2: Data loopback design for Altera 10 Gigabit Ethernet

This subsystem takes a clock signal and an active-low reset signal as input, and communicates with the external Physical (PHY) chip through a 10 Gigabit Media Independent Interface (XGMII) [3]. The NIOS II processor is used to run the application programs to control communication with the host computer. It is programmed through a JTAG chain. The 10 Gigabit Ethernet Intellectual Property (IP) provided by Altera, implements the MAC sub-layer and a partial Physical sub-layer when needed based on the interface type. The two Scatter Gather Direct Memory Access (SGDMA) controllers are used to transmit and receive functions of the MAC IP. The Block RAM (BRAM) is used for the storage of program code and buffering of data. Descriptors for the SGDMA controllers are used for fast buffering of data with minimum processor interference.

This design includes an Ethernet MAC with an Avalon Streaming (Avalon-ST) interface on the client side, and a standard XGMII interface

on the network side. This design aims to send the data to the PHY via XGMII interface and receiving it back. Dual Clock First In First Out (DC FIFOs) buffers are used between the two SGDMA and the Ethernet MAC core for clock domain crossing.

Test Data Packet

A test data packet in the Ethernet frame format is transmitted via XGMII. It is a 64 bytes datagram. First 6 bytes are for destination address, next 6 bytes are for source address, 2 bytes to specify the length of the data followed by the test data to be transmitted. It also has option for four bytes of Frame Check Sequence in CRC32 frame format [4] to be appended. Padding is optional and only needed when the data packet is smaller than 38 octets or bytes to ensure the minimum frame size of 64 octets as specified in the IEEE 802.3 standards.

Frequency Translation

Incoming data on the 64 bit parallel XGMII lines is accepted at a clock frequency of 156.25 MHz as shown in figure 3. It is then multiplexed to 16 bit parallel lines and the frequency is raised to 625 MHz. 64B/66B bit encoding is applied for clock recovery and to avoid any DC shift [5]. The frequency of the data in 16 bit parallel lines is also raised to 644.53125 MHz, then the data goes to Serializer/Deserializer, after this it is transmitted from the silicon to the physical media, through optical fiber with a data rate of 10.3125 Gbps.

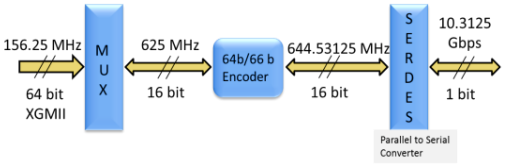

Figure 3: Three level of frequency translation in 10 Gigabit Ethernet communication

Simulation

The design and interconnection is done in Qsys using the standard IP cores provided in Altera Quartus II software. The testbench system is generated along with the simulation model in Verilog. Software for the NIOS II processor is developed in Eclipse IDE (Integrated Development Environment for NIOS II software development). The design is simulated in ModelSim Altera version 10.1.

Results

The data packet is transmitted to the Ethernet MAC. The simulation waveforms in figure 4 shows the output of the DC FIFO giving input to the MAC and the data at the output of the MAC after the loopback. The two data match with each other. It validates the functionality of this 10 Gigabit Ethernet communication design.

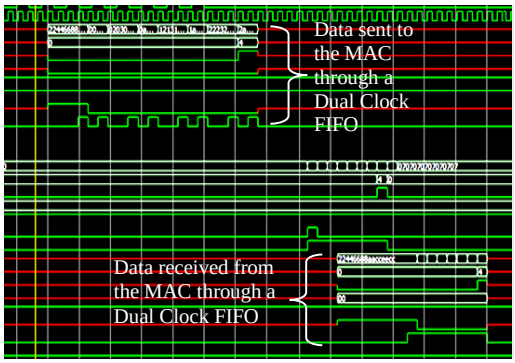

Figure 4: ModelSim Simulation waveforms for data loopback

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